Introduction to FACTS Controllers
Theory, Modeling, and Applications

(FIGURES)

Kalyan K. Sen, Ph.D., P.E.
Mey Ling Sen, M.E.E.

CHAPTER 1

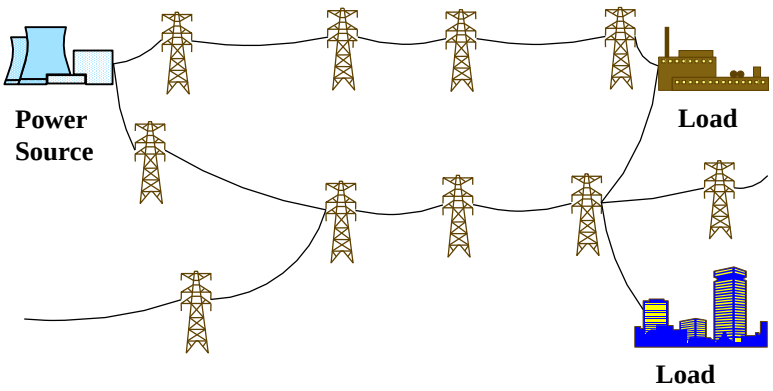


Figure 1-1. Part of a large interconnected transmission system supplying electric power from the generating point to the loads.

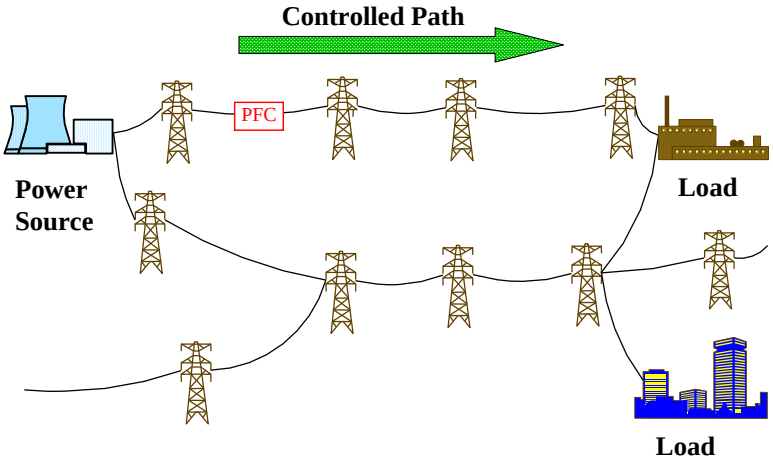


Figure 1-2. Power flow along a controlled path.

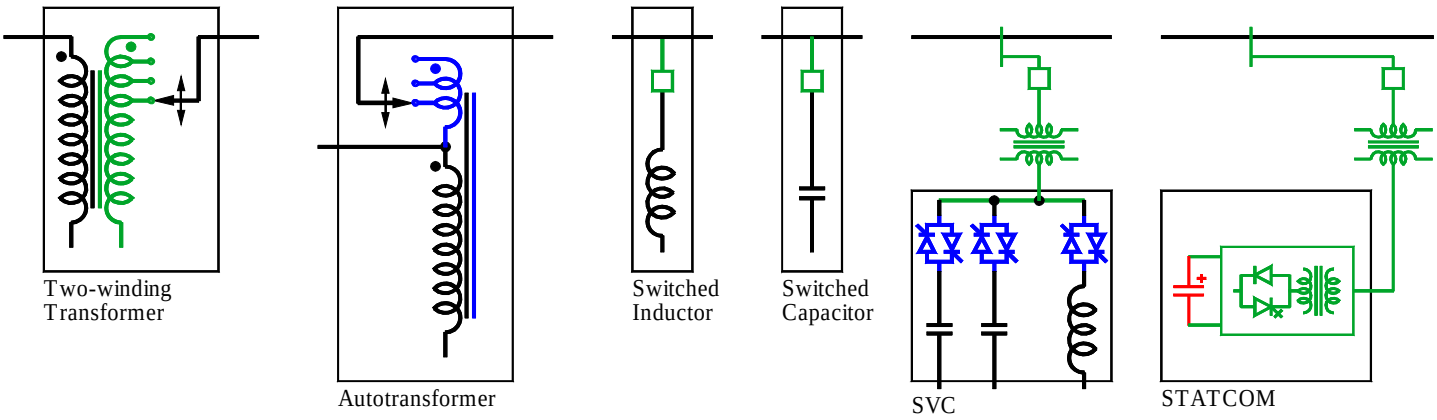


Figure 1-3. Transmission line voltage regulators.

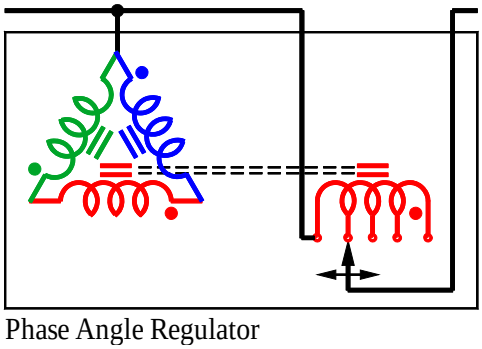


Figure 1-4. Transmission line voltage phase angle regulator.

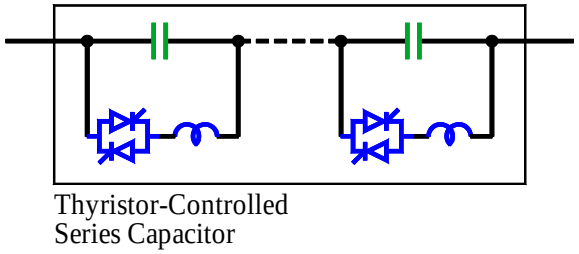


Figure 1-5. Thyristor-controlled series capacitor for transmission line reactance regulation.

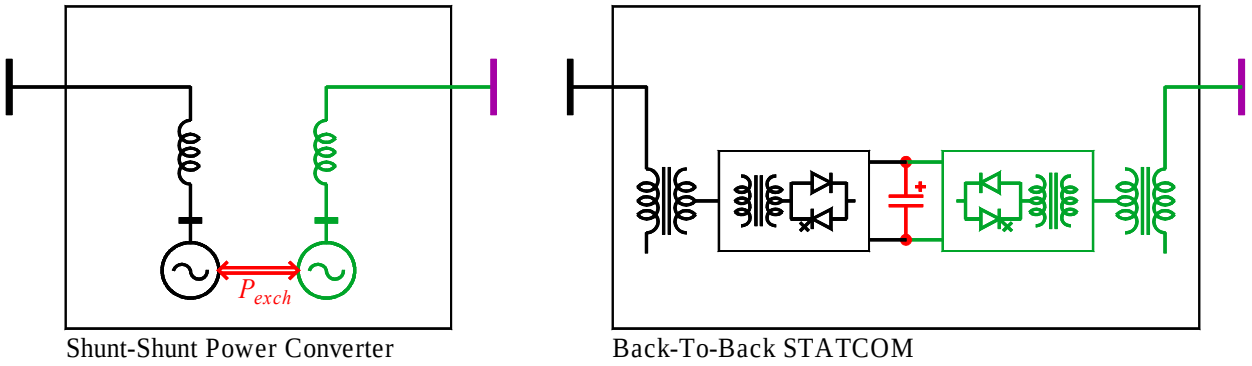


Figure 1-6. Point-to-point transfer of power with local reactive power compensation using a shunt–shunt power converter (BTB-STATCOM).

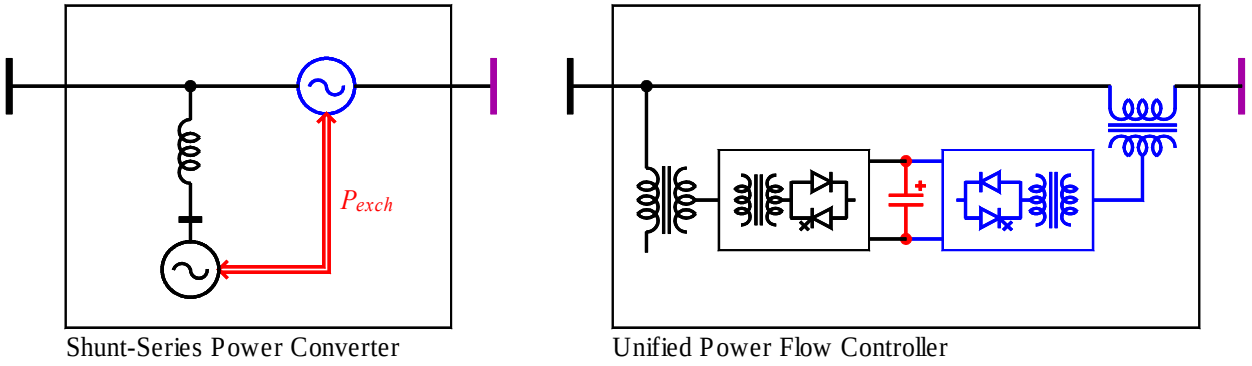


Figure 1-7. Independent active and reactive power flows controller with local reactive power compensation using a shunt–series power converter (UPFC).

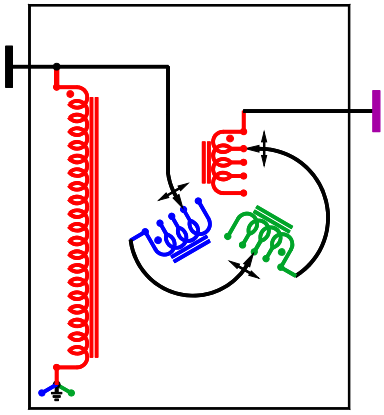


Figure 1-8. Sen transformer.

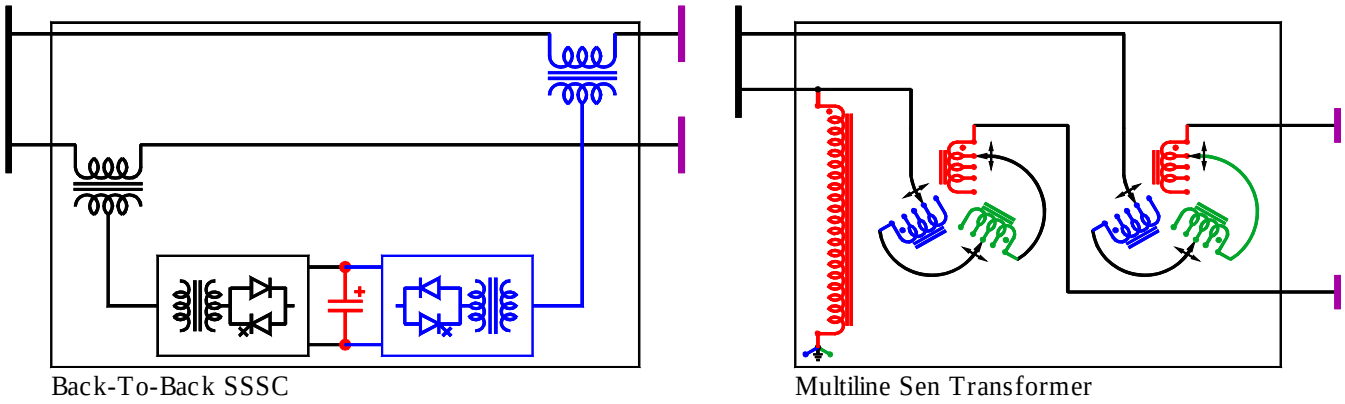


Figure 1-9. Multiline power flow concepts.

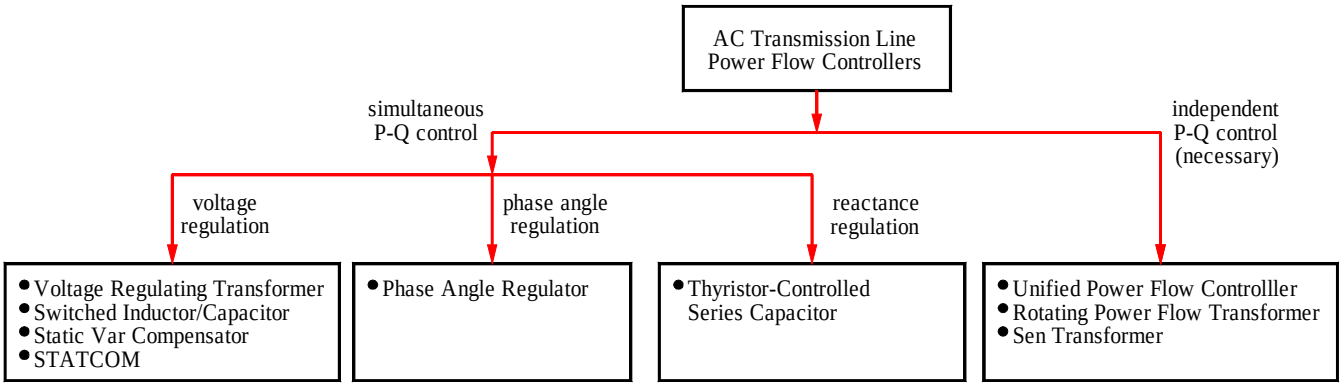


Figure 1-10. Choices for transmission line control equipment.

CHAPTER 2

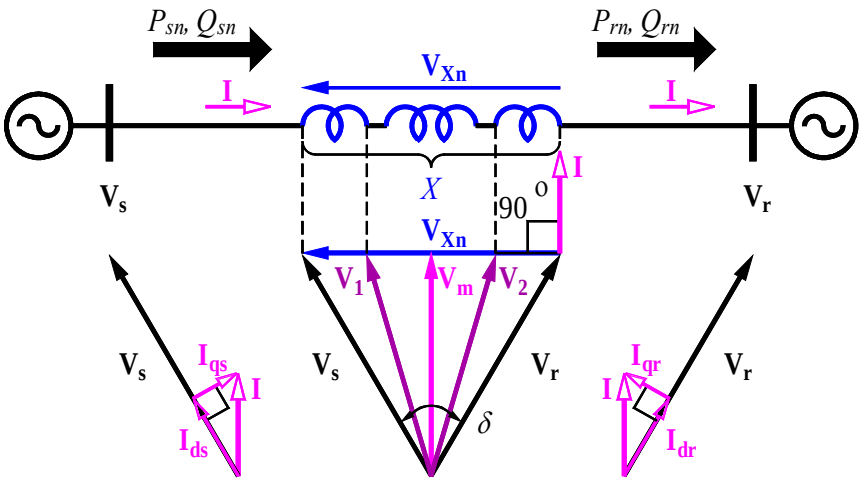


Figure 2-1. Simple power transmission system and the related phasor diagrams.

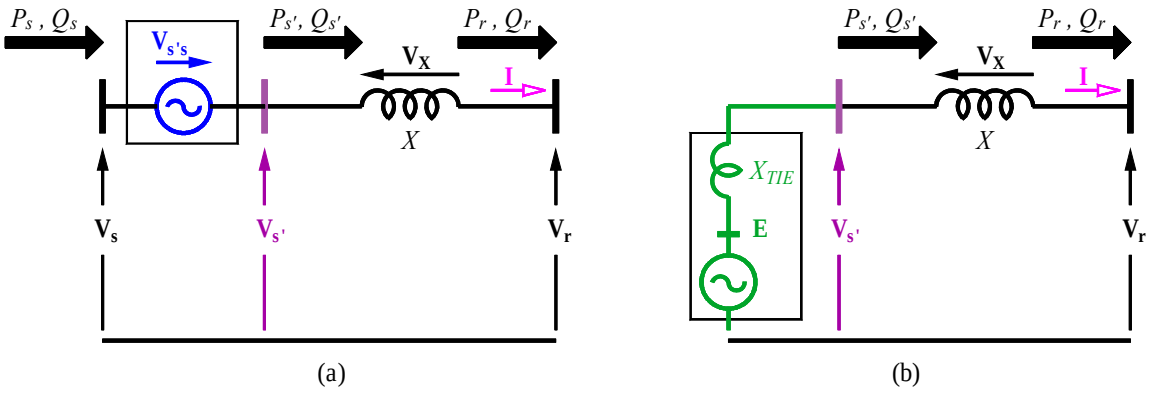


Figure 2-2. Two methods of controlling a transmission line voltage: (a) with a series-connected compensating voltage and (b) with a shunt-connected compensating voltage.

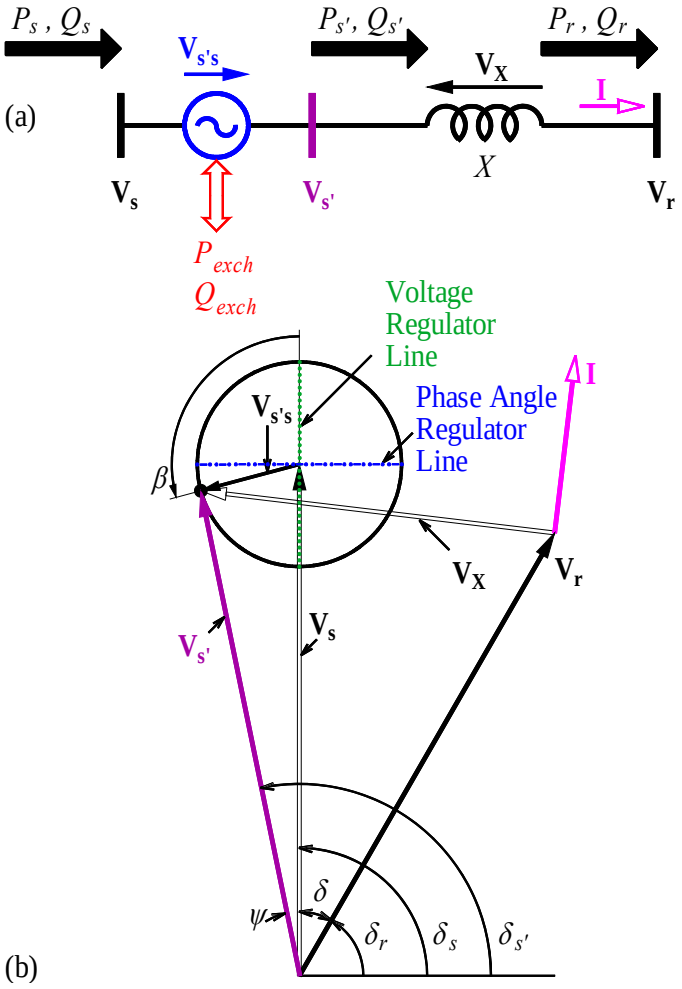


Figure 2-3. (a) Power transmission system with a series-connected compensating voltage ($\mathbf{V_{s's}}$). (b) Phasor diagram.

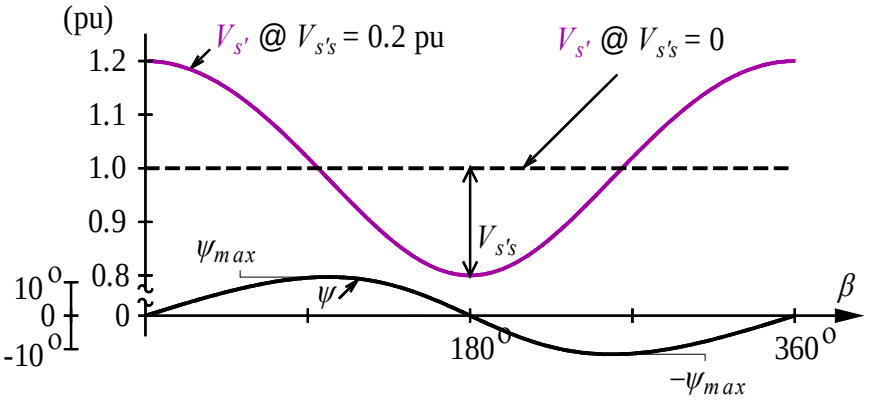


Figure 2-4. Variations of the magnitude ($V_{s'}$) and phase angle (ψ) of the modified sending-end voltage as a function of the relative phase angle (β) of the compensating voltage ($\mathbf{V_{s's}}$) with a fixed magnitude of 0.2 pu.

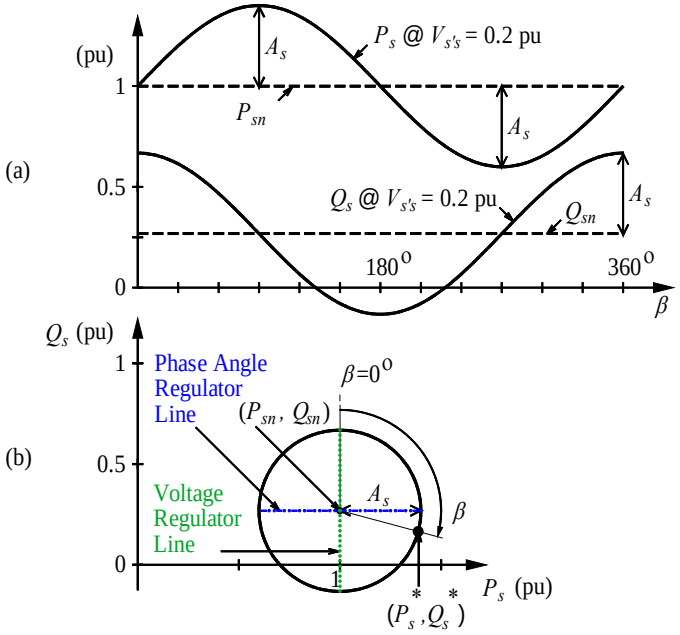


Figure 2-5. (a) Variation of the sending-end active and reactive power flows (P_s and Q_s) as a function of the relative phase angle (β) of the compensating voltage ($\mathbf{V_{s's}}$) with a fixed magnitude of 0.2 pu. (b) Sending-end Q_s versus P_s.

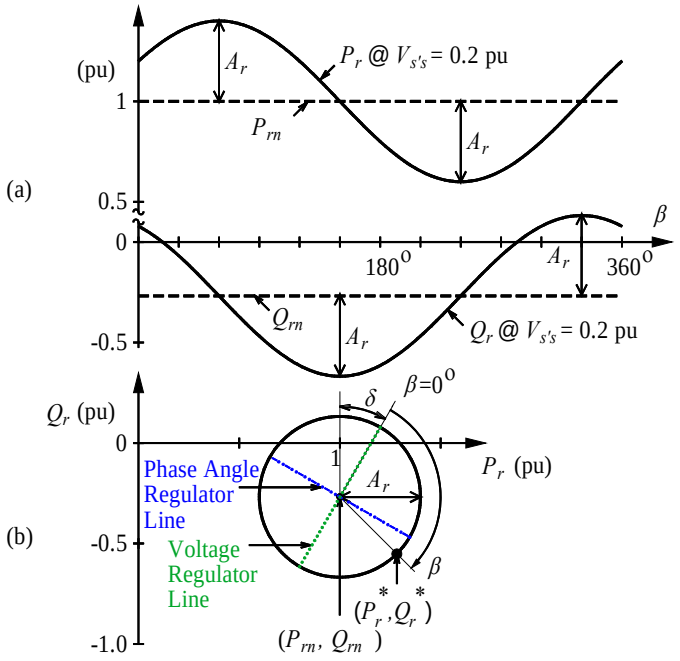


Figure 2-6. (a) Variation of the receiving-end active and reactive power flows (P_r and Q_r) as a function of the relative phase angle (β) of the compensating voltage ($\mathbf{V_{s's}}$) with a fixed magnitude of 0.2 pu. (b) Receiving-end Q_r versus P_r.

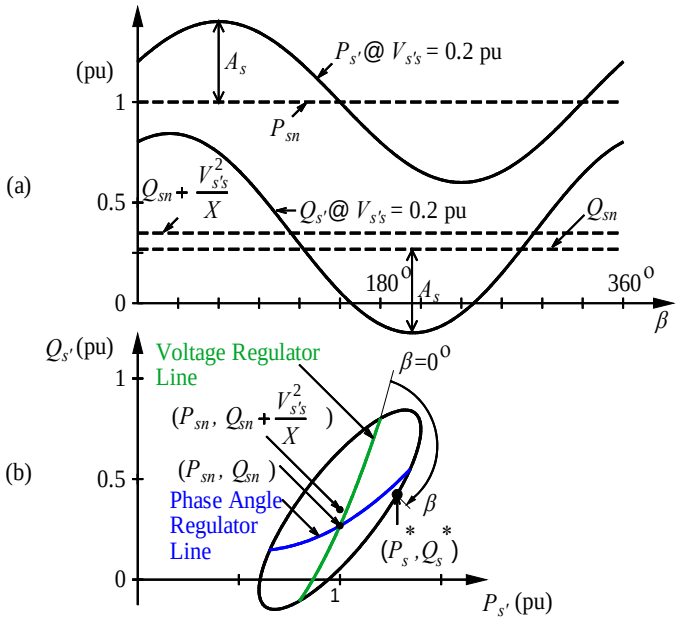


Figure 2-7. (a) Variation of the modified sending-end active and reactive power flows ($P_{s'}$ and $Q_{s'}$) as a function of the relative phase angle (β) of the compensating voltage ($\mathbf{V_{s's}}$) with a fixed magnitude of 0.2 pu. (b) Modified sending-end $Q_{s'}$ versus $P_{s'}$.

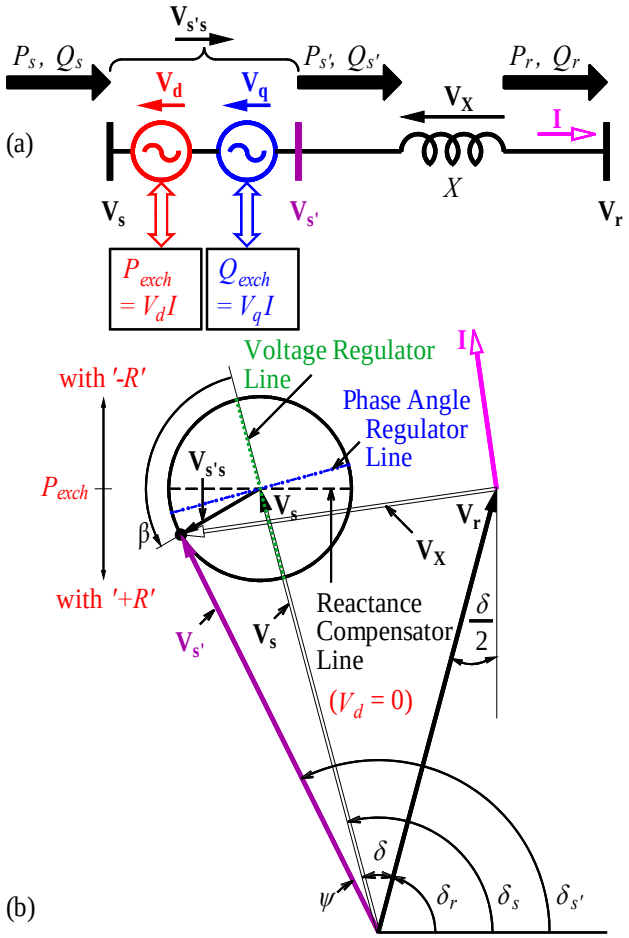


Figure 2-8. (a) Power transmission system with a series-connected compensating voltage ($\mathbf{V_{s's}}$). (b) Phasor diagram.

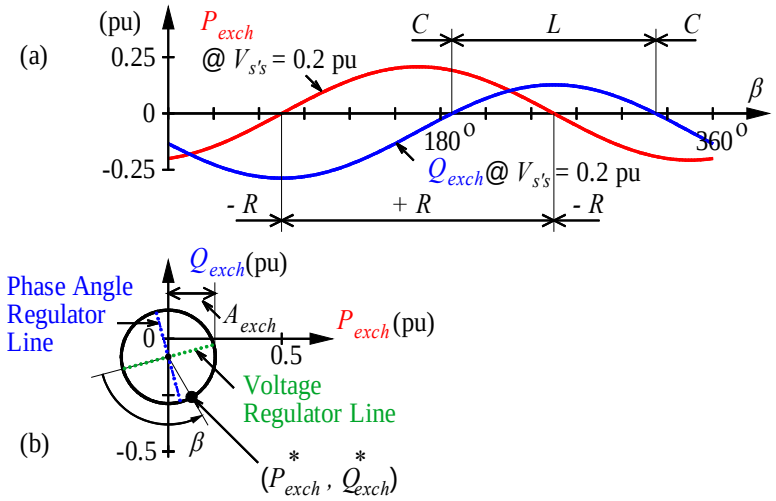


Figure 2-9. (a) Variation of the exchanged active and reactive powers (P_{exch} and Q_{exch}) as a function of the relative phase angle (β) of the compensating voltage ($\mathbf{V}_{s's}$) with a fixed magnitude of 0.2 pu. (b) Exchanged reactive power (Q_{exch}) versus active power (P_{exch}).

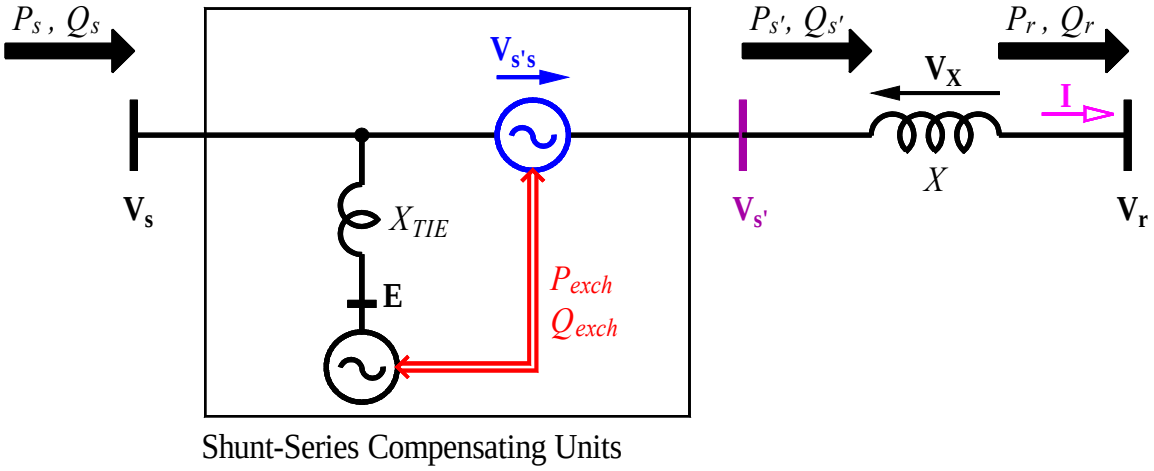


Figure 2-10. Scheme for implementing a series-connected compensating voltage.

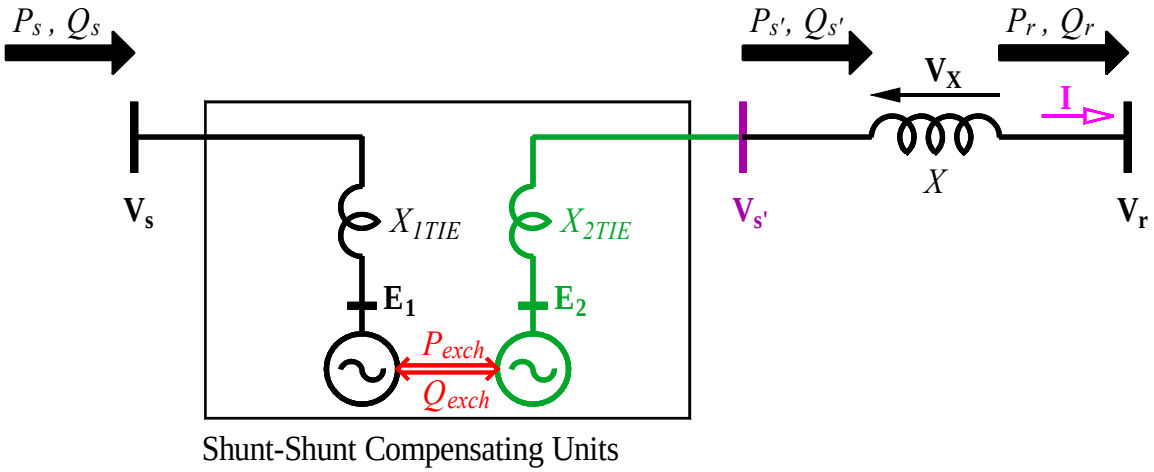


Figure 2-11. Scheme for implementing a shunt-connected compensating voltage.

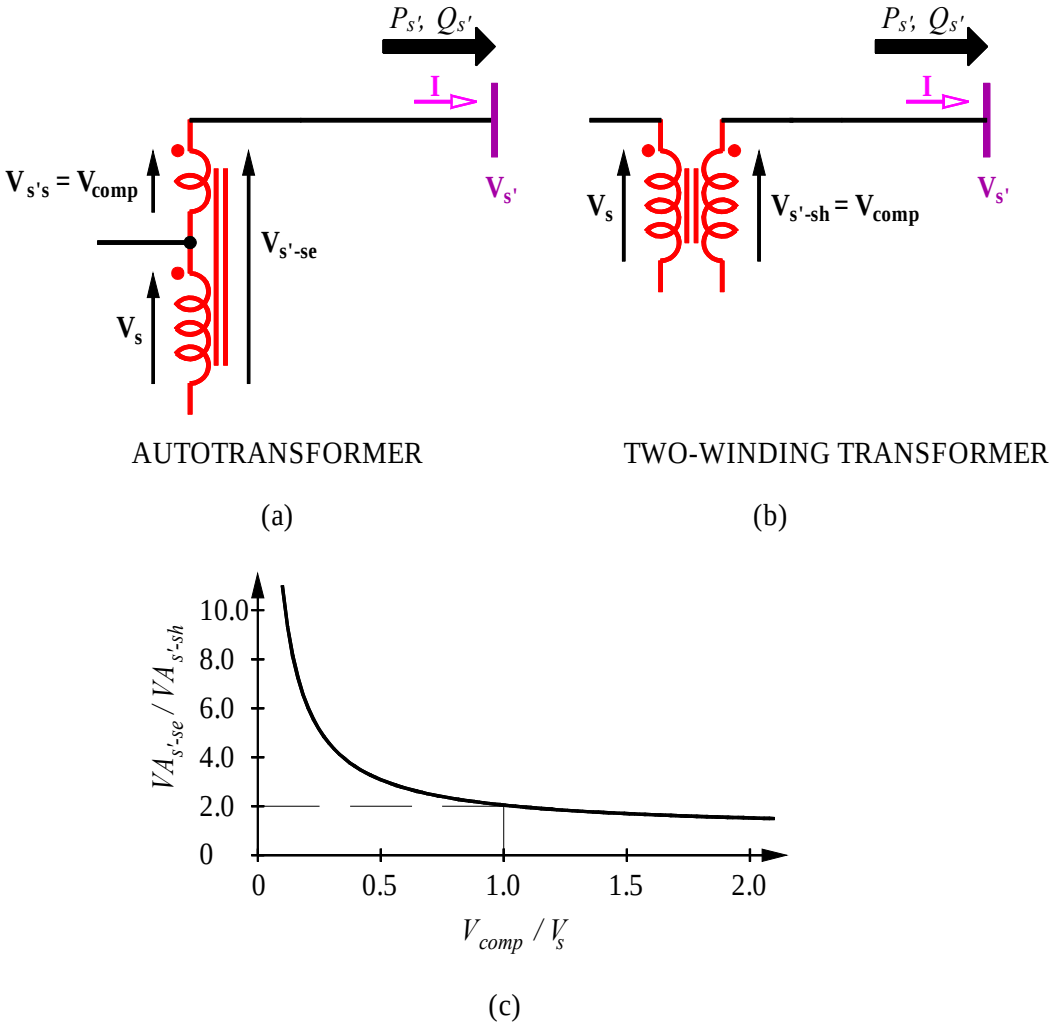


Figure 2-12. (a) Autotransformer. (b) Two-winding transformer. (c) Ratio of the transmitted VAs with series-compensated and shunt-compensated voltages as a function of normalized compensating voltage.

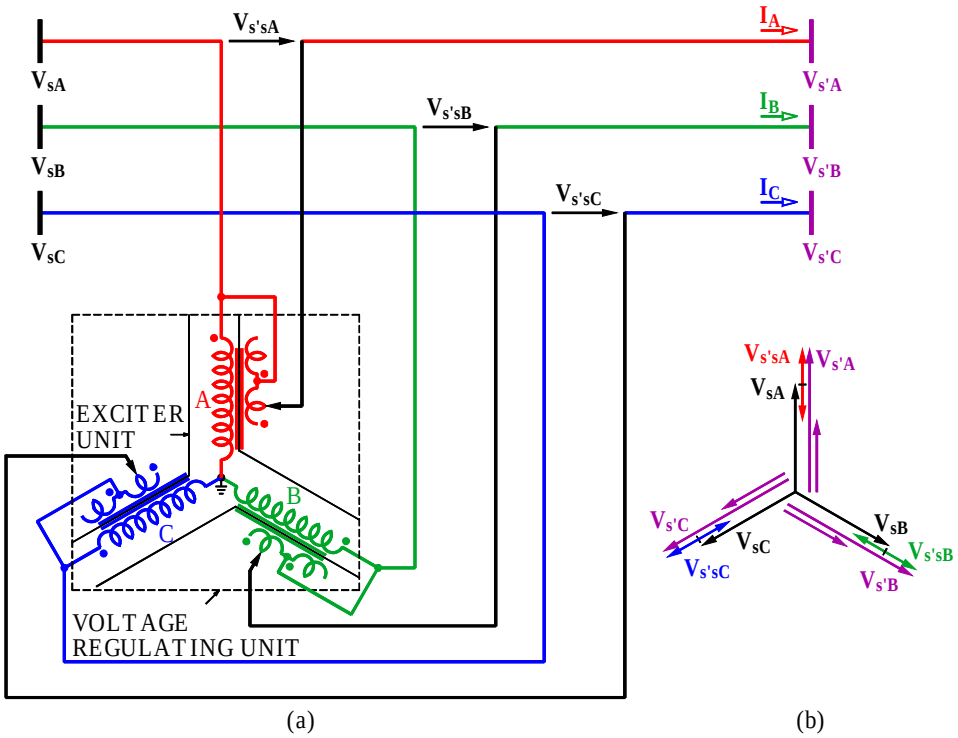


Figure 2-13. (a) Voltage regulating transformer. (b) Phasor diagram.

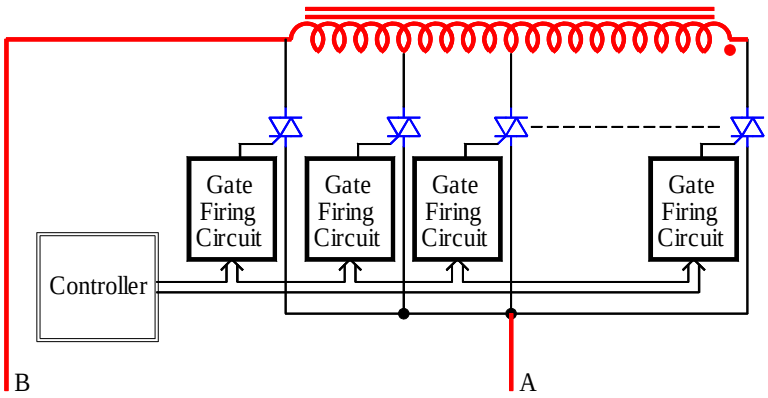


Figure 2-14. Thyristor-controlled load tap changer.

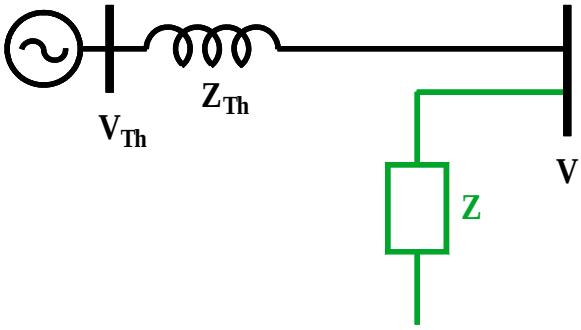


Figure 2-15. Equivalent transmission line with shunt compensation.

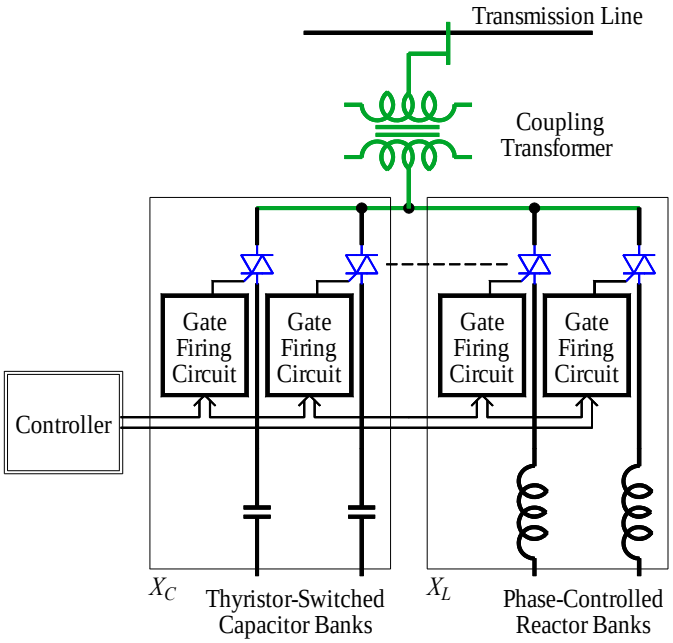


Figure 2-16. Static var compensator.

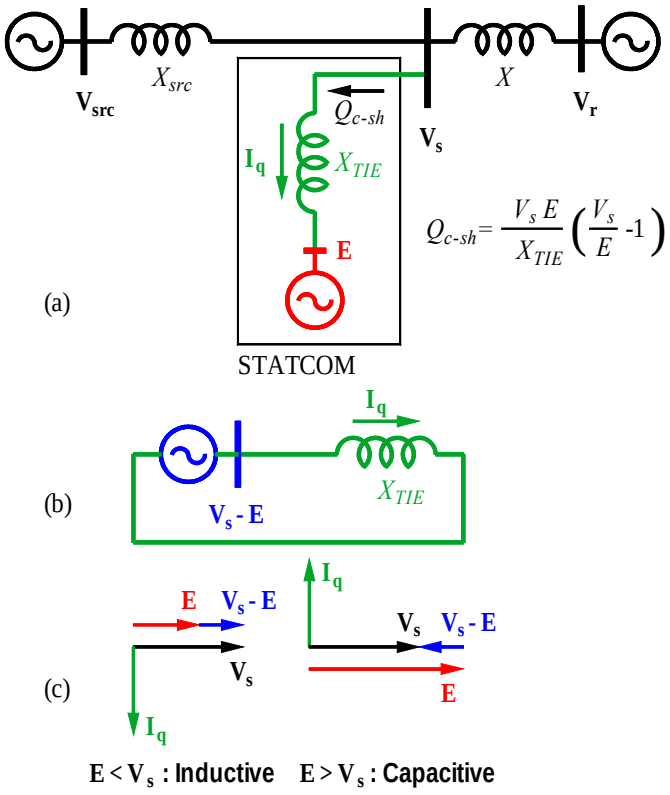


Figure 2-17. Concept of the STATCOM.

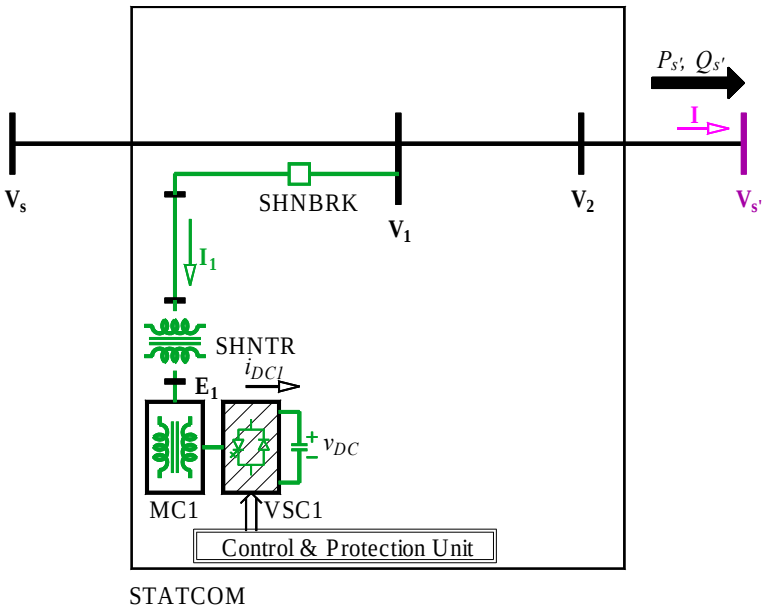


Figure 2-18. Static synchronous compensator (STATCOM).

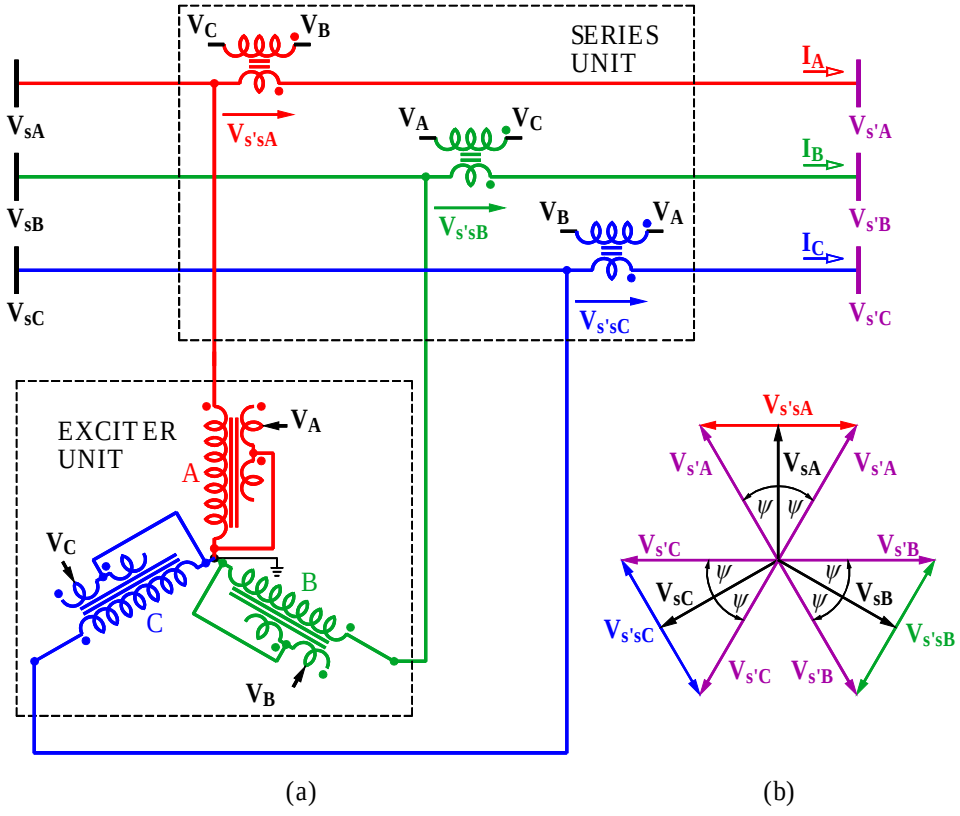


Figure 2-19. (a) Phase angle regulator. (b) Phasor diagram.

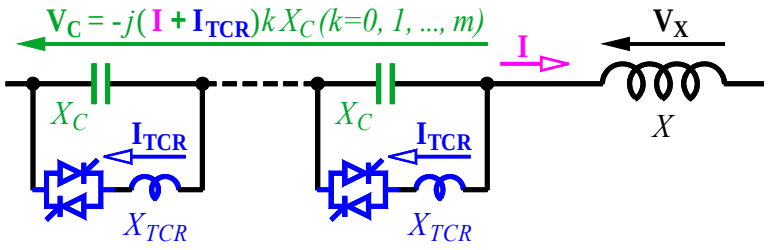


Figure 2-20. Thyristor-controlled series capacitor.

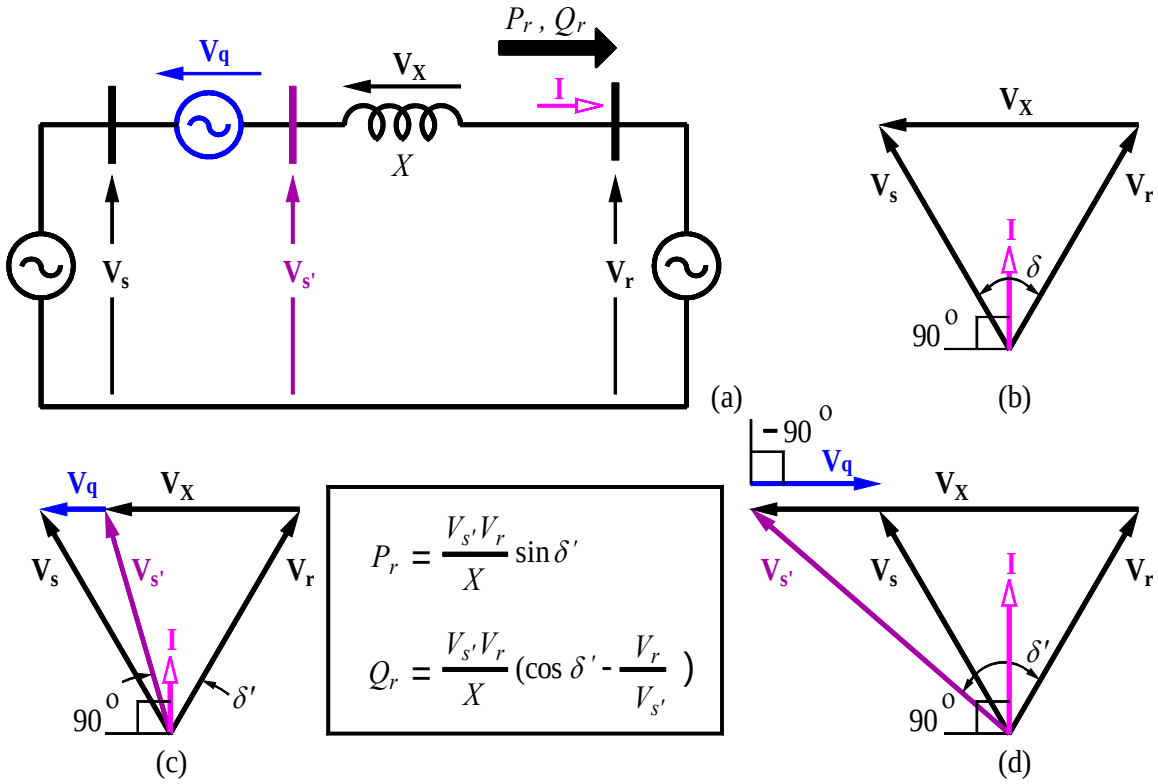


Figure 2-21. (a) Power transmission system and its series reactance emulator with a compensating voltage ($\mathbf{V_q}$) and phasor diagrams for (b) uncompensated line (c) inductively compensated line, and (d) capacitively compensated line.

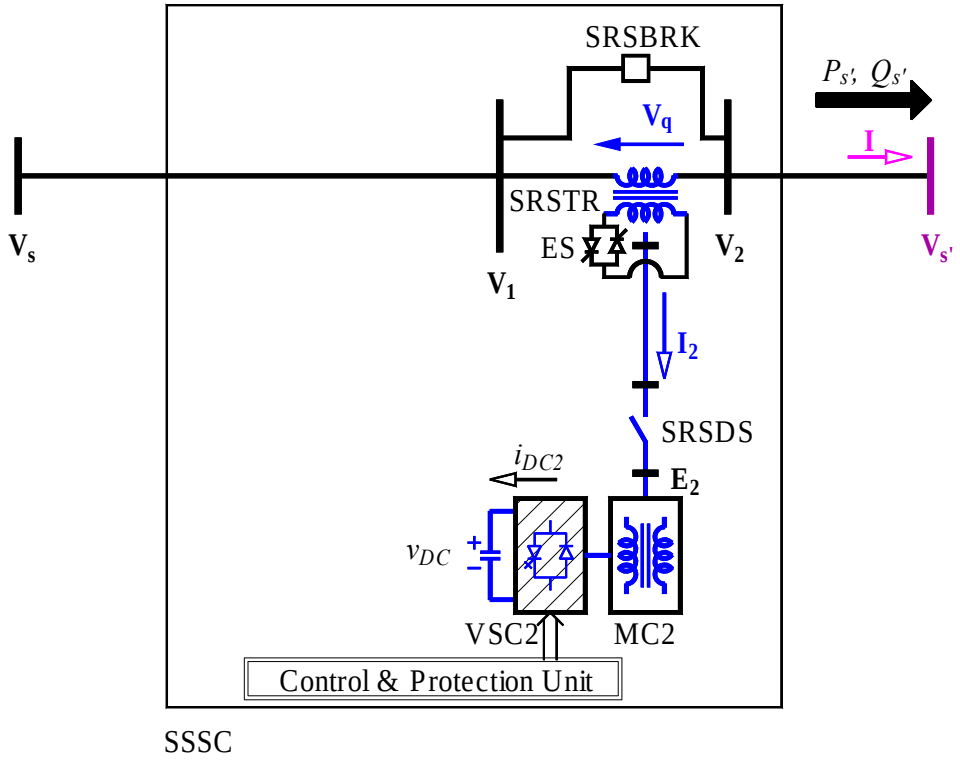


Figure 2-22. Static synchronous series compensator (SSSC).

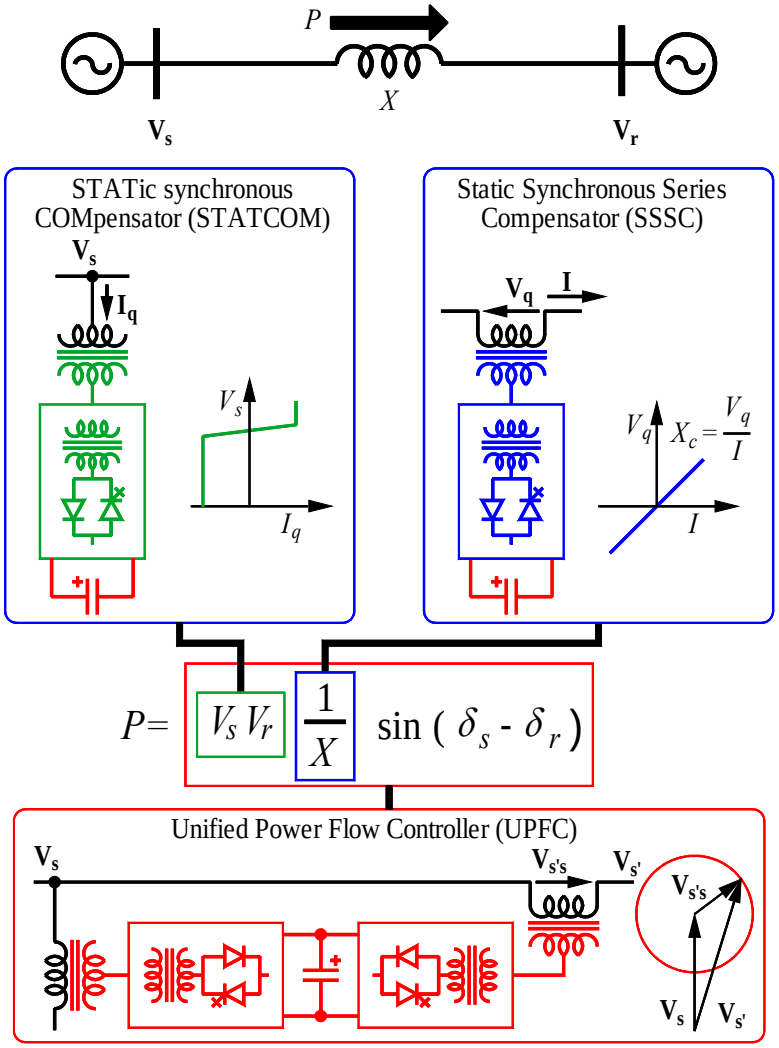


Figure 2-23. The UPFC (with shared DC link) and its building blocks: STATCOM and SSSC.

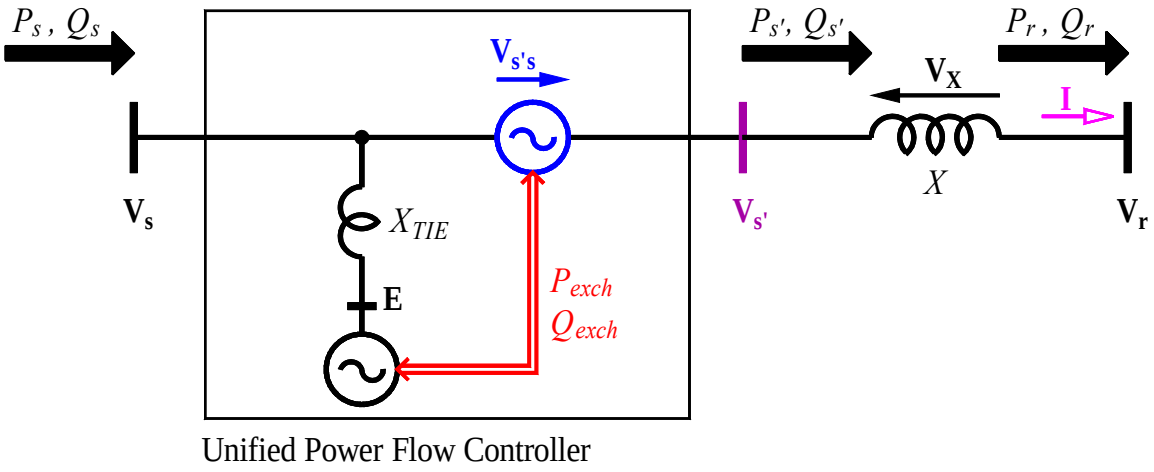


Figure 2-24. Concept of the unified power flow controller.

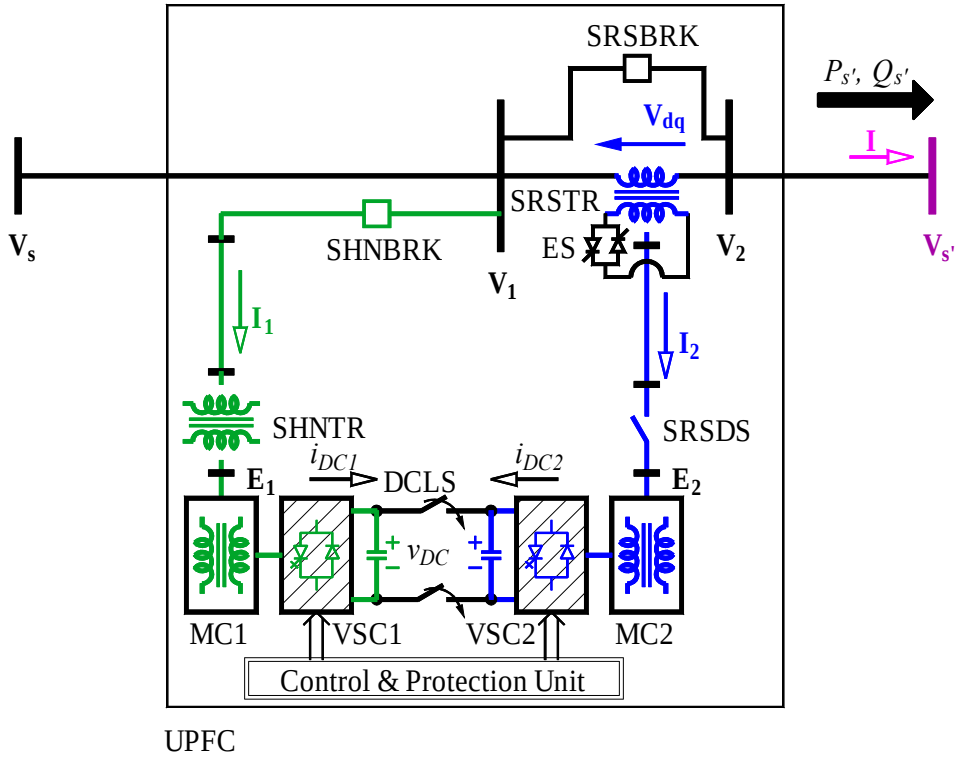


Figure 2-25. Unified power flow controller.

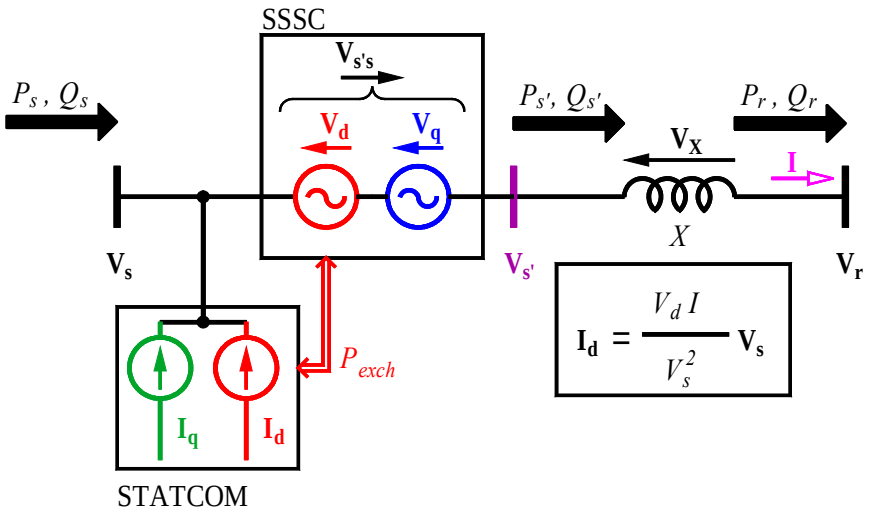


Figure 2-26. Basic UPFC model.

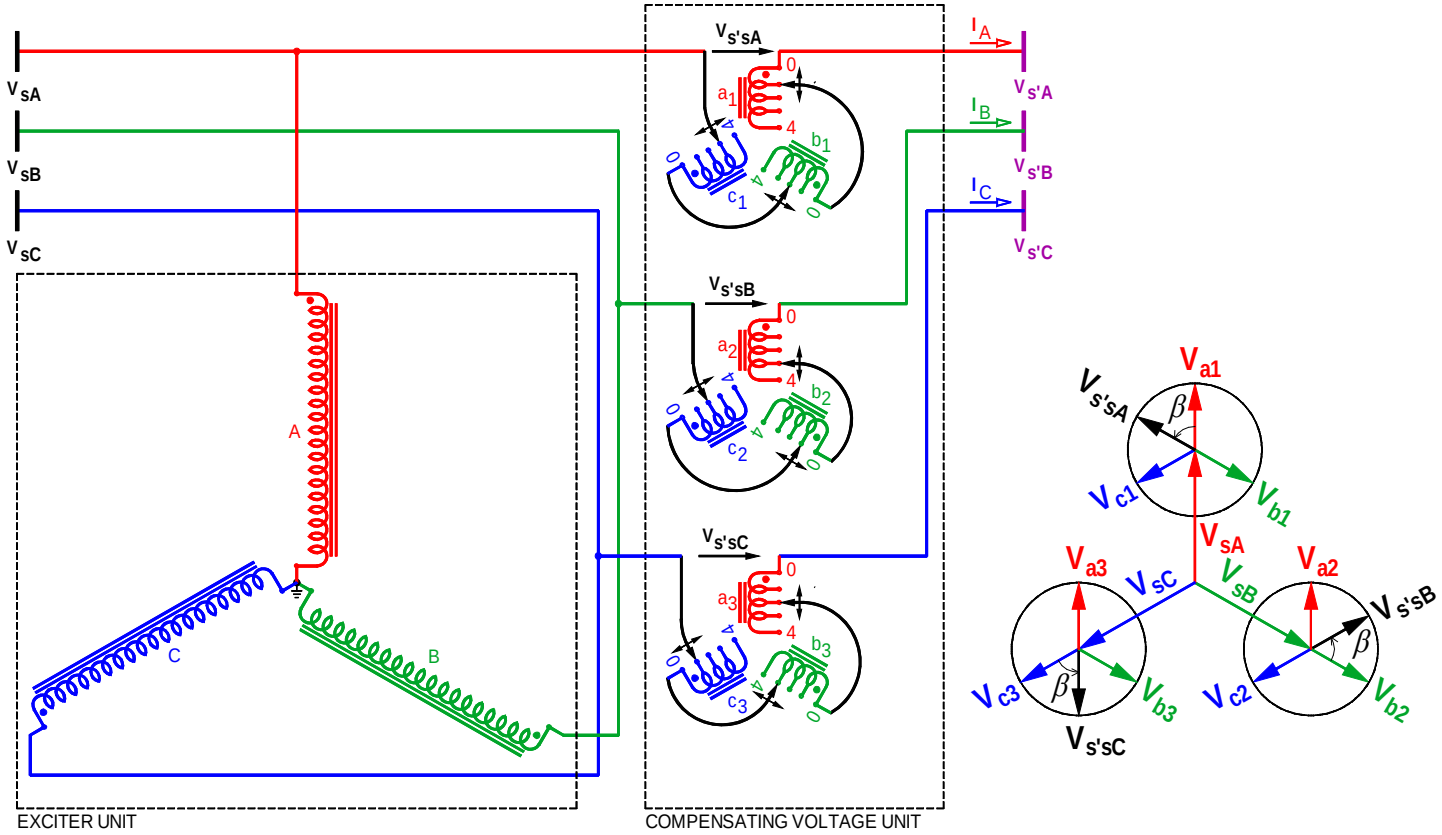


Figure 2-27. Sen transformer.

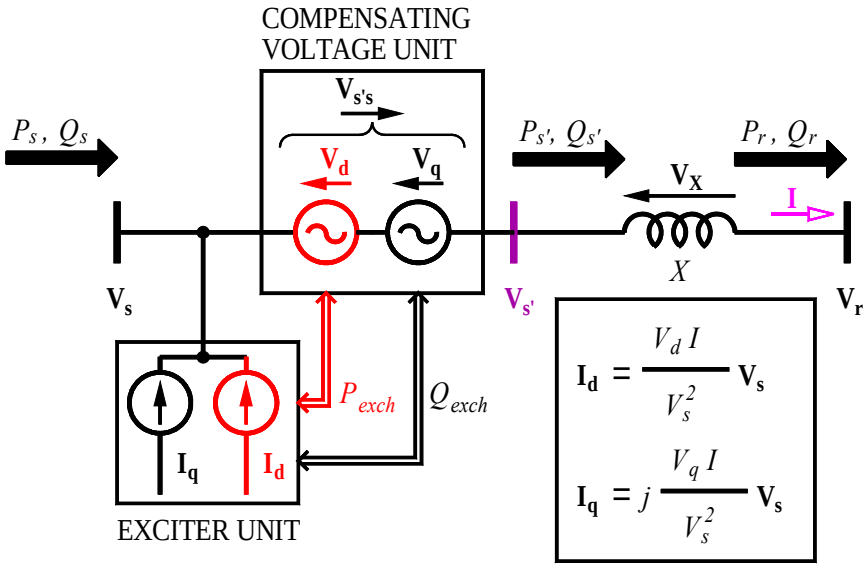


Figure 2-28. Basic ST model.

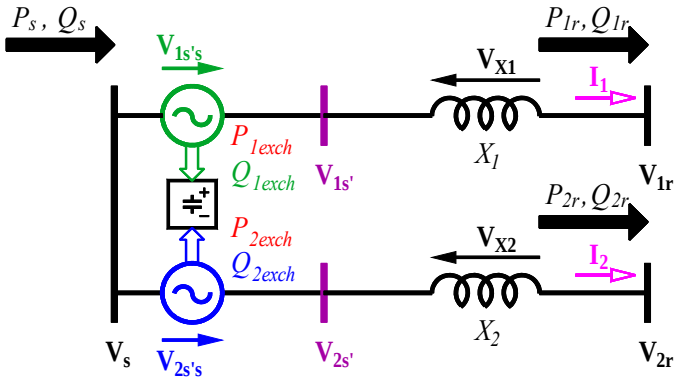


Figure 2-29. Basic BTB-SSSC.

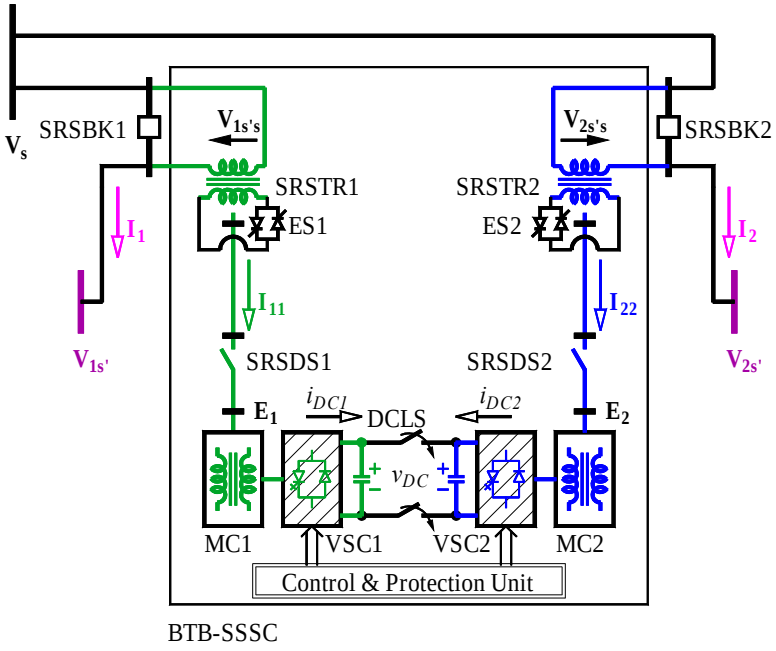


Figure 2-30. Implementation of a basic BTB-SSSC.

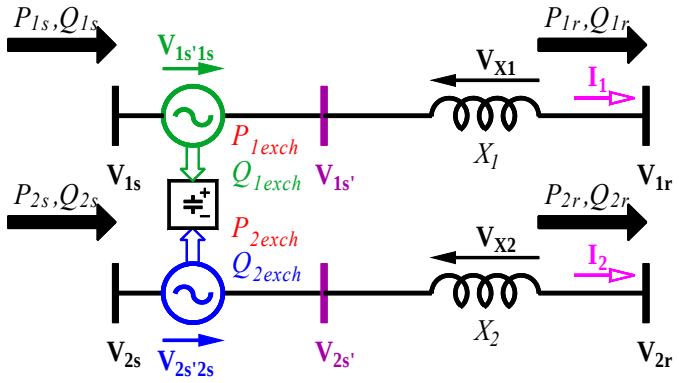


Figure 2-31. BTB-SSSC scheme as an asynchronous tie.

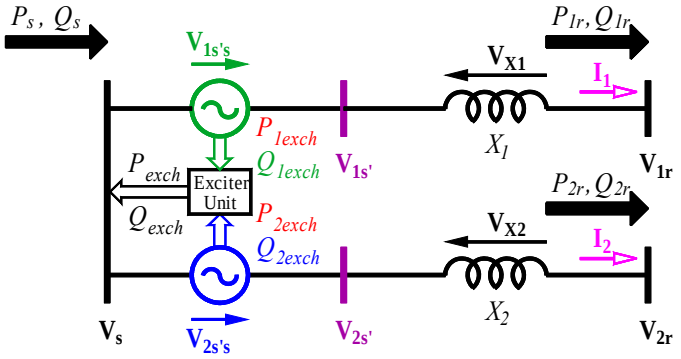


Figure 2-32. Implementation of a basic MST.

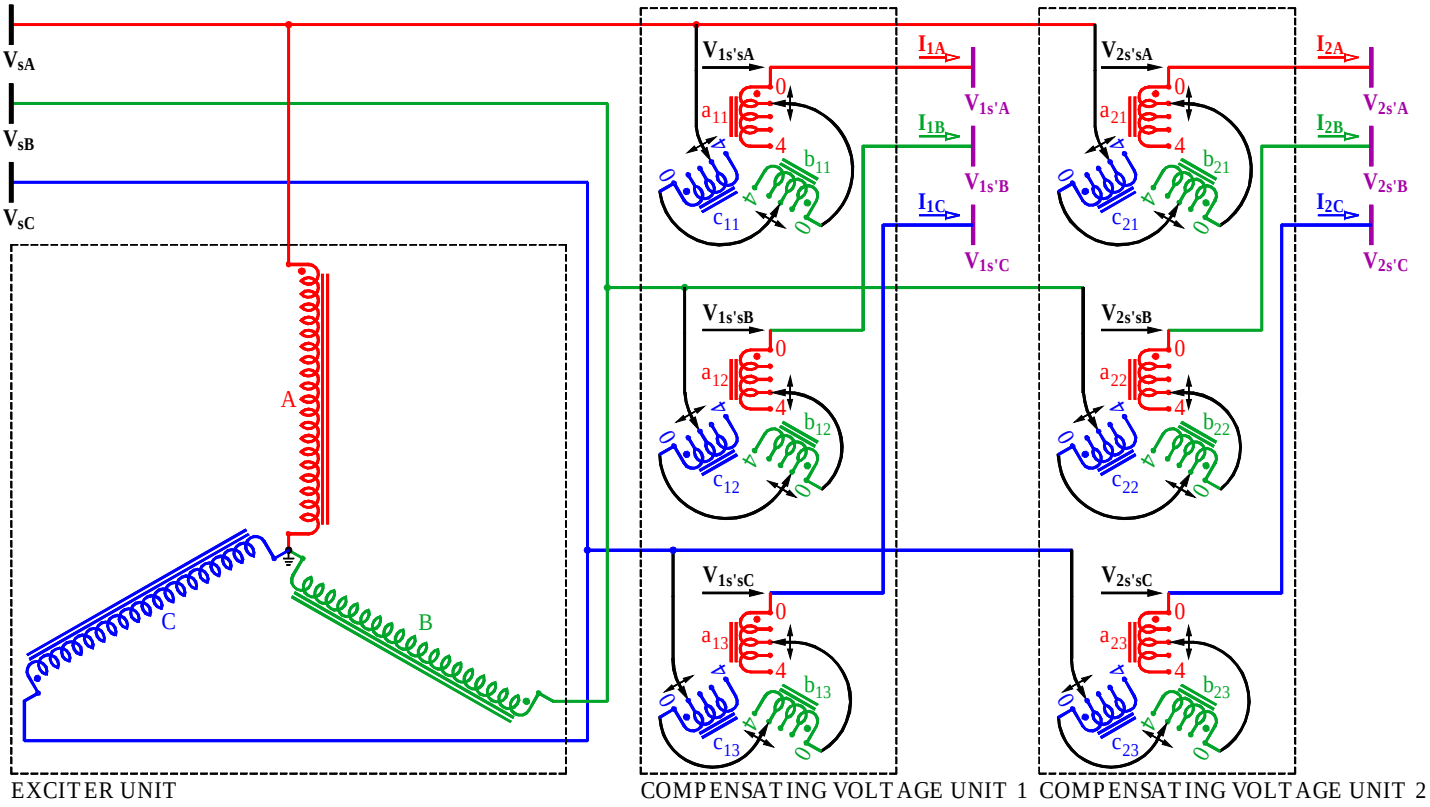


Figure 2-33. Multiline Sen transformer.

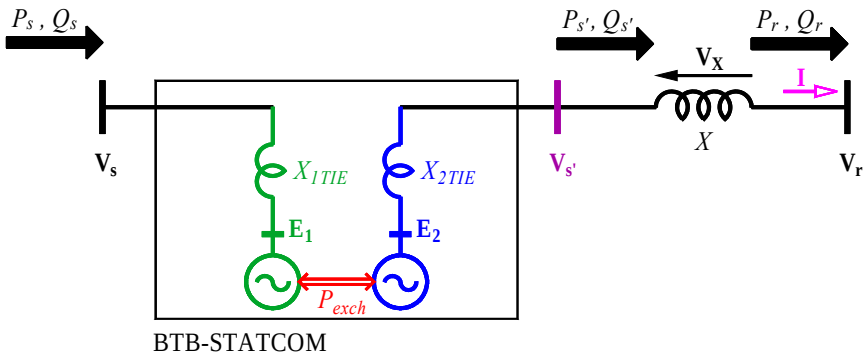


Figure 2-34. Concept of a back-to-back STATCOM.

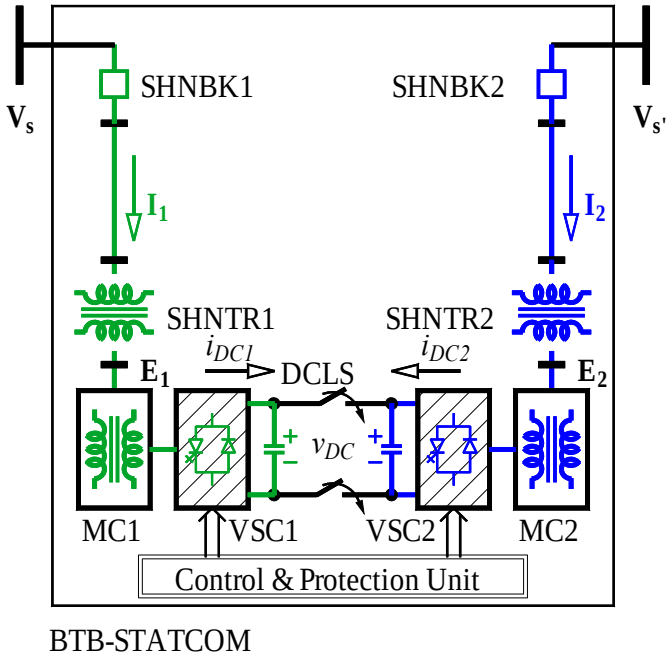


Figure 2-35. Back-to-back STATCOM.

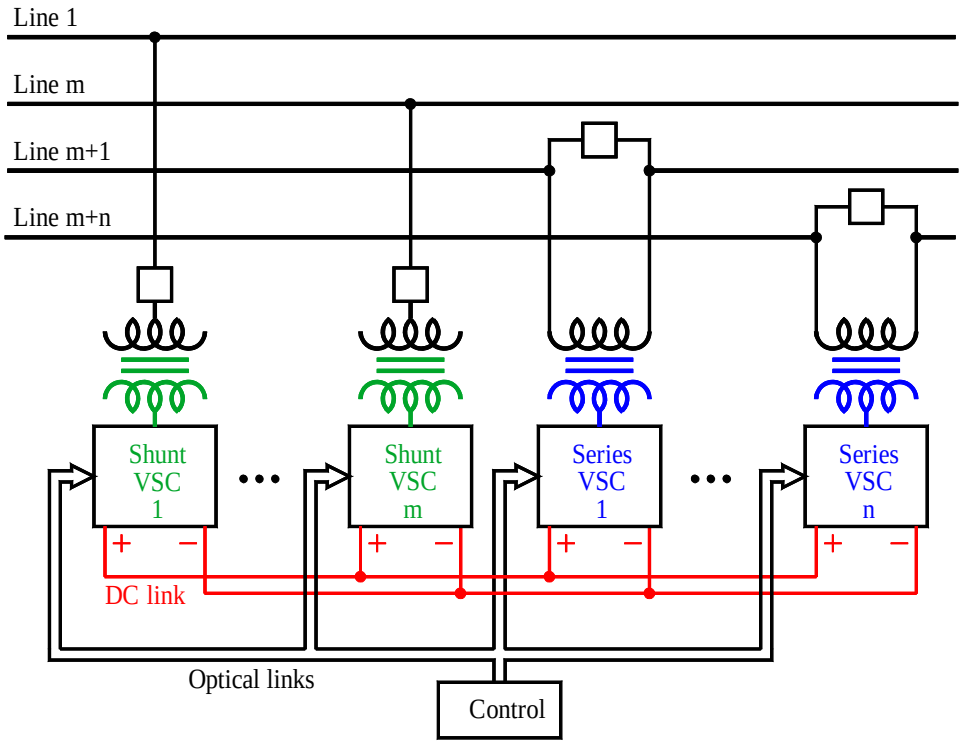


Figure 2-36. Generalized power flow controller.

CHAPTER 3

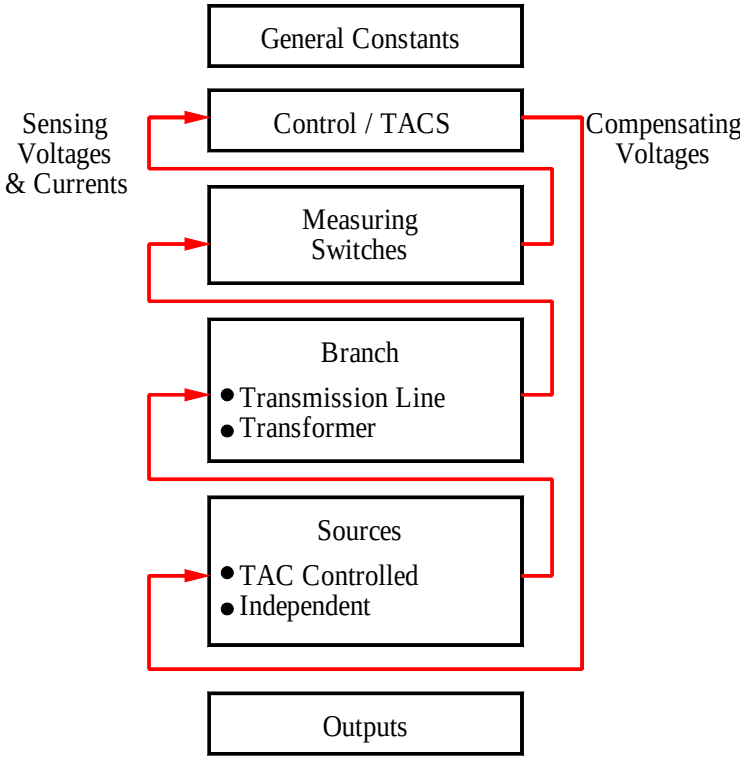


Figure 3-1. EMTP modeling structure.

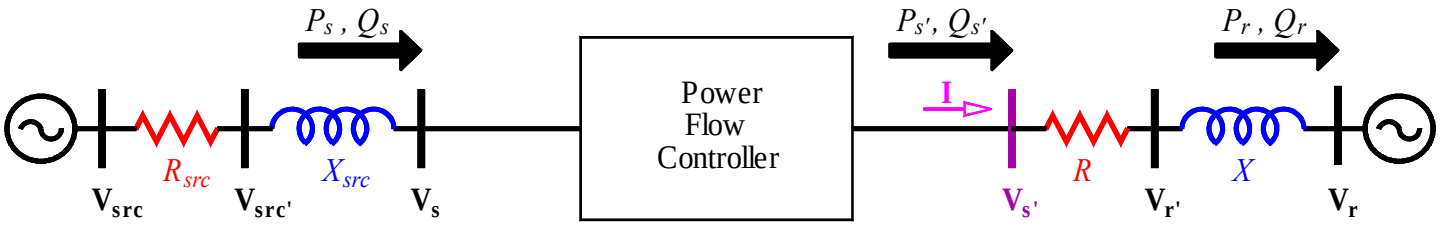


Figure 3-2. Two-bus network model.

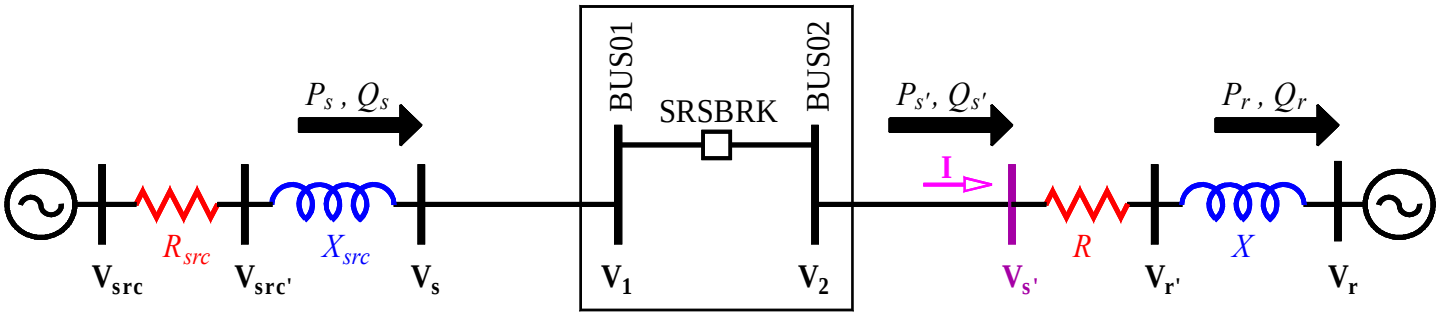


Figure 3-3. Two-bus network model in EMTP.

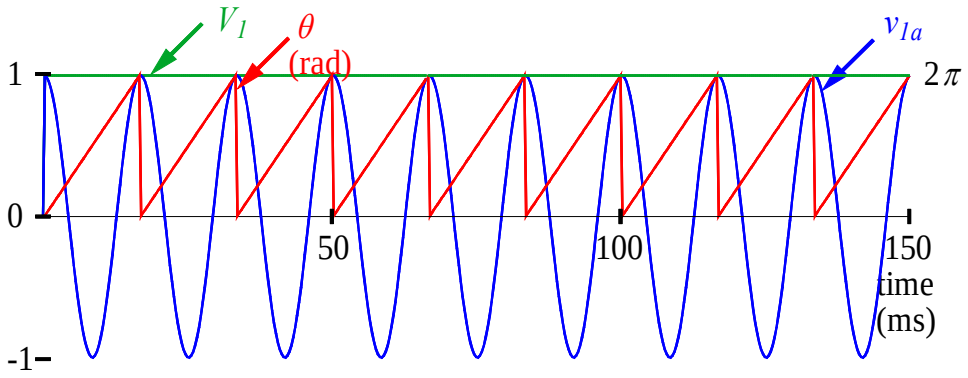


Figure 3-4. Phase *a* of line voltage (v_{1a}) at BUS01, its magnitude (V_1), and the PLL angle (θ).

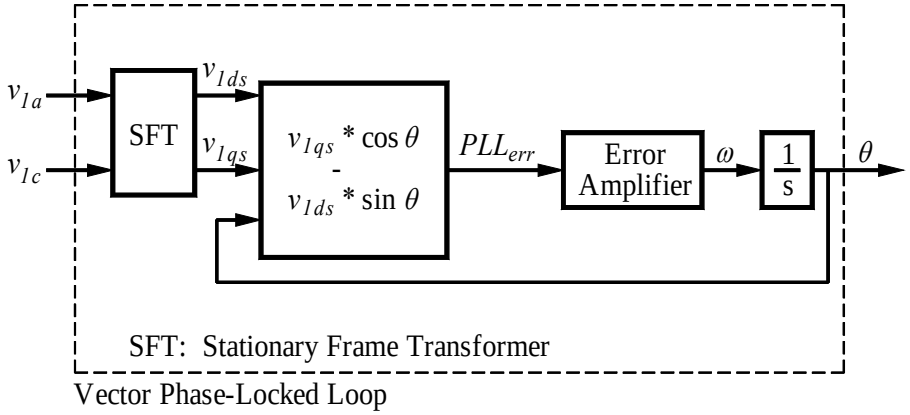


Figure 3-5. Block diagram of a vector PLL.

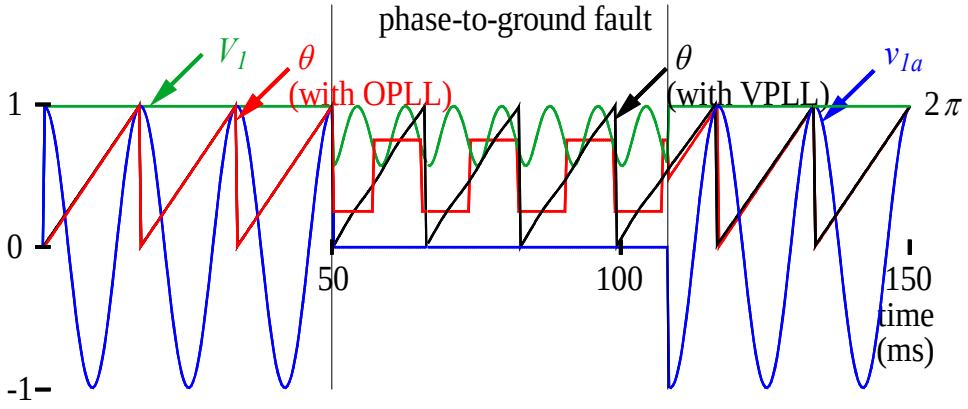


Figure 3-6. Phase *a* of line voltage (v_{1a}) at BUS01, its magnitude (V_1), and the PLL angle (θ) with and without a phase-to-ground fault.

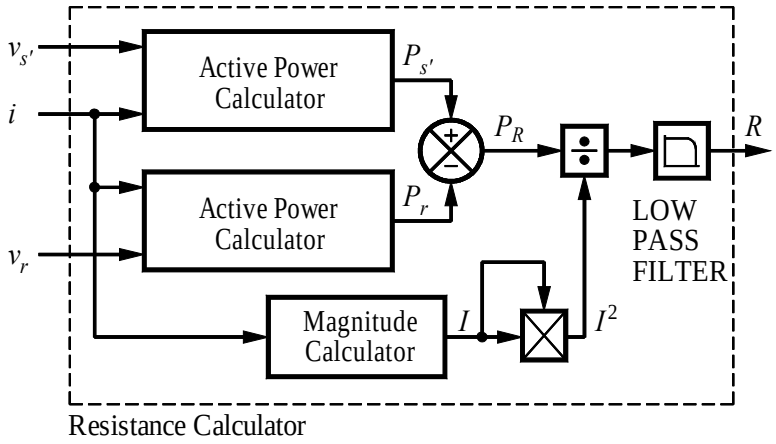


Figure 3-7. Block diagram for a steady-state resistance calculator.

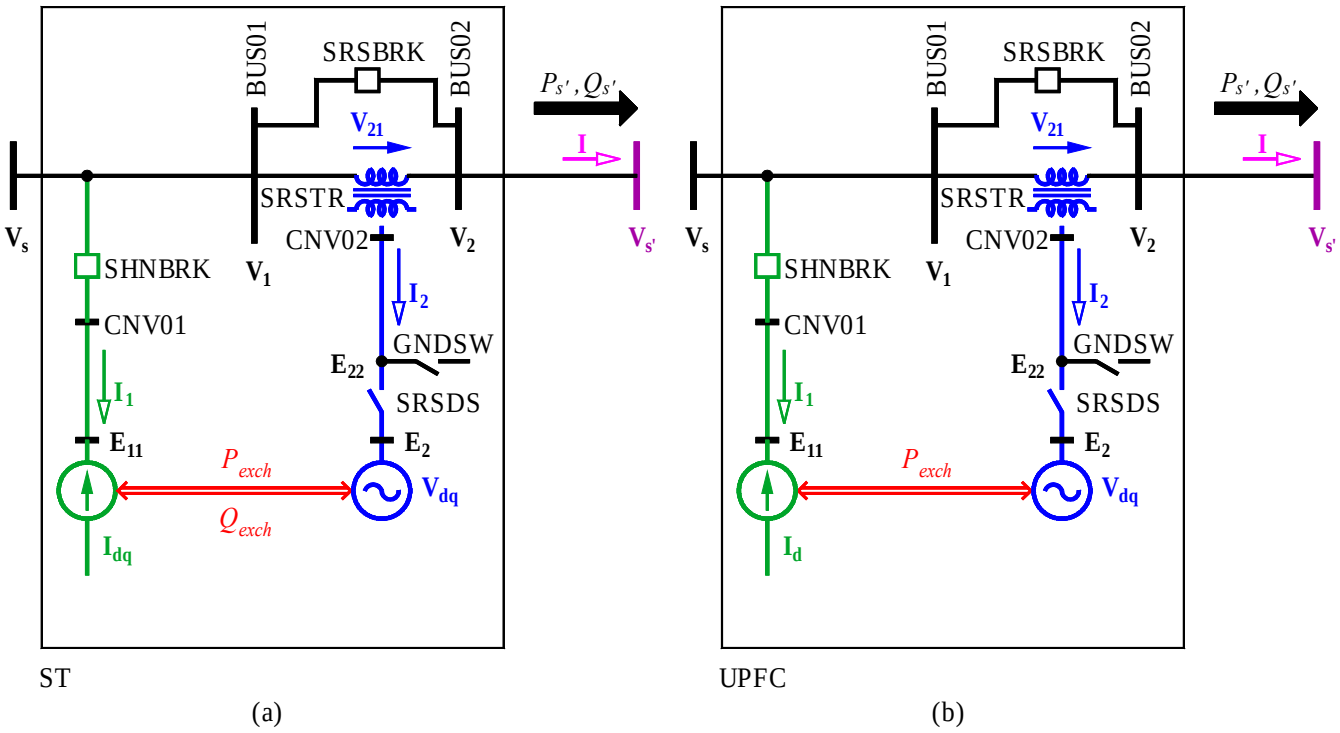


Figure 3-8. Simulation models of the (a) ST and (b) UPFC.

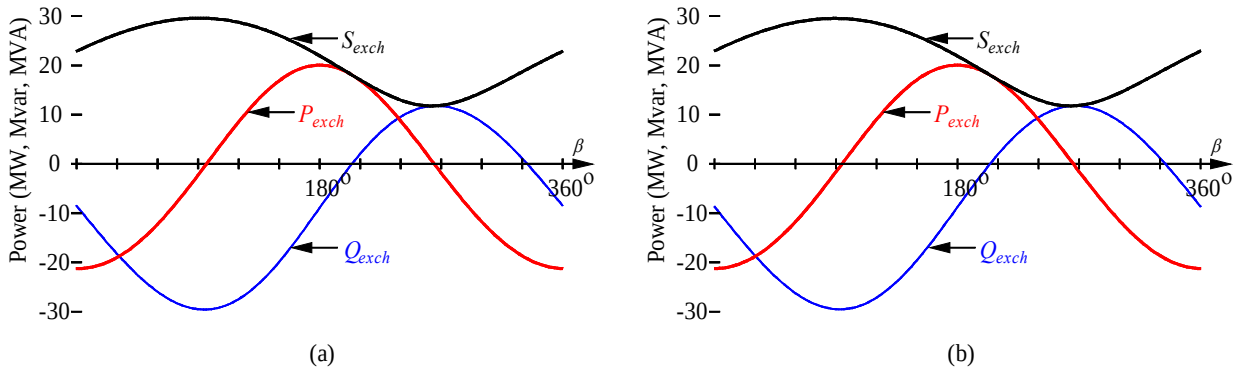


Figure 3-9. Variations of exchanged powers between the transmission line and the series unit of the (a) ST and (b) UPFC.

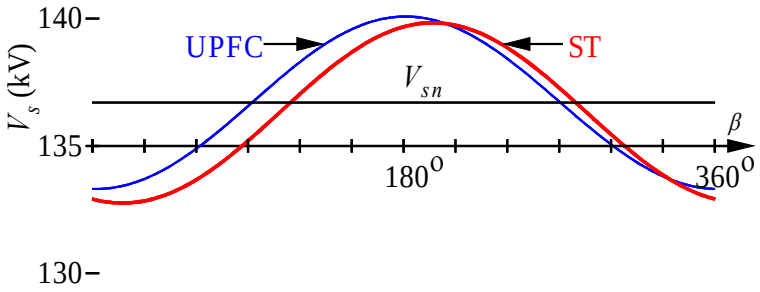


Figure 3-10. Variations of bus voltage with the operation of the ST and UPFC.

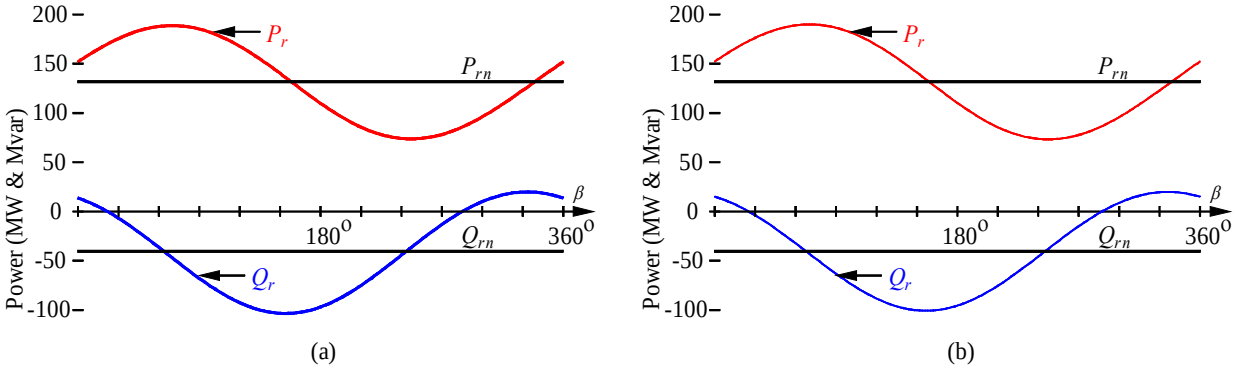


Figure 3-11. Variations of receiving-end power flow with the operation of the (a) ST and (b) UPFC.

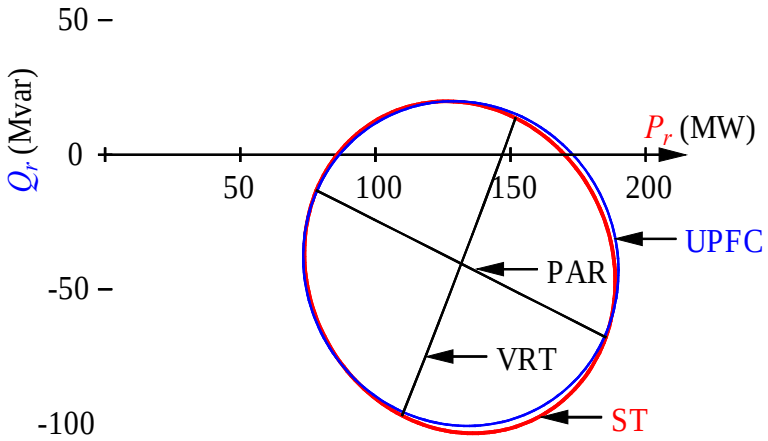


Figure 3-12. Comparison of active and reactive power flows at the receiving end of the transmission line with the operation of the VRT, PAR, UPFC, and ST.

CHAPTER 4

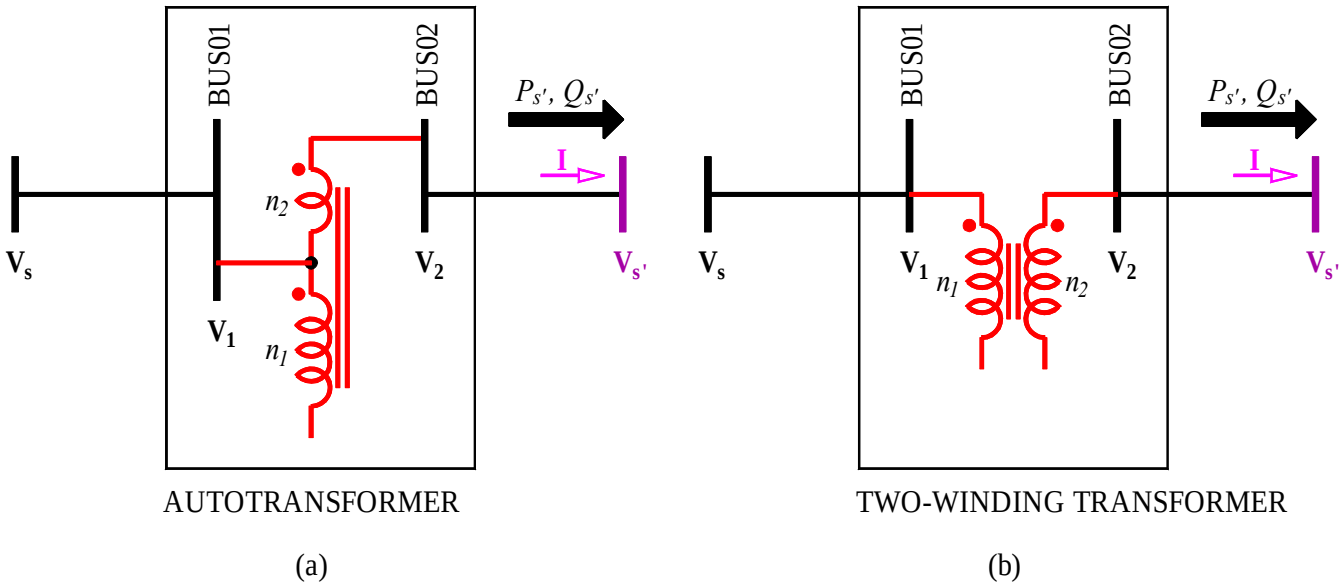


Figure 4-1. (a) Autotransformer. (b) Two-winding transformer.

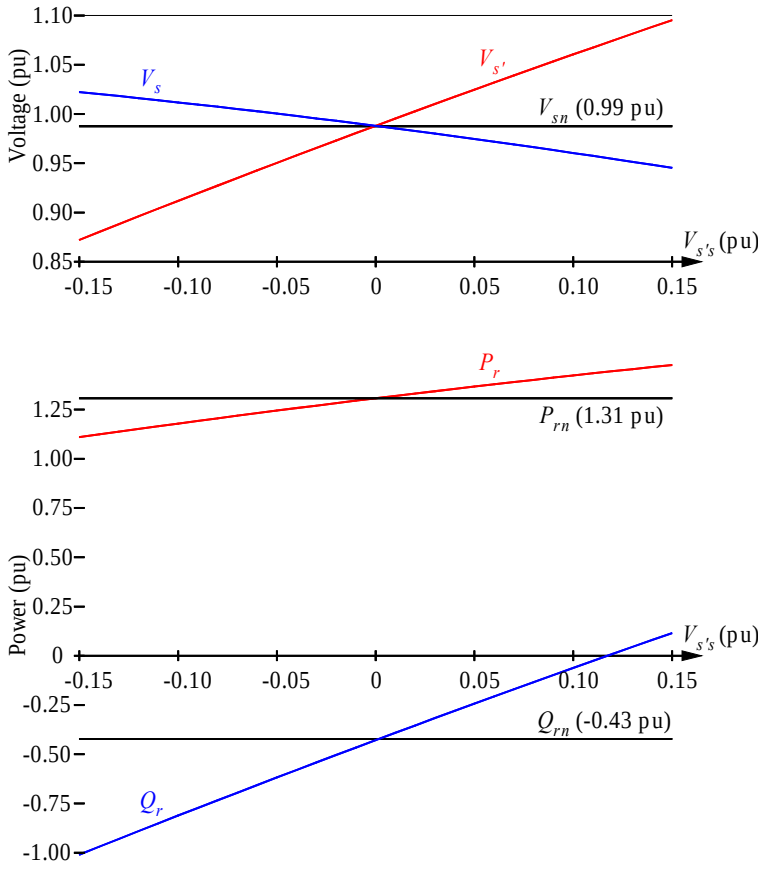


Figure 4-2. Ranges of voltages at the sending and modified sending ends and active and reactive power flows at the receiving end when an autotransformer is implemented with a series-connected compensating voltage through a coupling transformer with no leakage impedance.

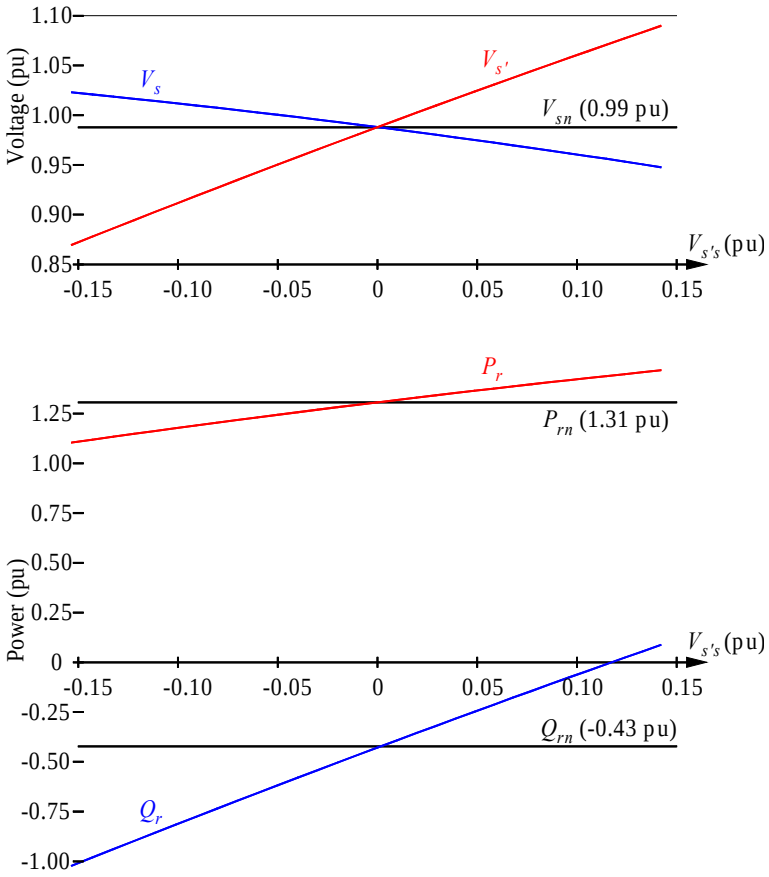


Figure 4-3. Ranges of voltages at the sending and modified sending ends and active and reactive power flows at the receiving end when an autotransformer is implemented with a series-connected compensating voltage through a coupling transformer with no leakage impedance and the series-connected compensating voltage is a multiplier of the input voltage.

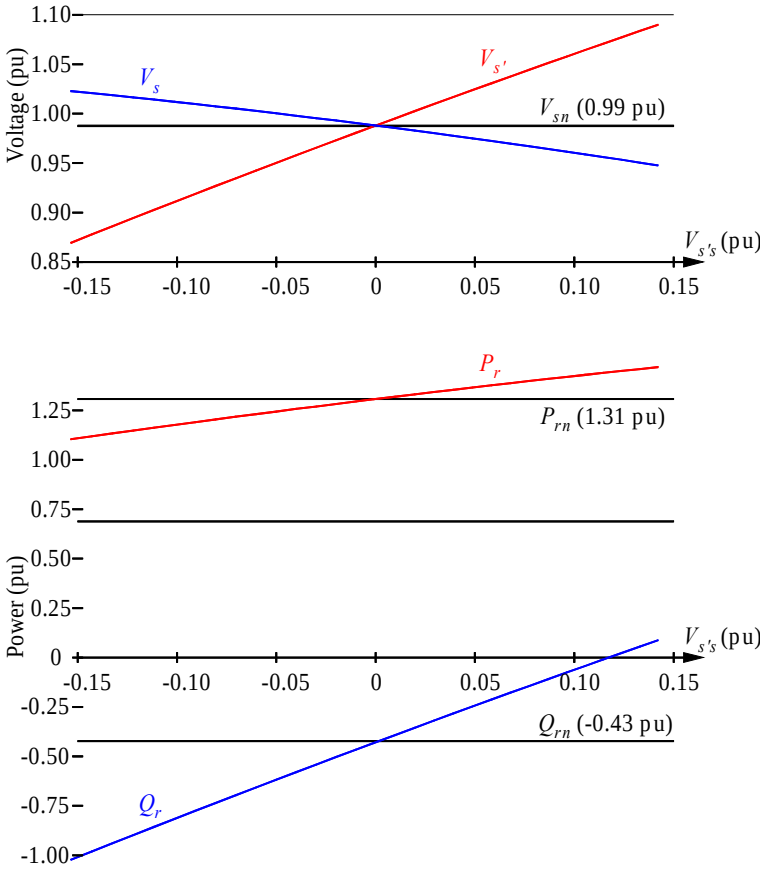


Figure 4-4. Ranges of voltages at the sending and modified sending ends and active and reactive power flows at the receiving end with an actual autotransformer with no leakage impedance.

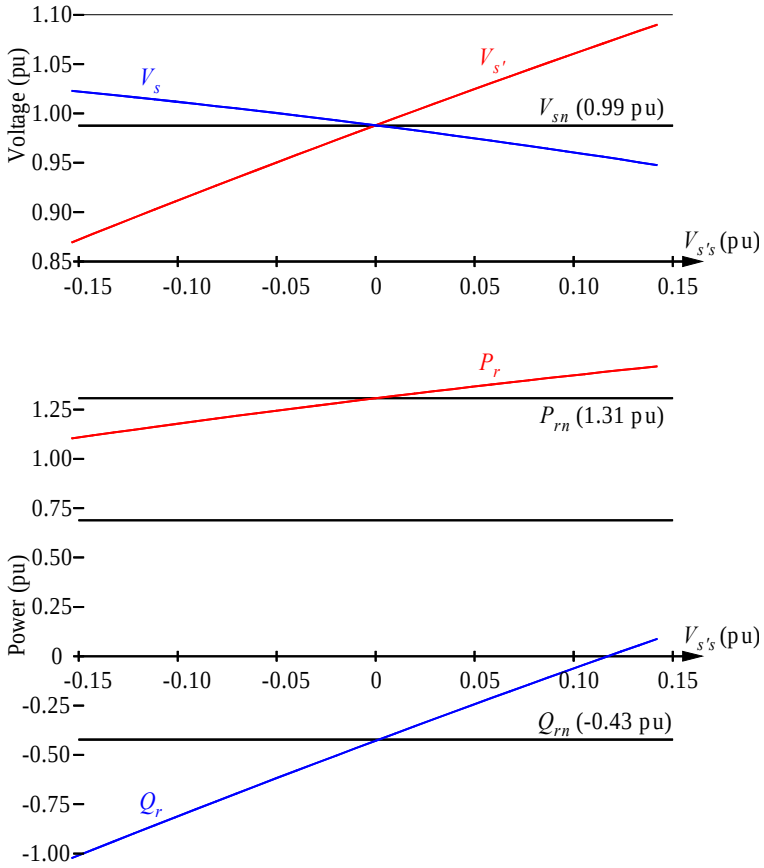


Figure 4-5. Ranges of voltages at the sending and modified sending ends and active and reactive power flows at the receiving end with an actual two-winding transformer with no leakage impedance.

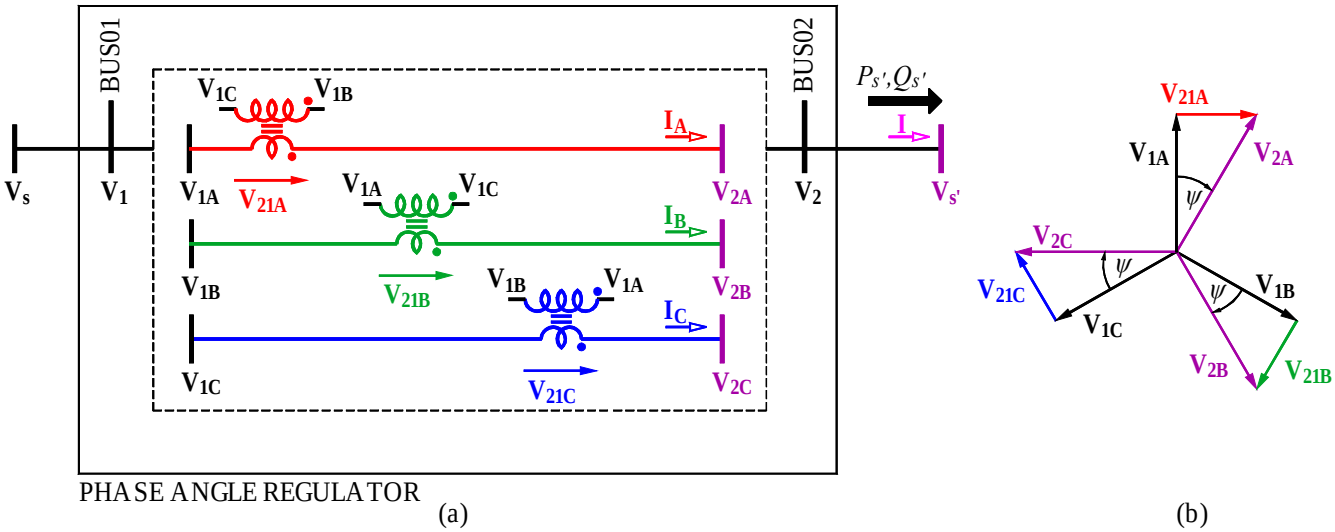


Figure 4-6. Phase angle regulator.

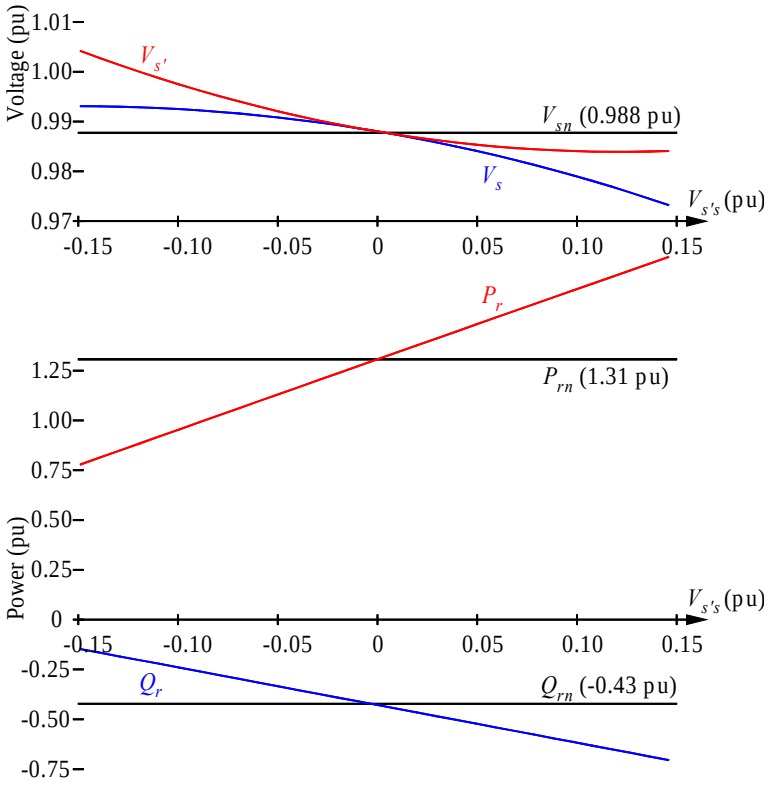


Figure 4-7. Ranges of voltages at the sending and modified sending ends and active and reactive power flows at the receiving end with a phase angle regulator with no leakage impedance.

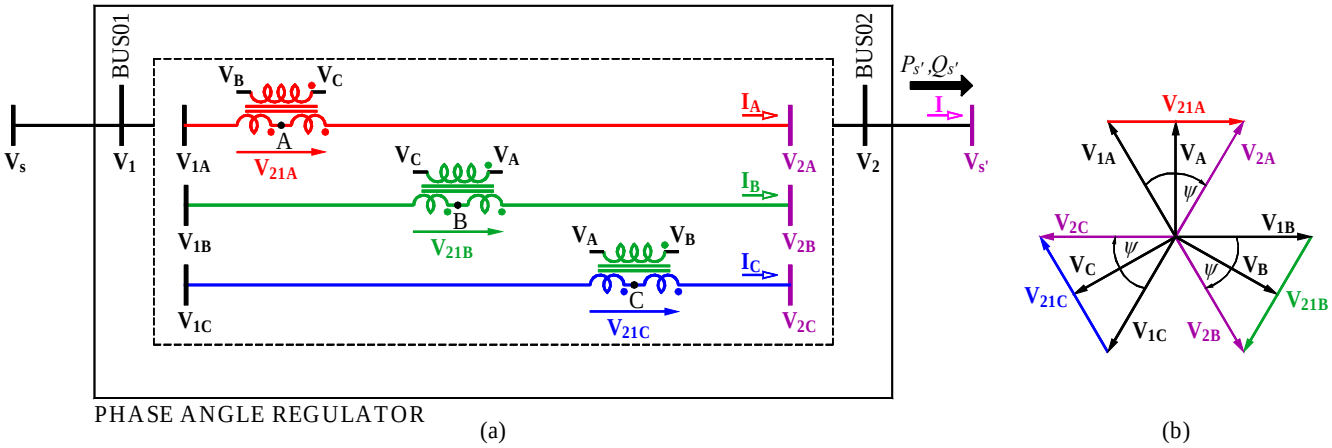


Figure 4-8. True phase angle regulator configuration.

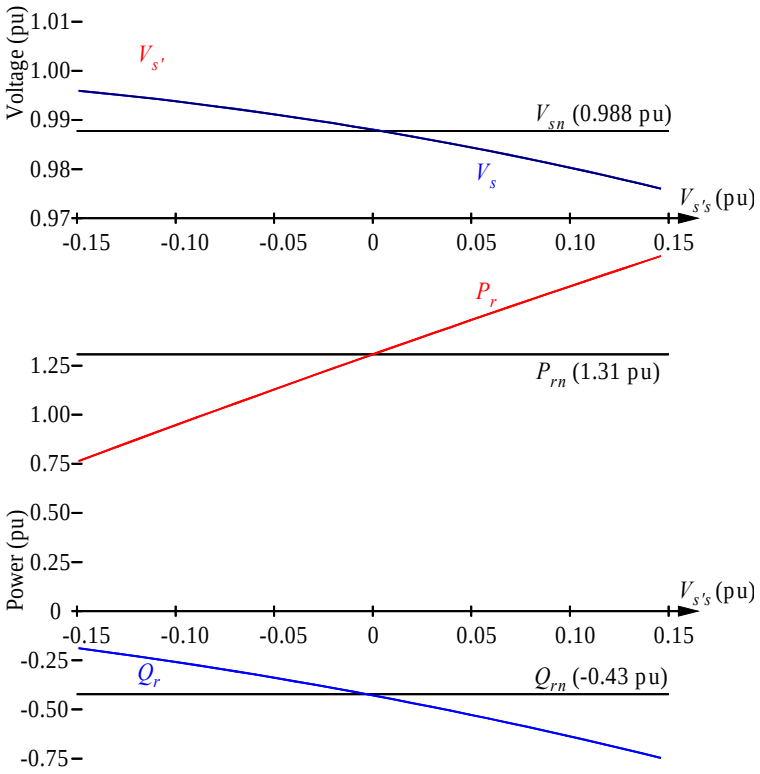


Figure 4-9. Ranges of voltages at the sending and modified sending ends and active and reactive power flows at the receiving end with a phase angle regulator with no leakage impedance and the Δ–connected primary windings are excited from the center-tapped series compensating windings.

CHAPTER 5

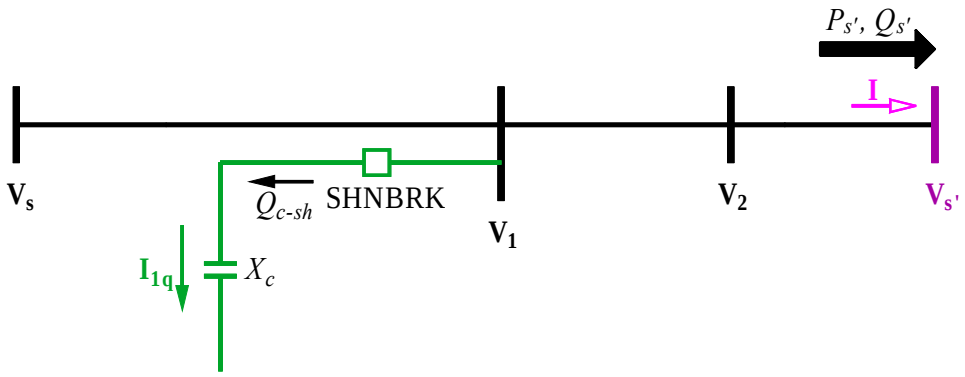


Figure 5-1. Shunt-connected mechanically switched capacitor.

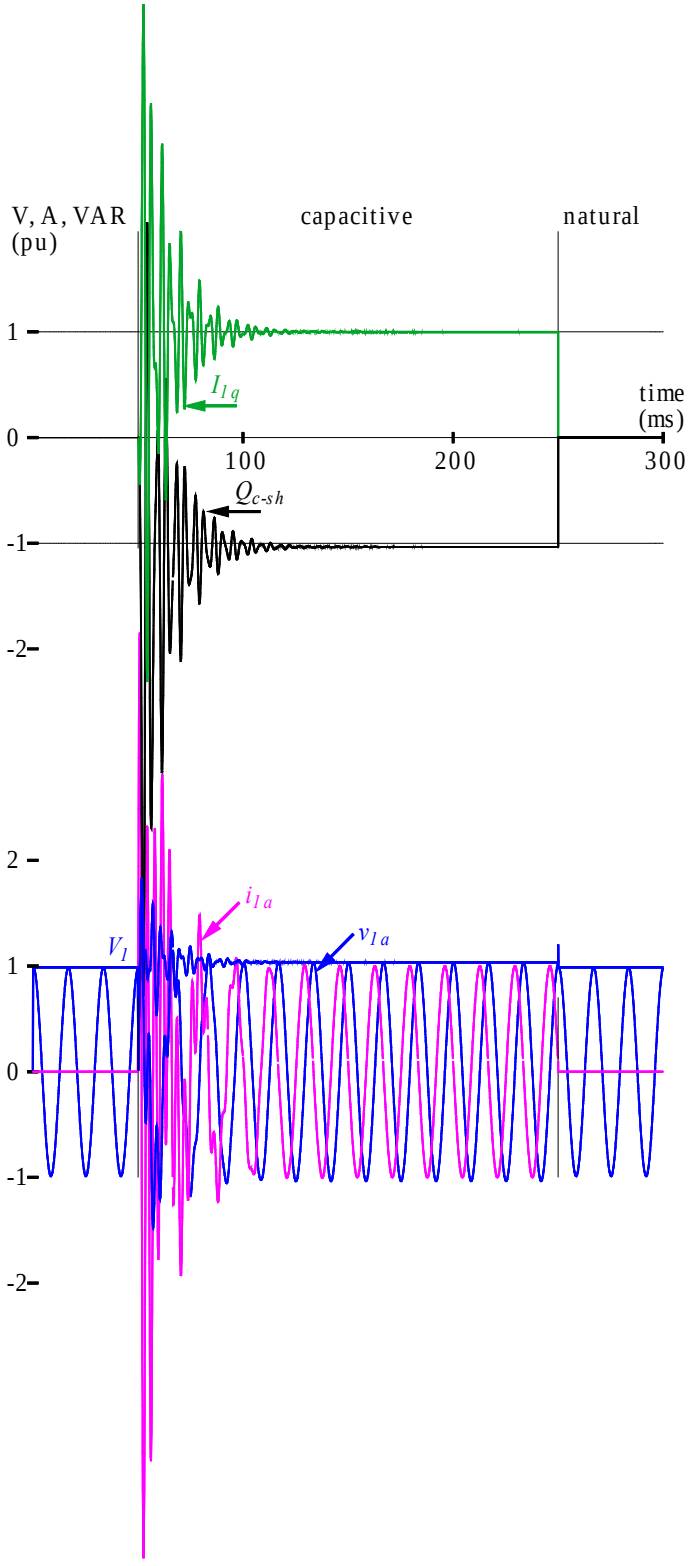


Figure 5-2. Exchanged reactive power and the resulting voltages and currents due to a shunt-connected mechanically switched capacitor to a transmission line.

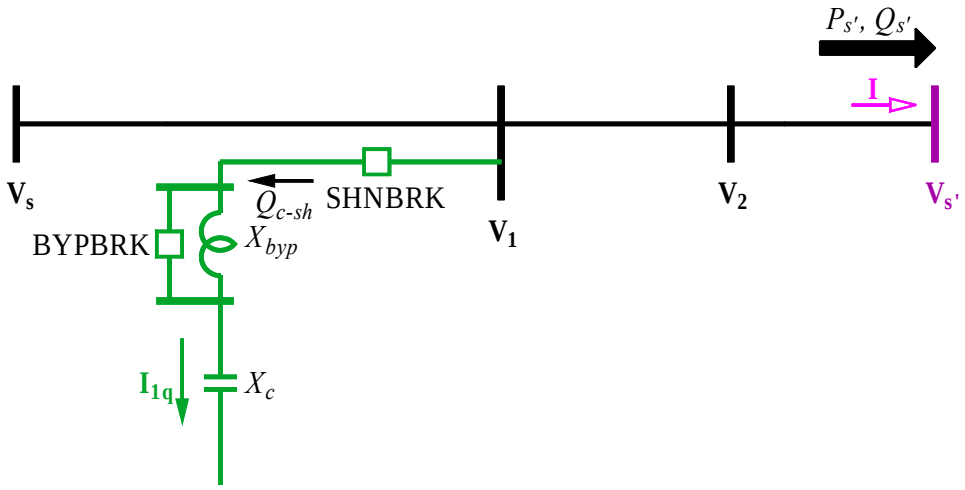


Figure 5-3. Shunt-connected mechanically switched capacitor with series reactor.

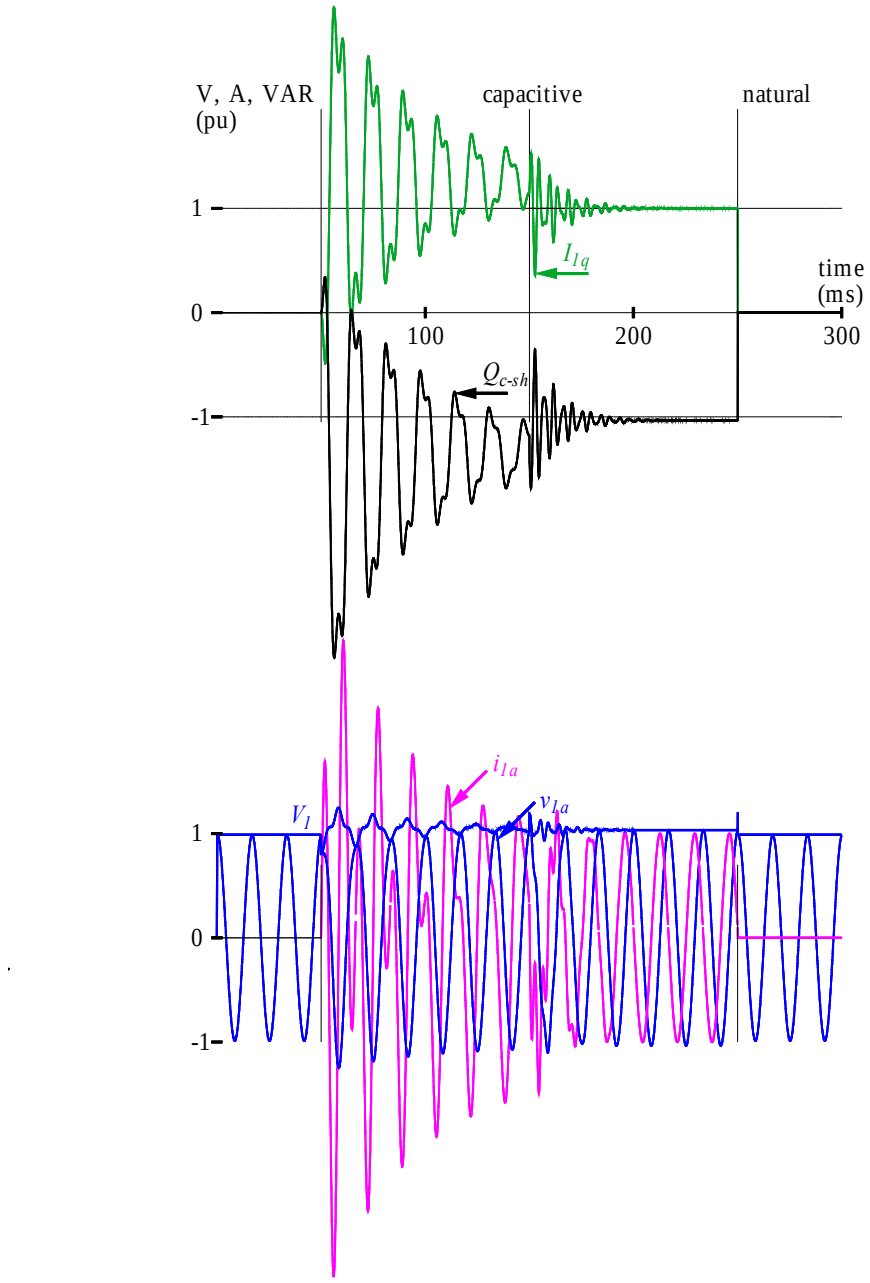


Figure 5-4. Exchanged reactive power and the resulting voltages and currents due to a shunt-connected mechanically switched capacitor (with a series reactor) to a transmission line.

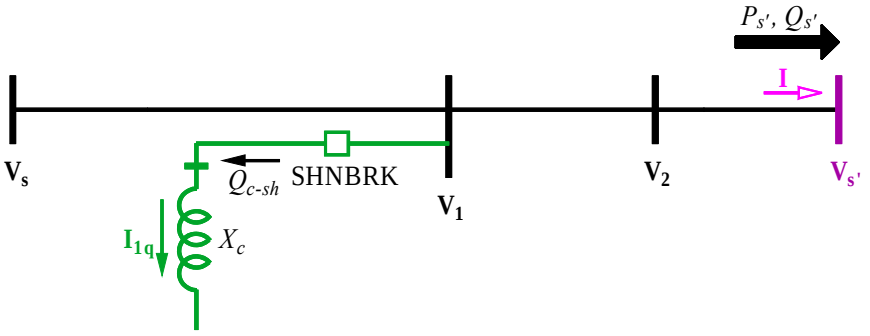


Figure 5-5. Shunt-connected mechanically switched reactor.

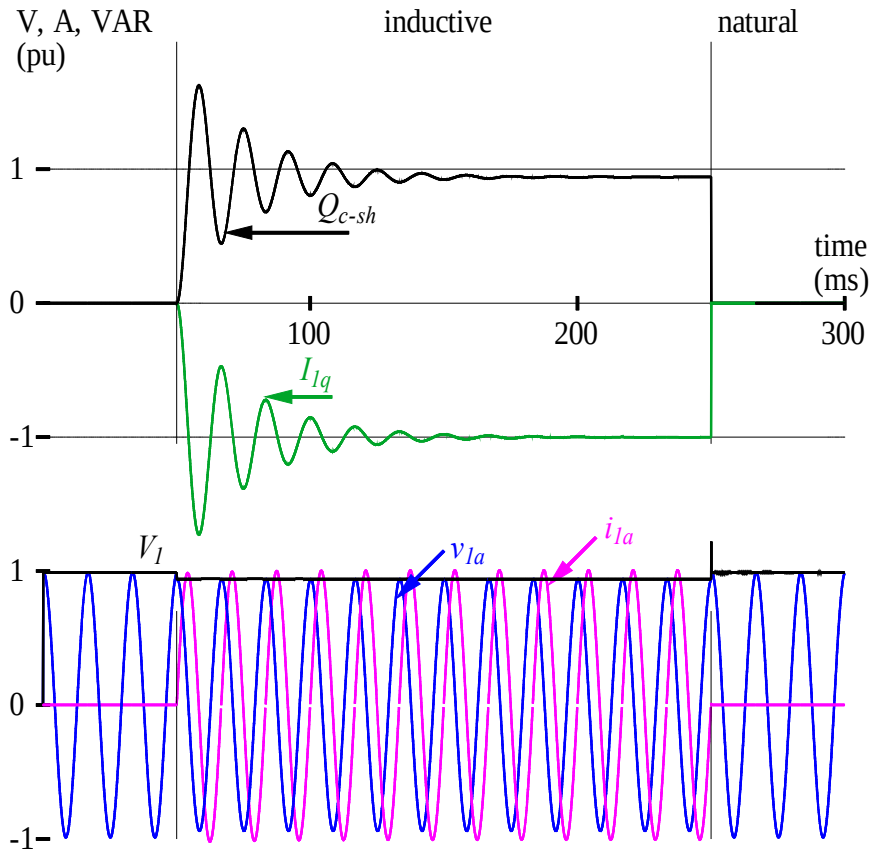


Figure 5-6. Exchanged reactive power and the resulting voltages and currents due to a shunt-connected reactor to a transmission line.

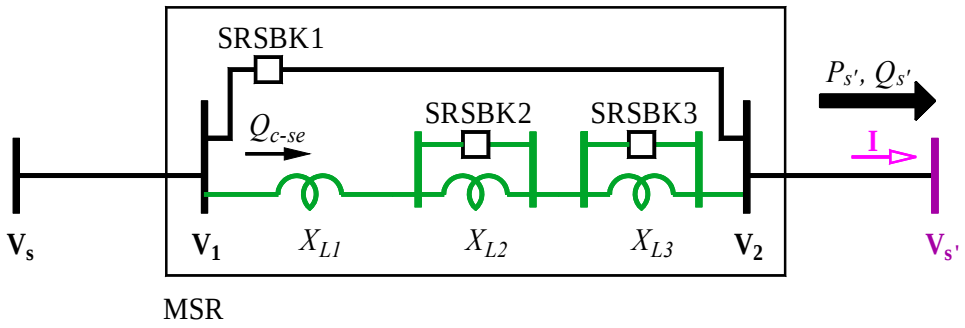


Figure 5-7. Series-connected mechanically switched reactor.

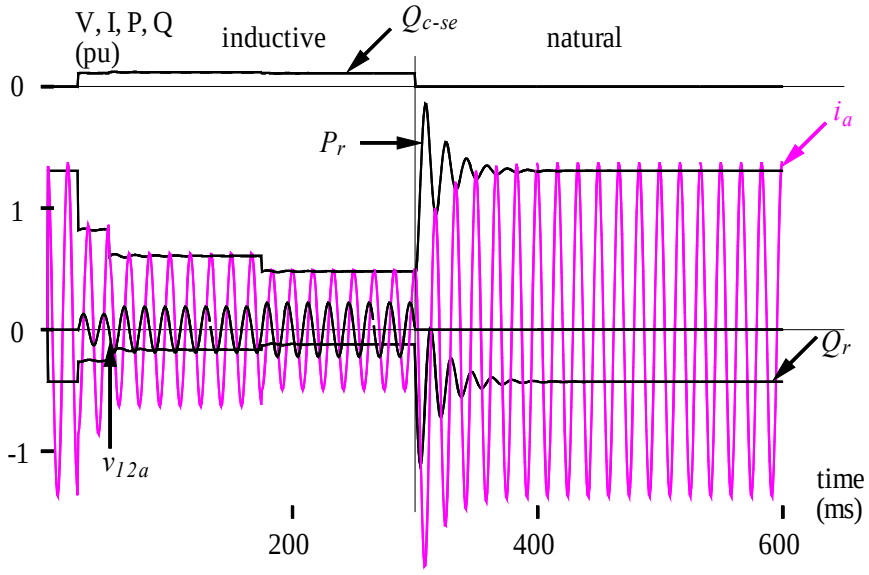


Figure 5-8. Effect of a series-connected reactor in the transmission line.

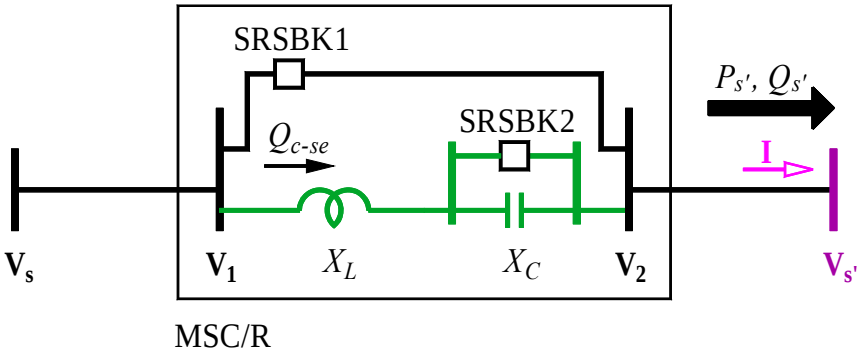


Figure 5-9. Series-connected mechanically switched capacitor with reactor.

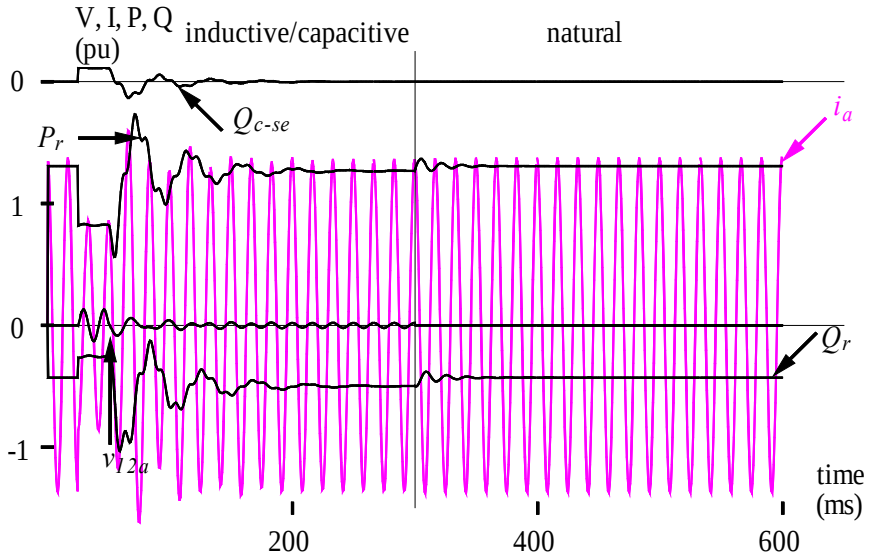


Figure 5-10. Effect of a series-connected reactor/capacitor in the transmission line.

CHAPTER 6

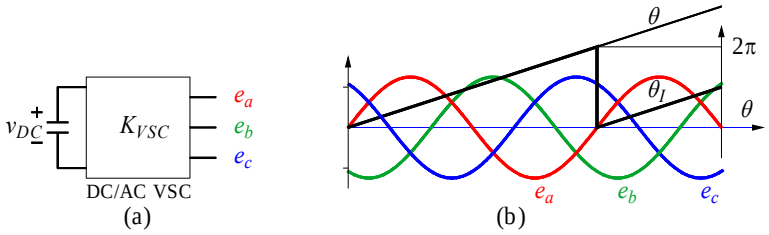


Figure 6-1. Generation of a three-phase ideal VSC voltage.

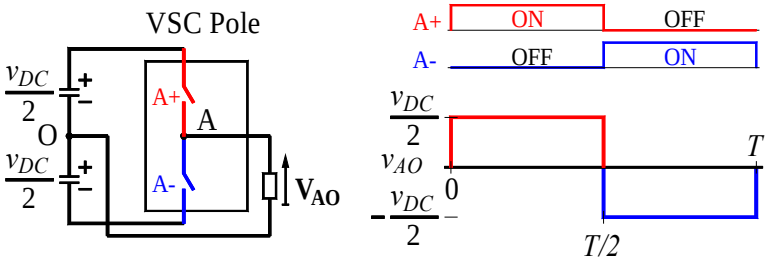


Figure 6-2. VSC pole and its output voltage.

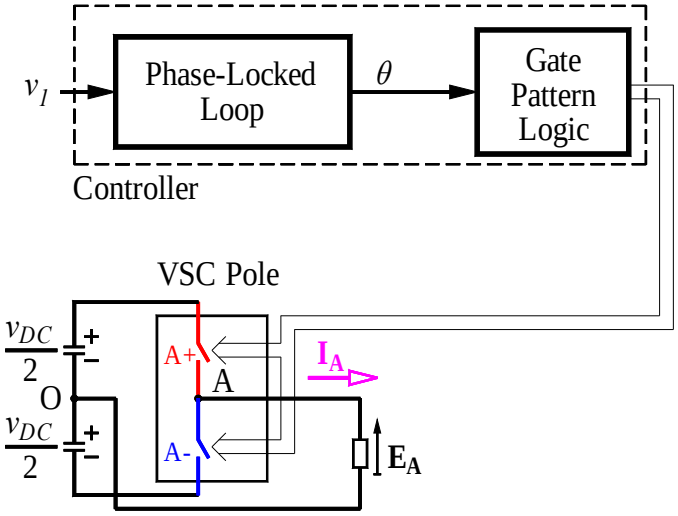


Figure 6-3. Model of a VSC pole in EMTP.

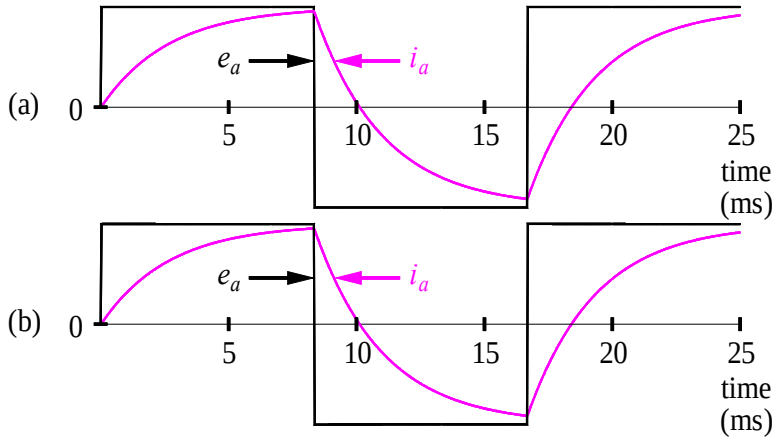


Figure 6-4. Voltages and currents from the simulation of a VSC pole with (a) ideal switches and (b) TAC-controlled switches.

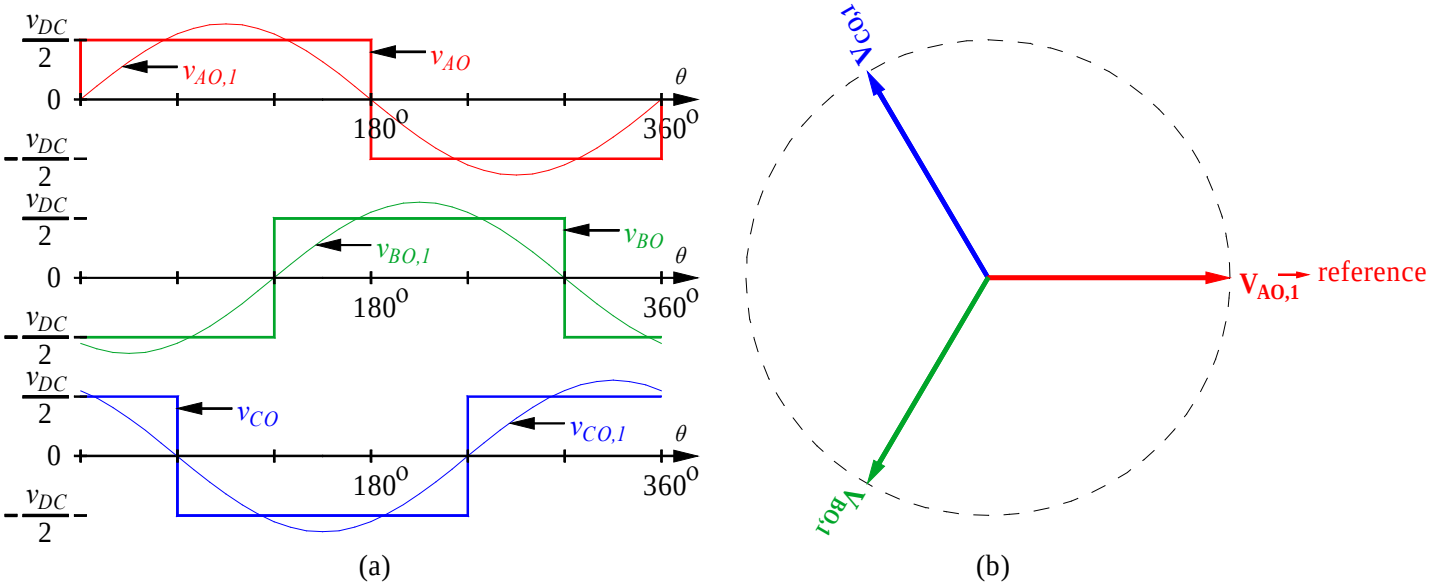


Figure 6-5. Pole voltages and fundamental voltage phasors in a six-pulse VSC configuration. (a) Three 120° phase-shifted fundamental pole voltages and the corresponding square wave voltages. (b) Phasor diagram of fundamental pole voltage phasors in a six-pulse VSC configuration.

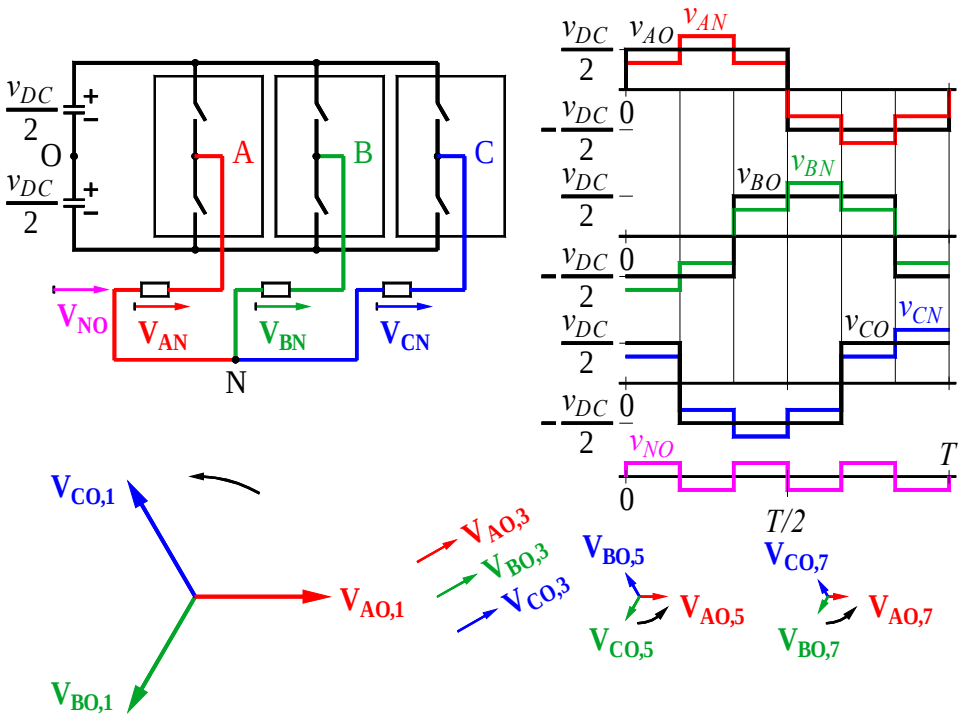


Figure 6-6. Six-pulse VSC and its output voltages.

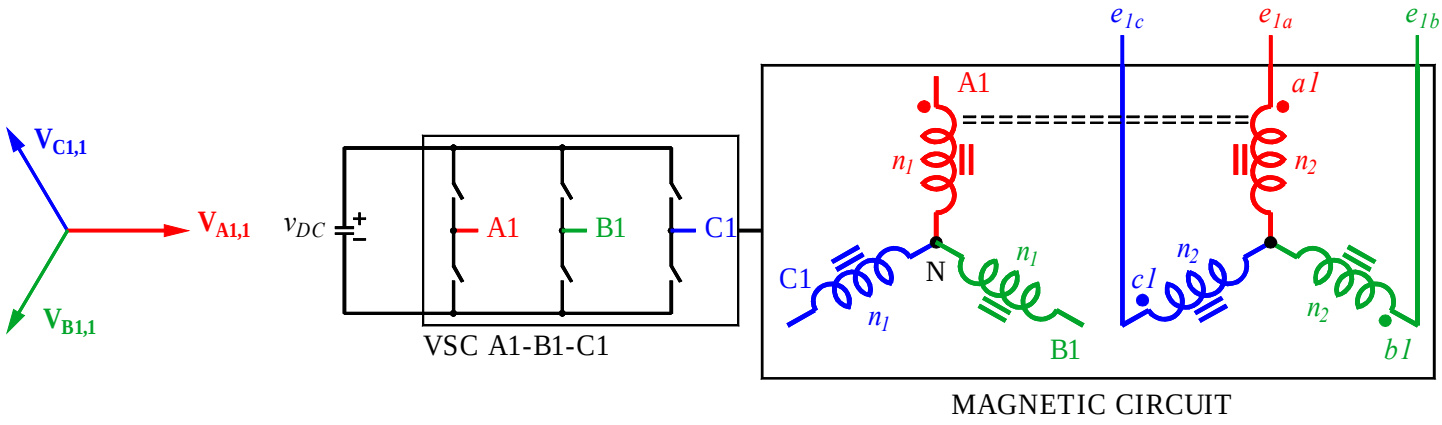


Figure 6-7. Six-pulse VSC model in EMTP.

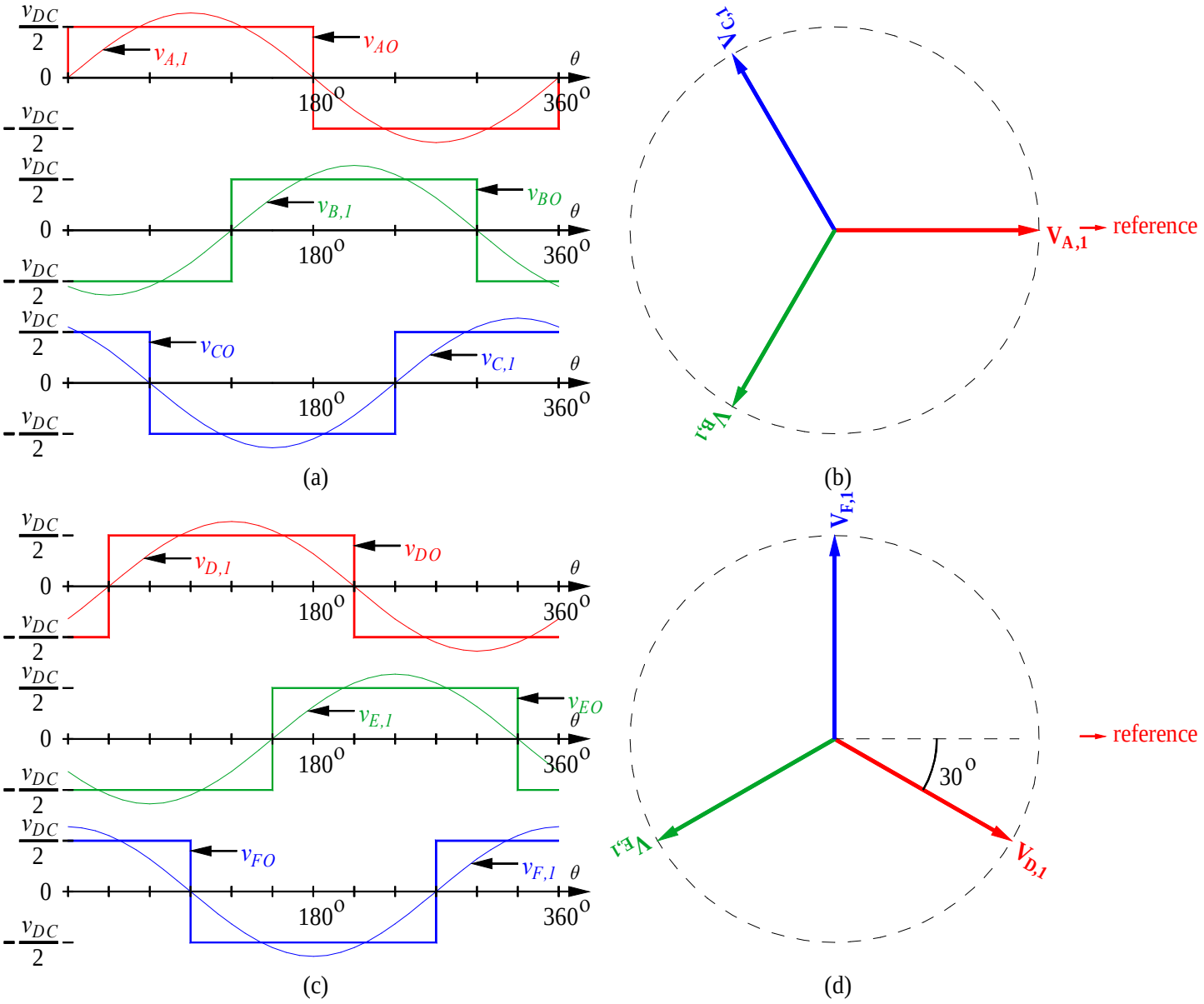


Figure 6-8. Pole voltages and fundamental voltage phasors in a 12-pulse HN-VSC configuration. (a) Three 120° phase-shifted fundamental pole voltages and the corresponding square wave voltages at 0°. (b) Phasor diagram of fundamental pole voltage phasors in A-B-C six-pulse VSC. (c) Three 120° phase-shifted fundamental pole voltages and the corresponding square wave voltages at –30°. (d) Phasor diagram of fundamental pole voltage phasors in D-E-F six-pulse VSC.

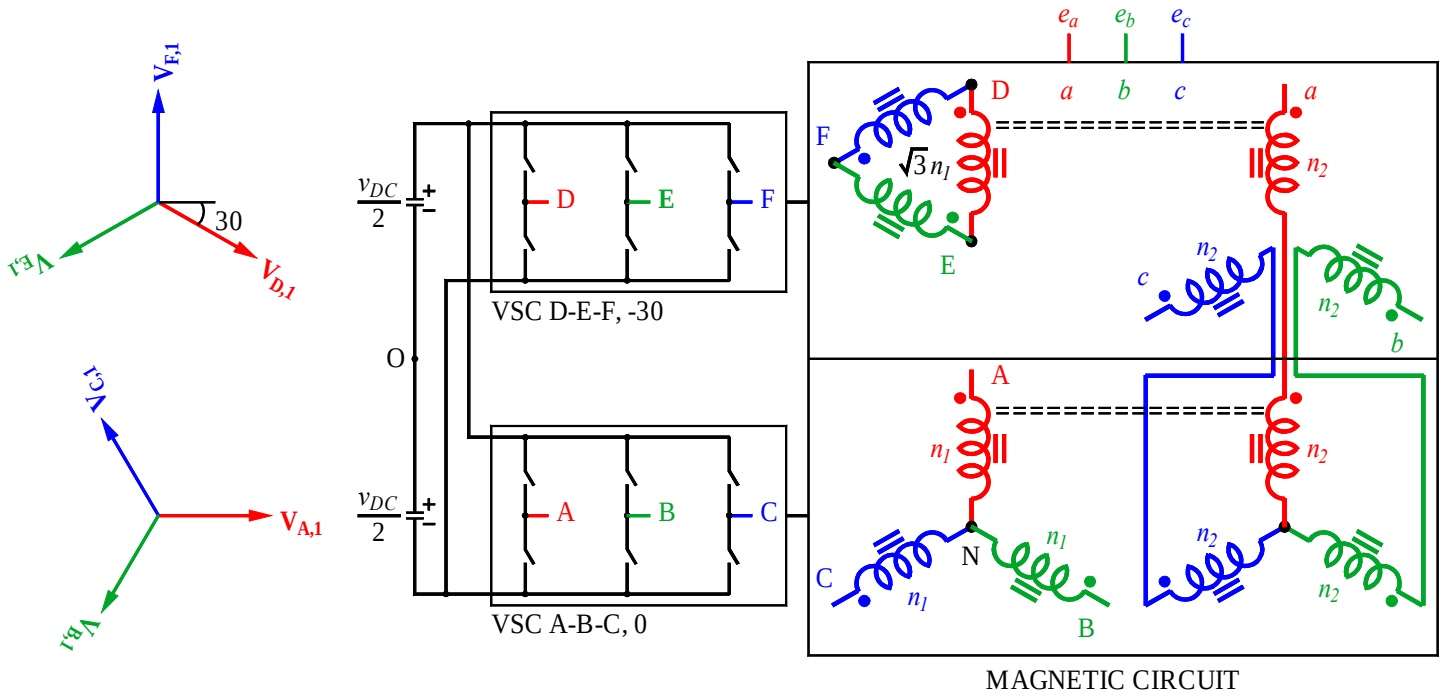


Figure 6-9. 12-pulse HN-VSC configuration (all angles are in degrees).

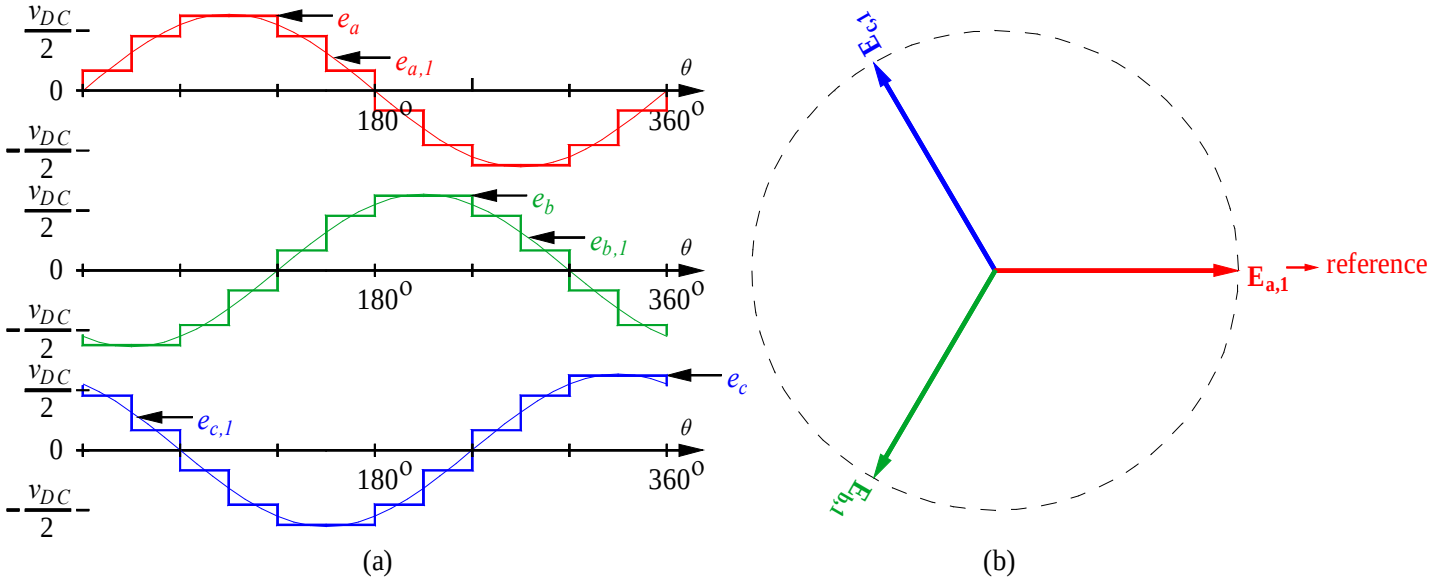


Figure 6-10. (a) Three 120^{o} phase-shifted fundamental output voltages and the corresponding 12-pulse voltages. (b) Phasor diagram of fundamental output voltage phasors in a 12-pulse HN-VSC configuration.

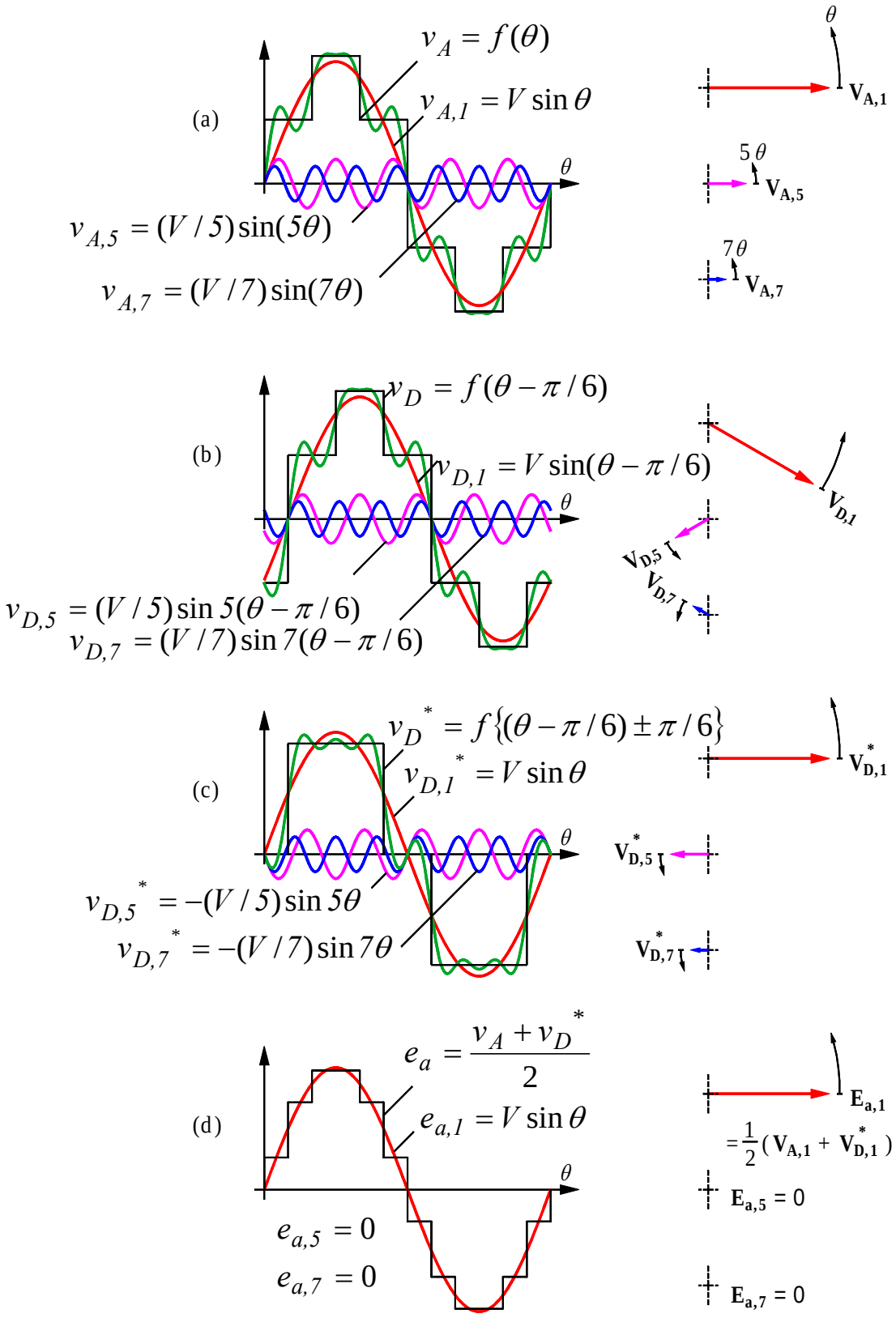


Figure 6-11. Graphical presentation of the cancellation technique of the fifth and the seventh harmonic components (all angles are in radians).

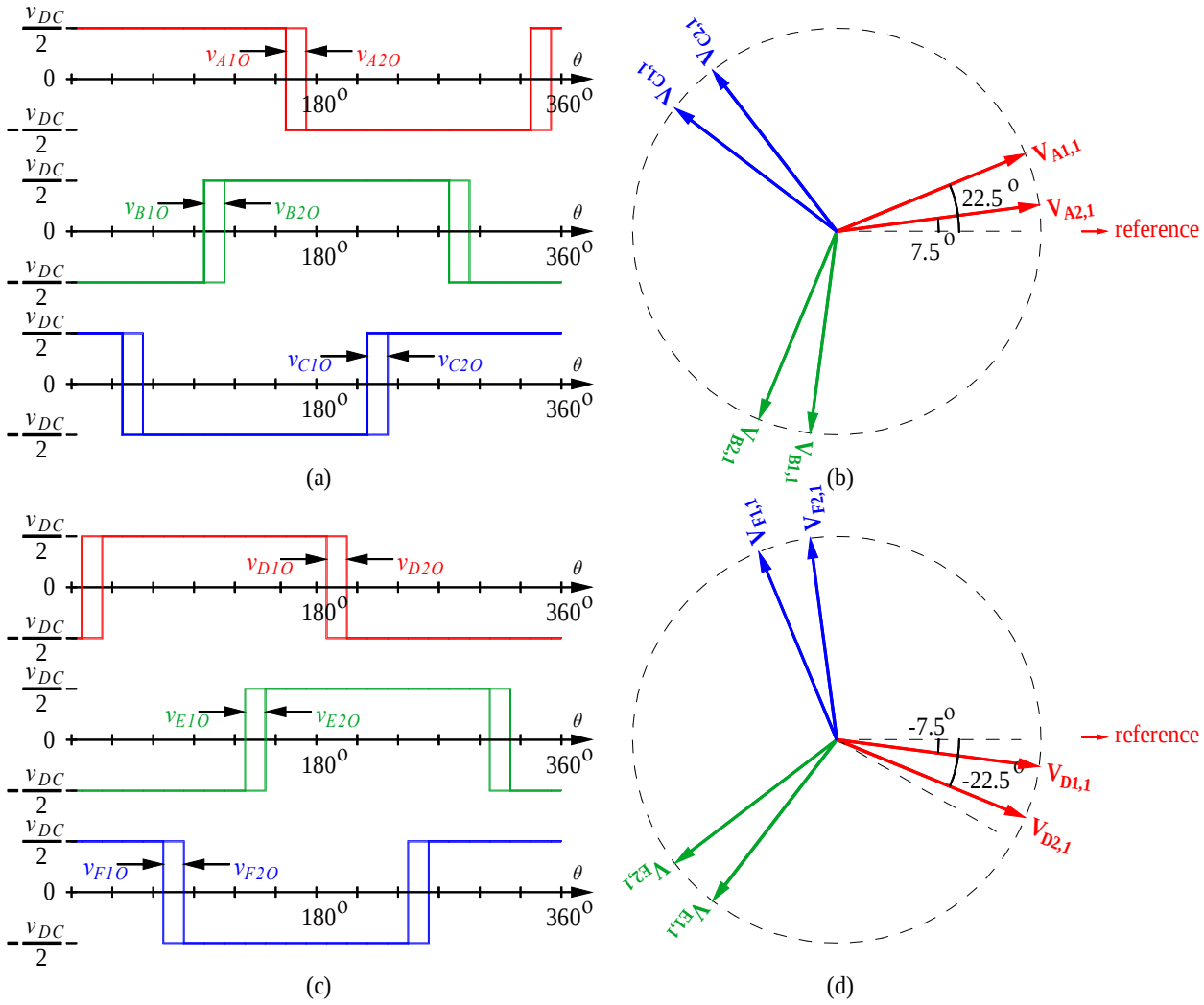


Figure 6-12. Pole voltages and fundamental voltage phasors in a 24-pulse HN-VSC configuration. (a) Two sets of square wave voltages at 22.5° and 7.5°. (b) Phasor diagram of fundamental pole voltage phasors in A1-B1-C1 six-pulse VSC and A2-B2-C2 six-pulse VSC. (c) Two sets of square wave voltages at –7.5° and –22.5°. (d) Phasor diagram of fundamental pole voltage phasors in D1-E1-F1 six-pulse VSC and D2-E2-F2 six-pulse VSC.

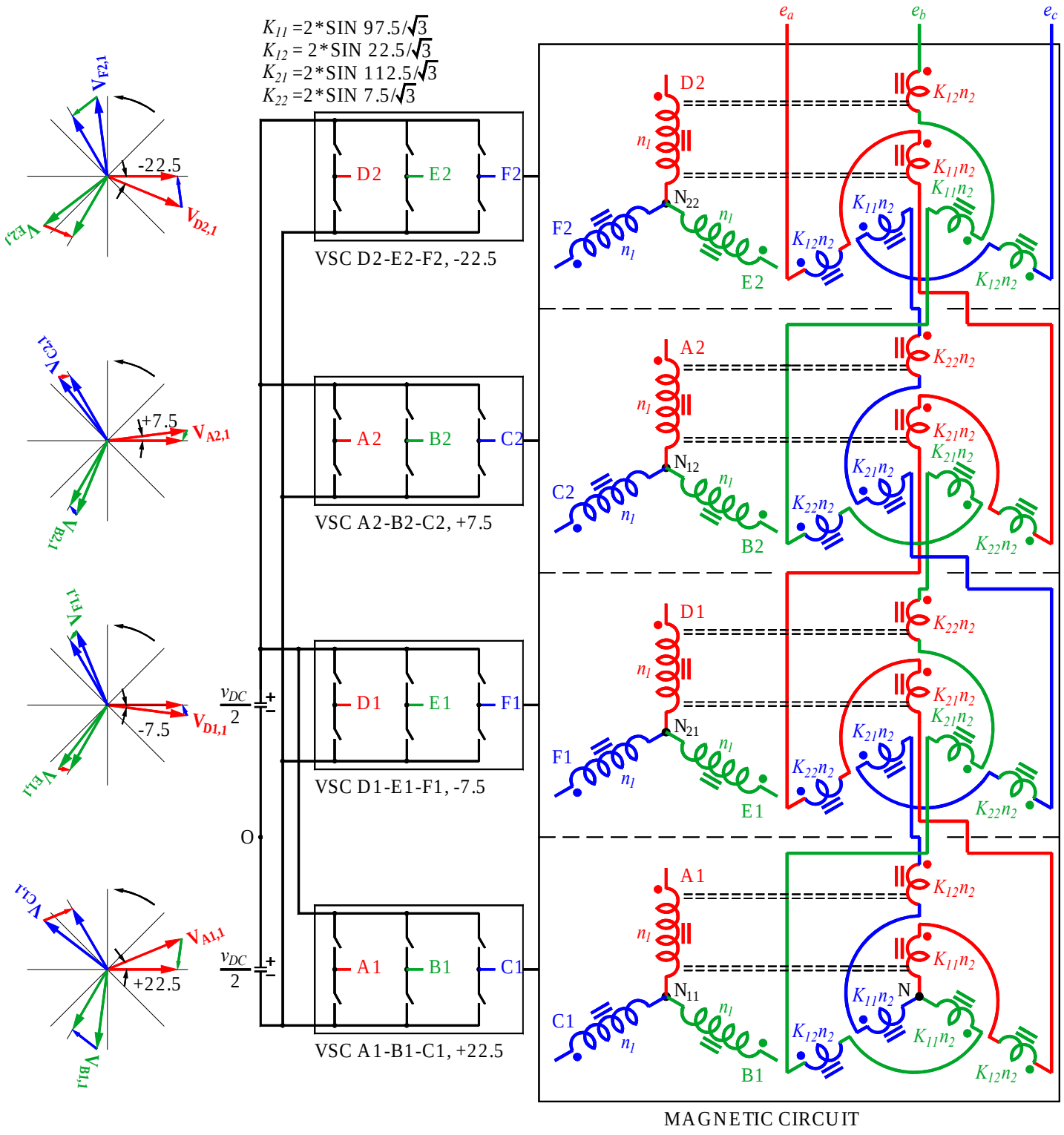


Figure 6-13. 24-pulse HN-VSC configuration (all angles are in degrees).

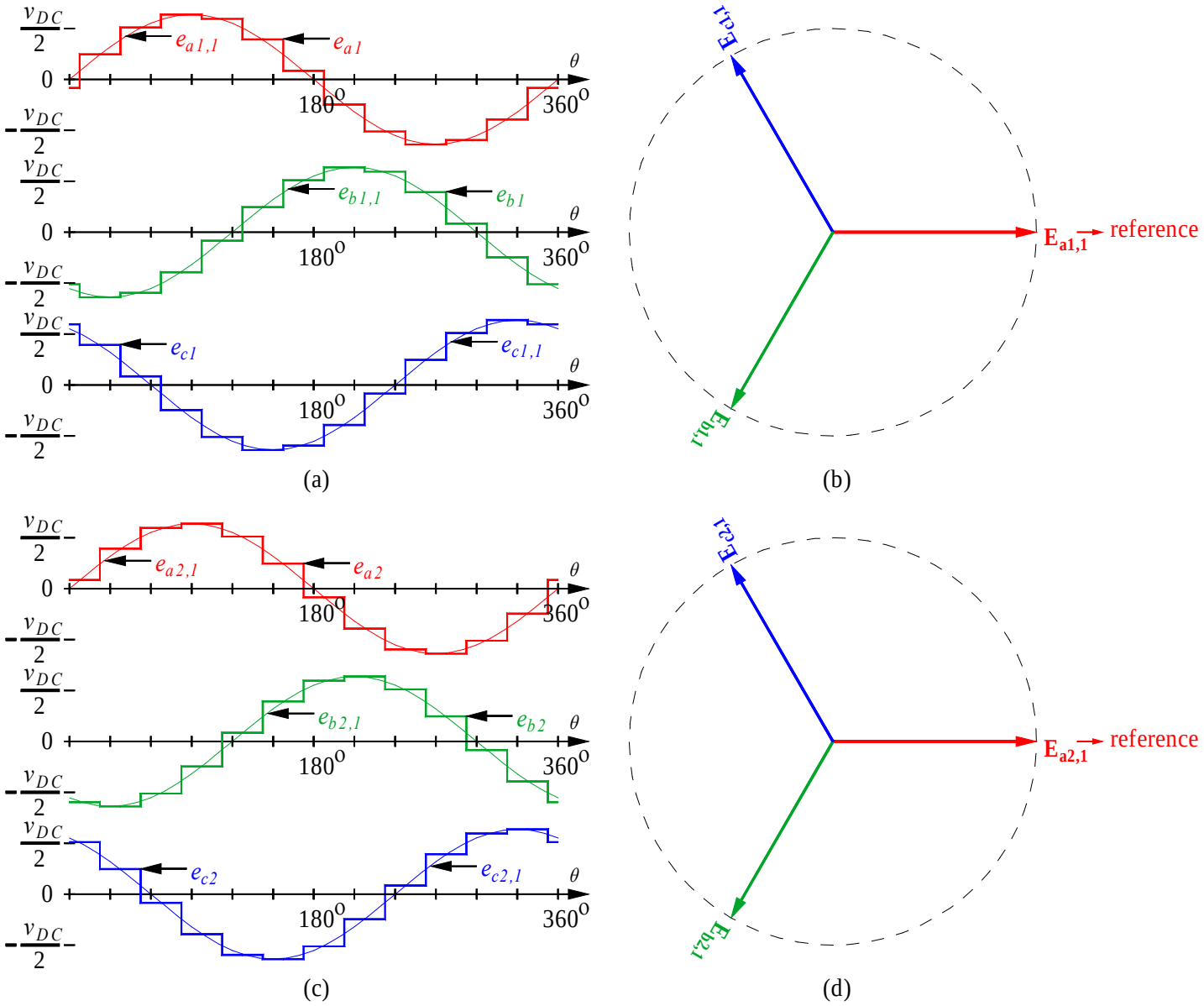


Figure 6-14. Two 12-pulse voltages and fundamental voltage phasors in a 24-pulse HN-VSC configuration. (a) Three 120° phase-shifted fundamental voltages and the corresponding 12-pulse voltages at 0°. (b) Phasor diagram of fundamental voltage phasors in *a1-b1-c1* 12-pulse HN-VSC. (c) Three 120° phase-shifted fundamental voltages and the corresponding 12-pulse voltages at 0°. (d) Phasor diagram of fundamental voltage phasors in *a2-b2-c2* 12-pulse HN-VSC.

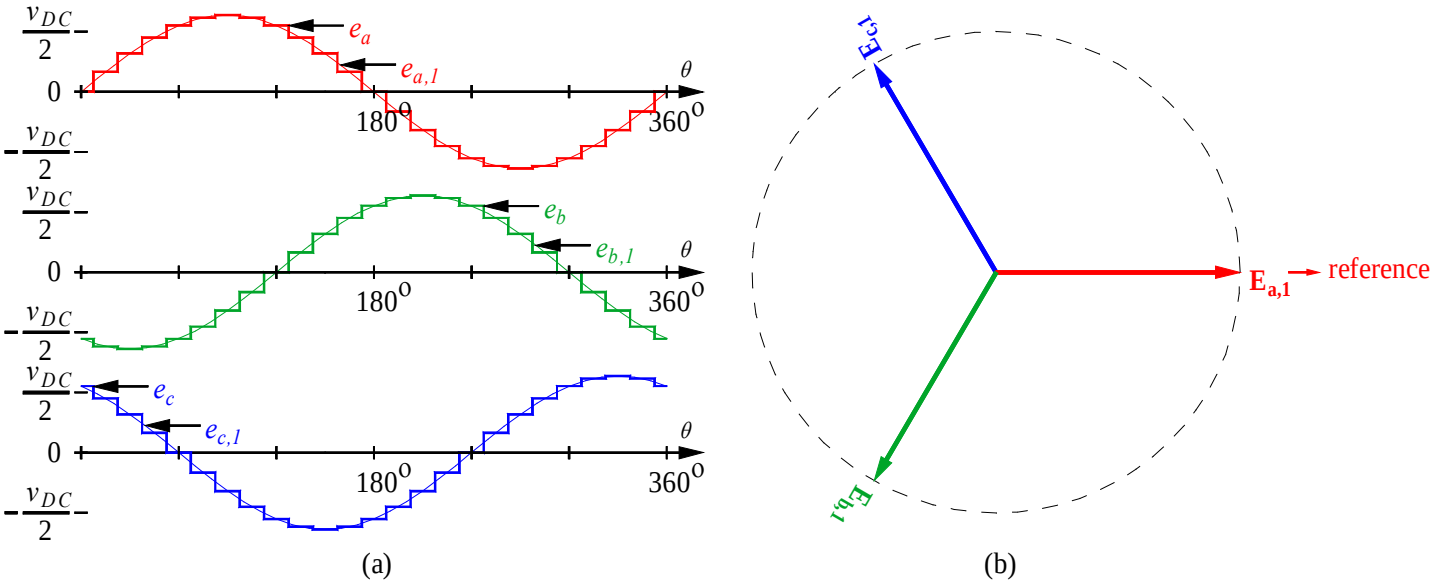


Figure 6-15. (a) Three 120° phase-shifted fundamental output voltages and the corresponding 24-pulse voltages. (b) Phasor diagram of fundamental output voltage phasors in a 24-pulse HN-VSC configuration.

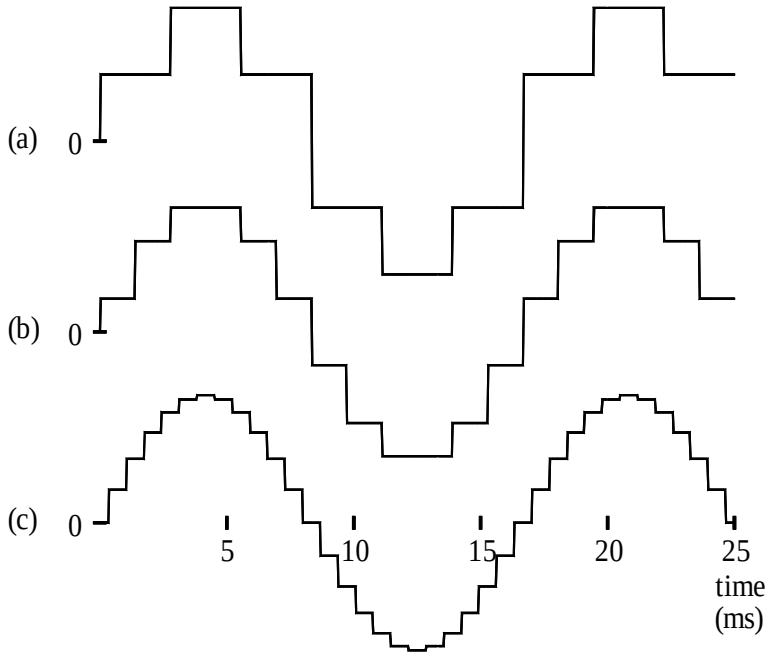


Figure 6-16. Output voltages from the simulation of (a) a 6-pulse HN-VSC, (b) a 12-pulse HN-VSC, and (c) a 24-pulse HN-VSC.

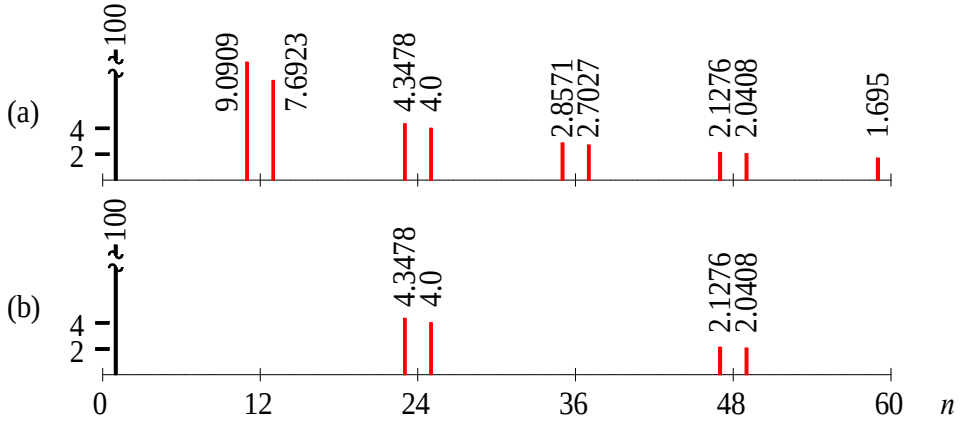


Figure 6-17. Normalized harmonic components of output voltages from (a) a 12-pulse HN-VSC and (b) a 24-pulse HN-VSC as a function of harmonic order (n).

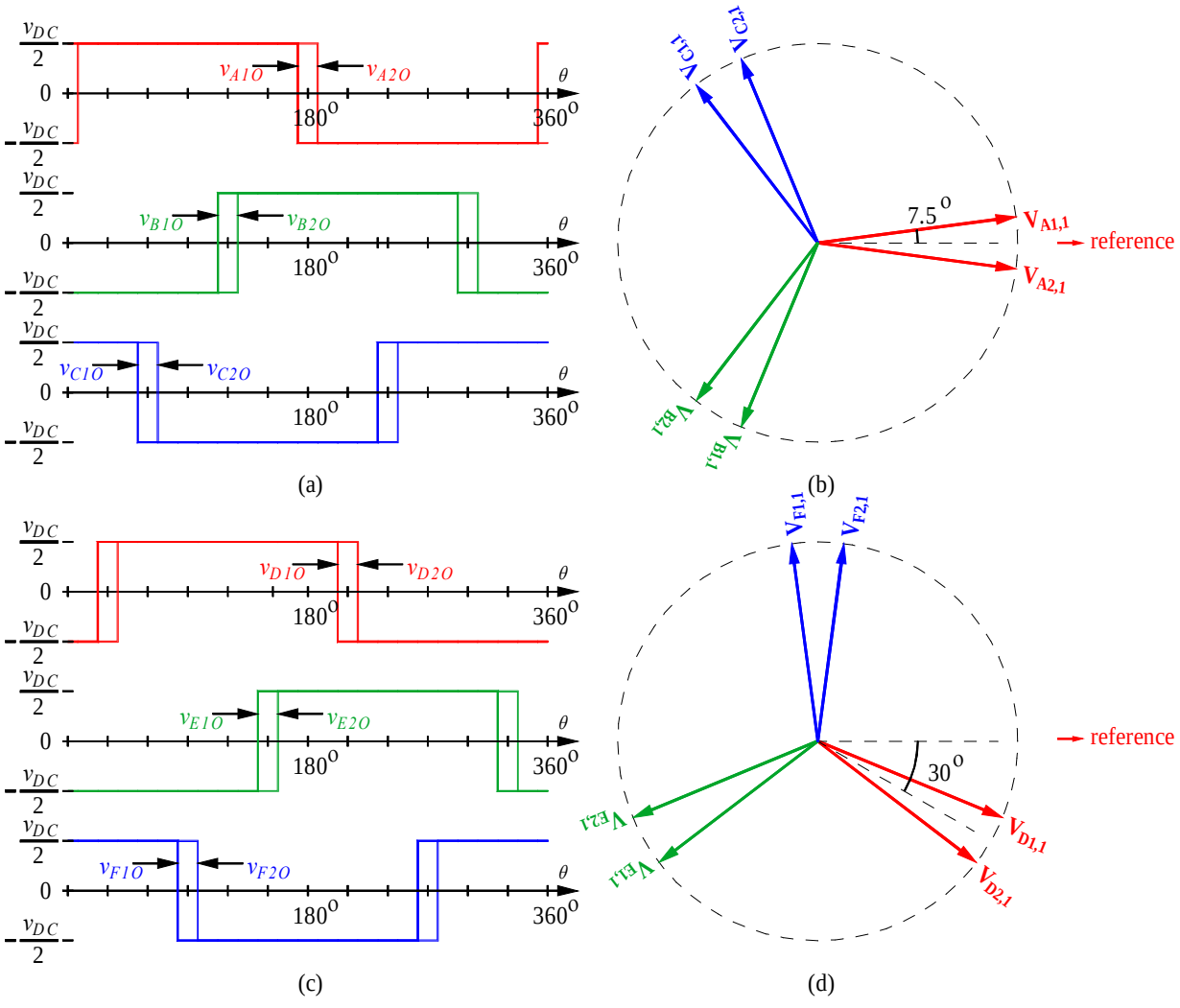


Figure 6-18. Pole voltages and fundamental voltage phasors in a 24-pulse QHN-VSC configuration. (a) Two sets of square wave voltages at 7.5° and –7.5°. (b) Phasor diagram of fundamental pole voltage phasors in A1-B1-C1 six-pulse VSC and A2-B2-C2 six-pulse VSC. (c) Two sets of square wave voltages at –22.5° and –37.5°. (d) Phasor diagram of fundamental pole voltage phasors in D1-E1-F1 six-pulse VSC and D2-E2-F2 six-pulse VSC.

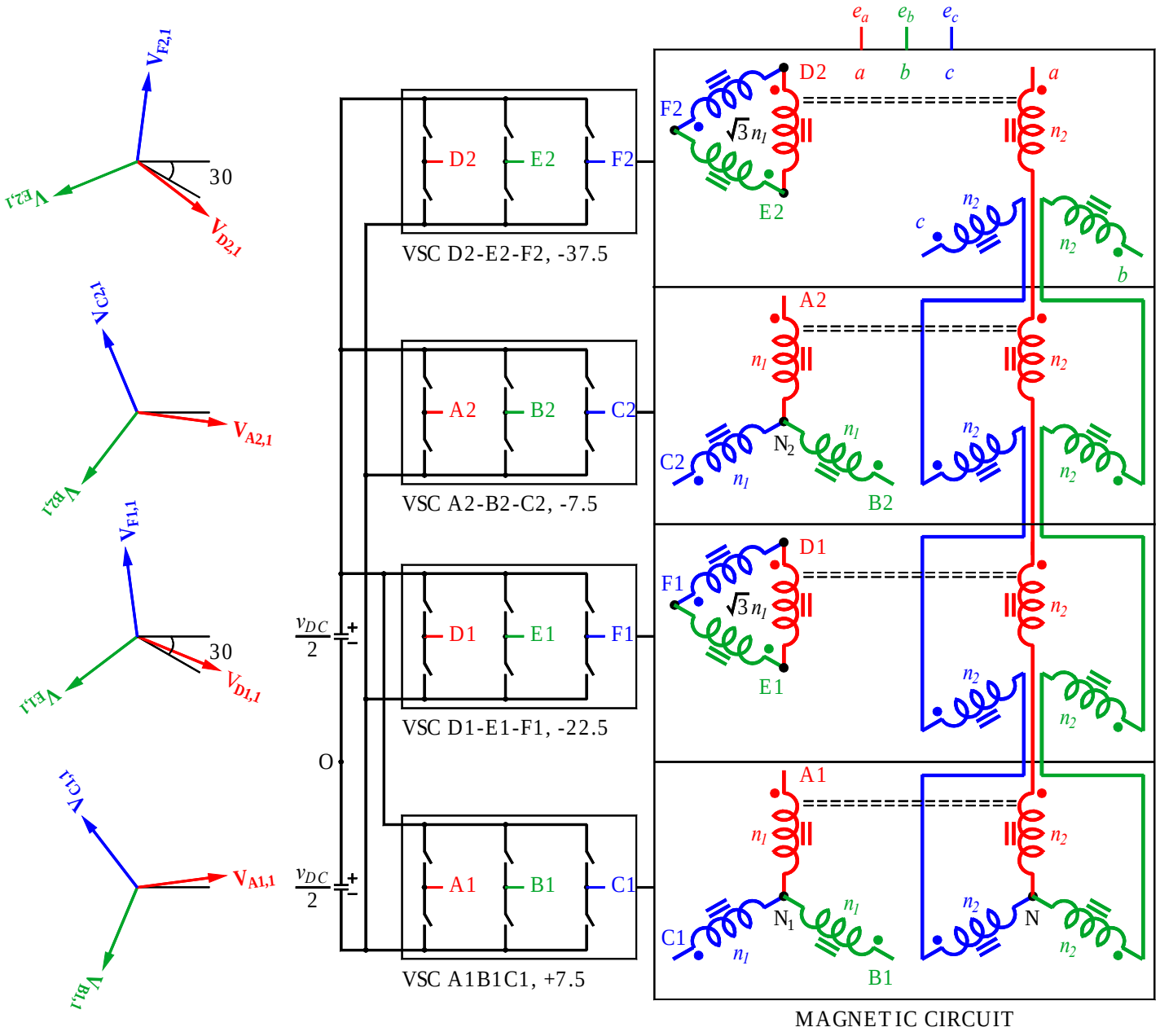


Figure 6-19. 24-pulse QHN-VSC configuration (all angles are in degrees).

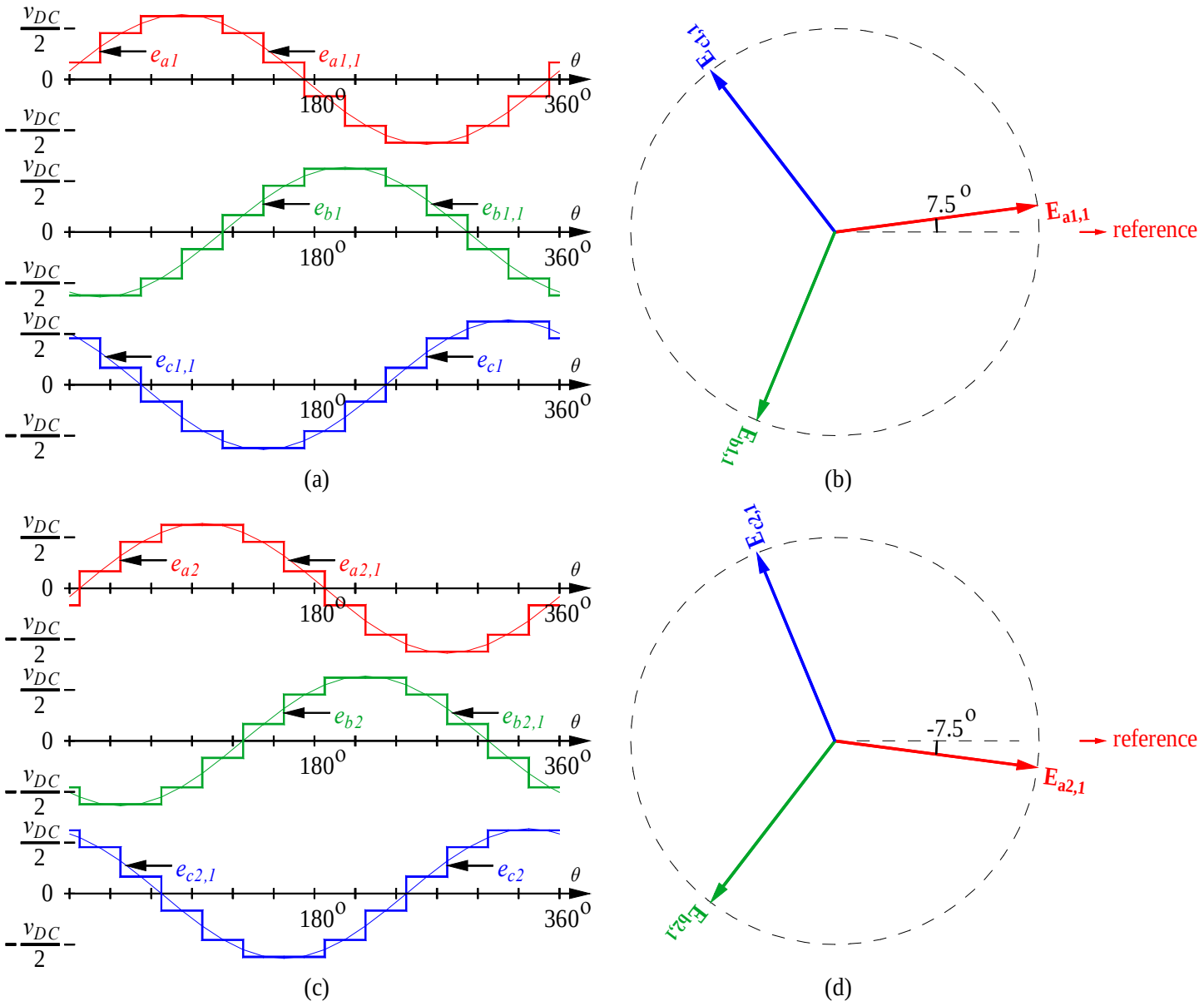


Figure 6-20. Two 12-pulse voltages and fundamental voltage phasors in a 24-pulse QHN-VSC configuration. (a) Three 120° phase-shifted fundamental voltages and the corresponding 12-pulse voltages at 7.5°. (b) Phasor diagram of fundamental voltage phasors in *a1-b1-c1* 12-pulse HN-VSC. (c) Three 120° phase-shifted fundamental voltages and the corresponding 12-pulse voltages at –7.5°. (d) Phasor diagram of fundamental voltage phasors in *a2-b2-c2* 12-pulse HN-VSC.

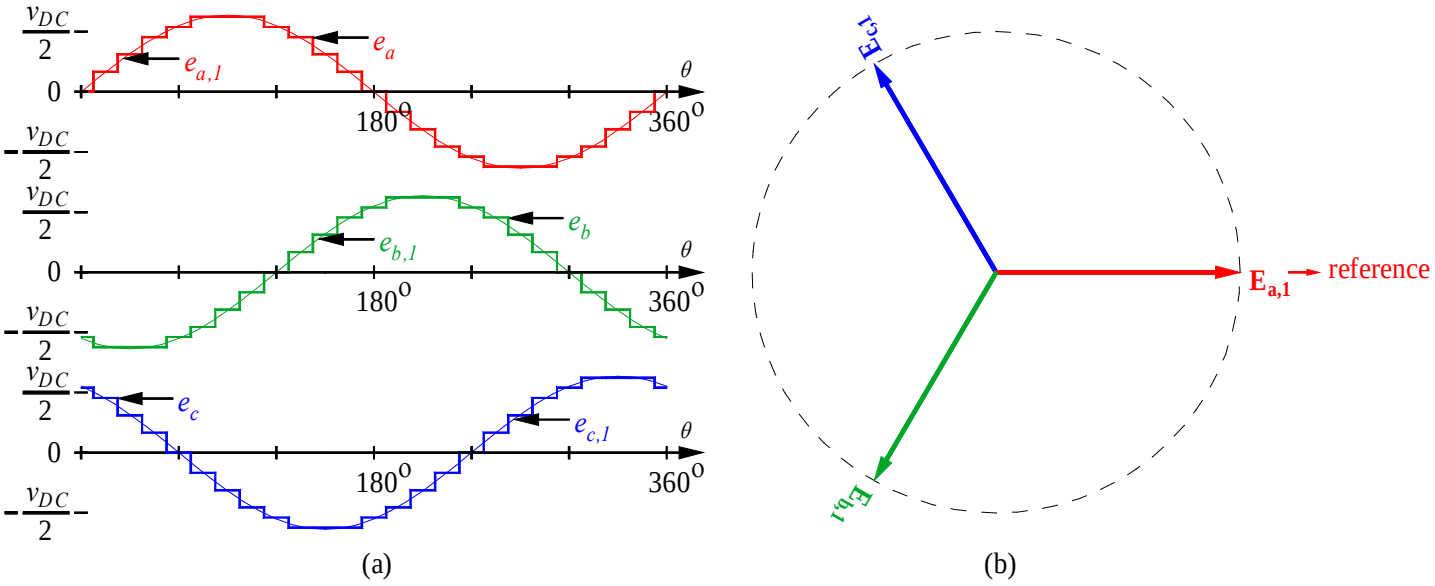


Figure 6-21. (a) Three 120° phase-shifted fundamental output voltages and the corresponding 24-pulse voltages. (b) Phasor diagram of fundamental output voltage phasors in a 24-pulse QHN-VSC configuration.

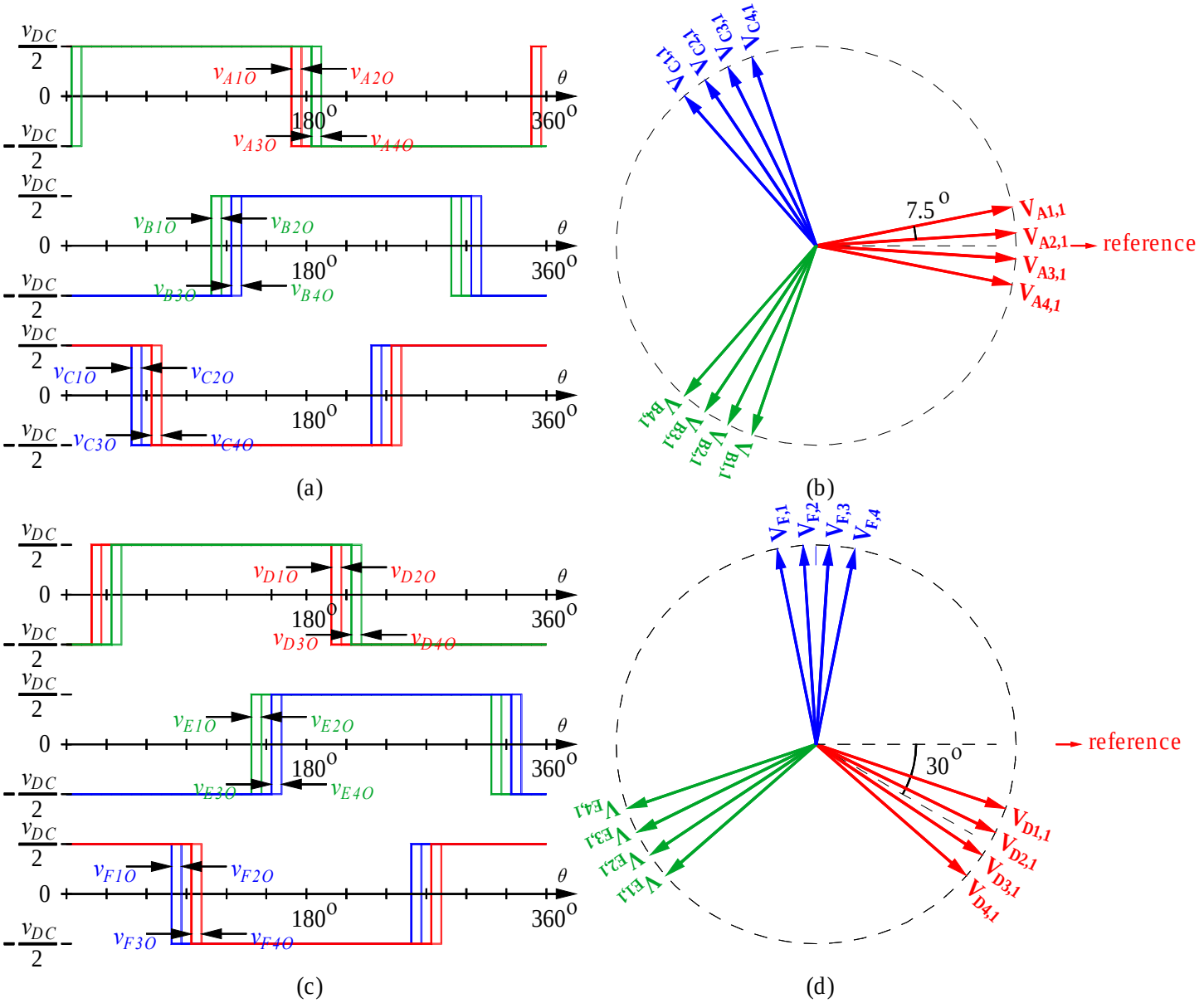


Figure 6-22. Pole voltages and fundamental voltage phasors in a 48-pulse QHN-VSC configuration. (a) Four sets of square wave voltages at 11.25°, 3.75°, –3.75°, and –11.25°. (b) Phasor diagram of fundamental pole voltage phasors in A1-B1-C1 six-pulse VSC, A2-B2-C2 six-pulse VSC, A3-B3-C3 six-pulse VSC, and A4-B4-C4 six-pulse VSC. (c) Four sets of square wave voltages at –18.75°, –26.25°, –33.75°, and –41.25°. (d) Phasor diagram of fundamental pole voltage phasors in D1-E1-F1 six-pulse VSC, D2-E2-F2 six-pulse VSC, D3-E3-F3 six-pulse VSC, and D4-E4-F4 six-pulse VSC.

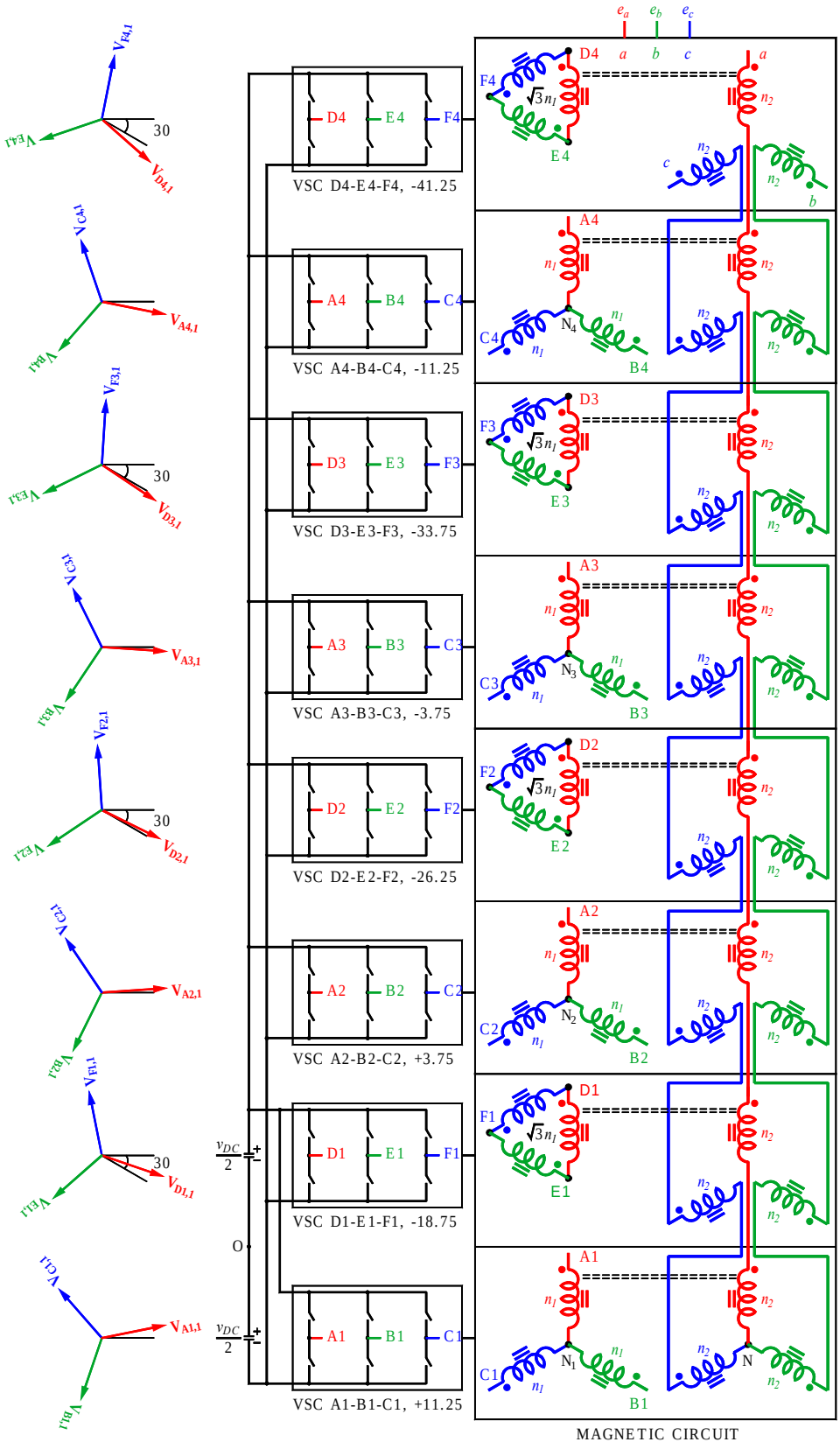


Figure 6-23. 48-pulse QHN-VSC configuration (all angles are in degrees).

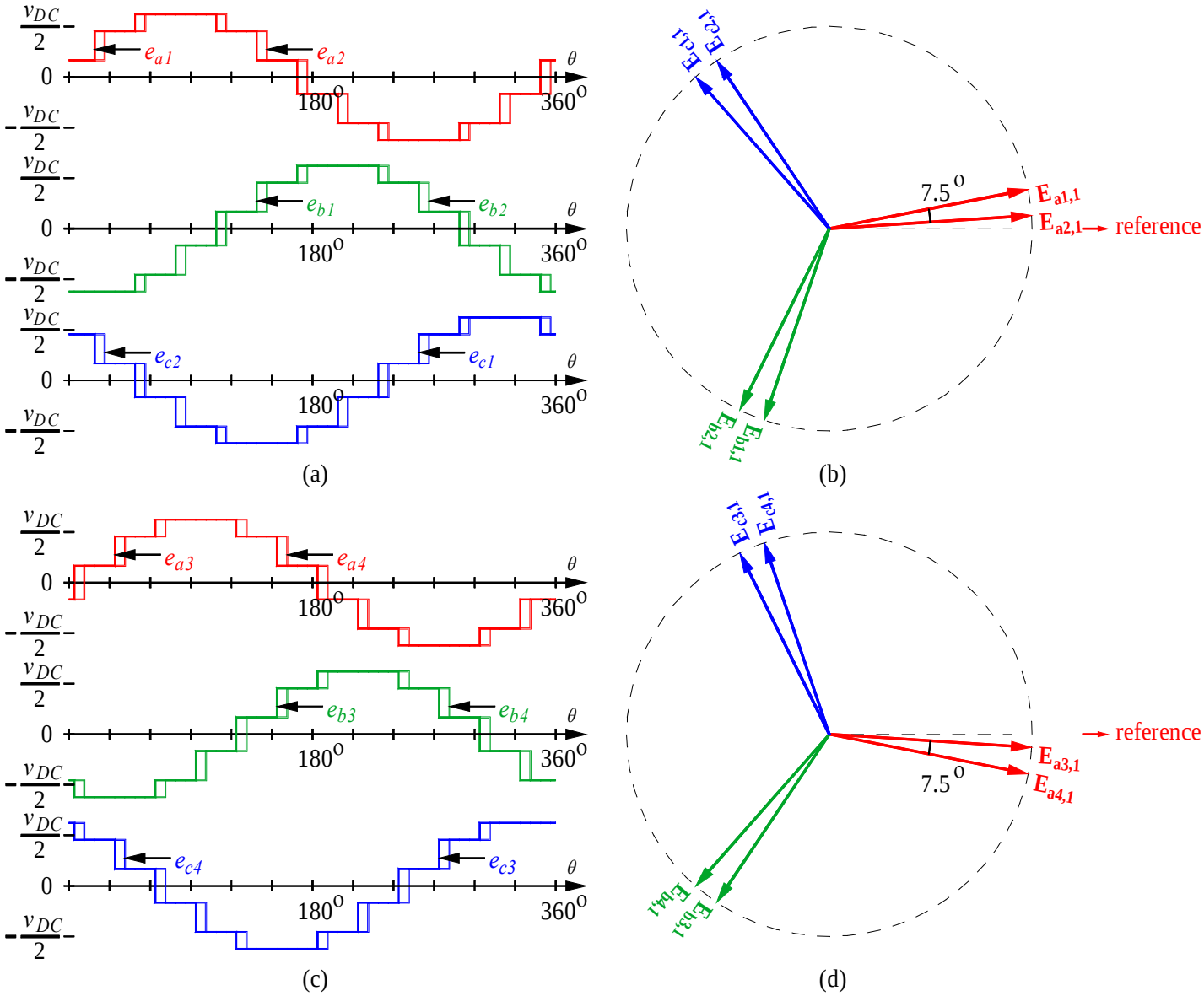


Figure 6-24. Four 12-pulse voltages and fundamental voltage phasors in a 48-pulse QHN-VSC configuration. (a) Two 12-pulse voltages at 11.25° and 3.75°, respectively. (b) Phasor diagram of fundamental voltage phasors in *a1-b1-c1* and *a2-b2-c2* 12-pulse HN-VSCs. (c) Two 12-pulse voltages at –11.25° and –3.75°, respectively. (d) Phasor diagram of fundamental voltage phasors in *a3-b3-c3* and *a4-b4-c4* 12-pulse HN-VSCs.

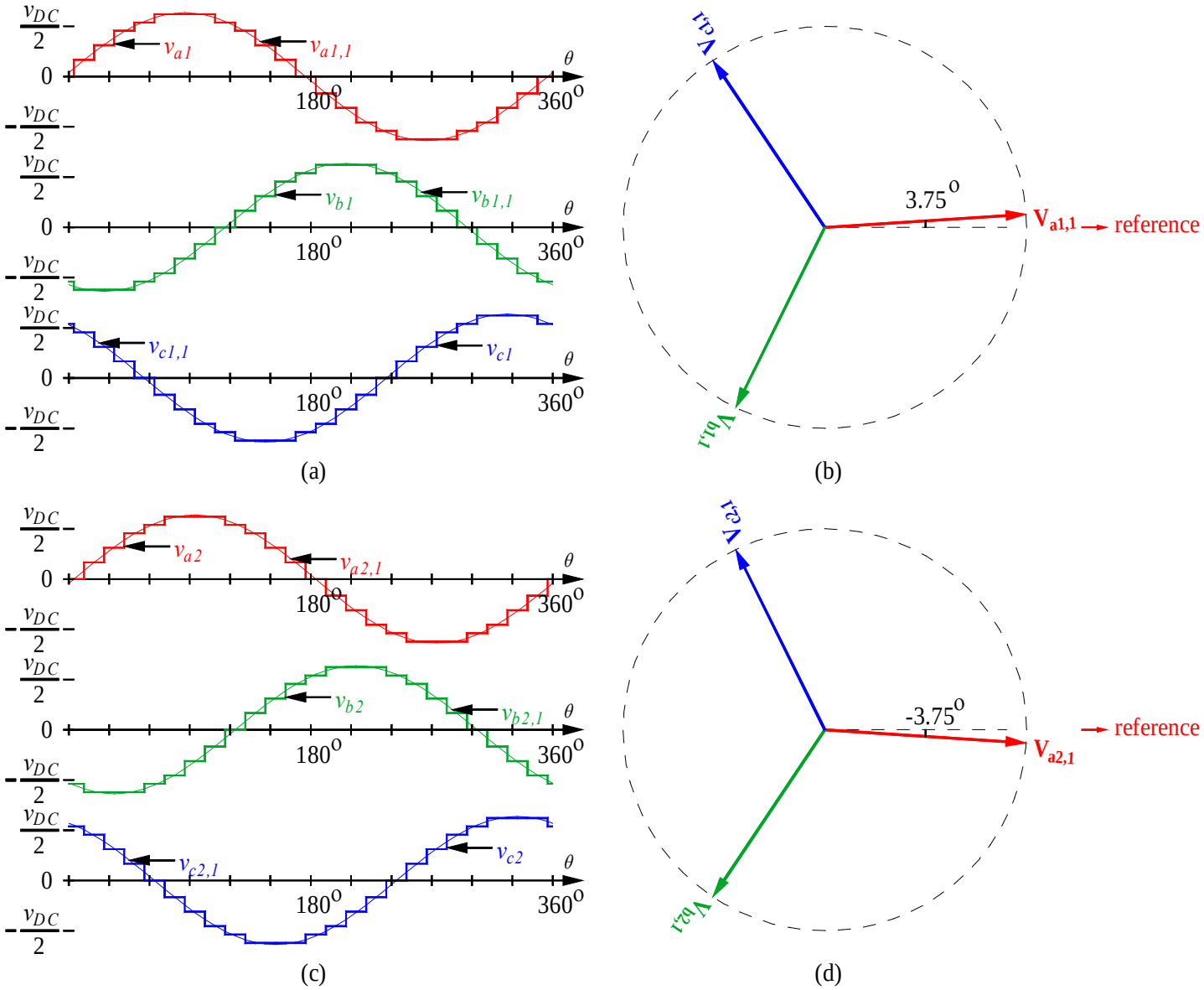


Figure 6-25. Two 24-pulse voltages and fundamental voltage phasors in a 48-pulse QHN-VSC configuration. (a) Three 120° phase-shifted fundamental voltages and the corresponding 24-pulse voltages at 3.75°. (b) Phasor diagram of fundamental voltage phasors in *a1-b1-c1* 24-pulse QHN-VSC. (c) Three 120° phase-shifted fundamental voltages and the corresponding 12-pulse voltages at –3.75°. (d) Phasor diagram of fundamental voltage phasors in *a2-b2-c2* 24-pulse QHN-VSC.

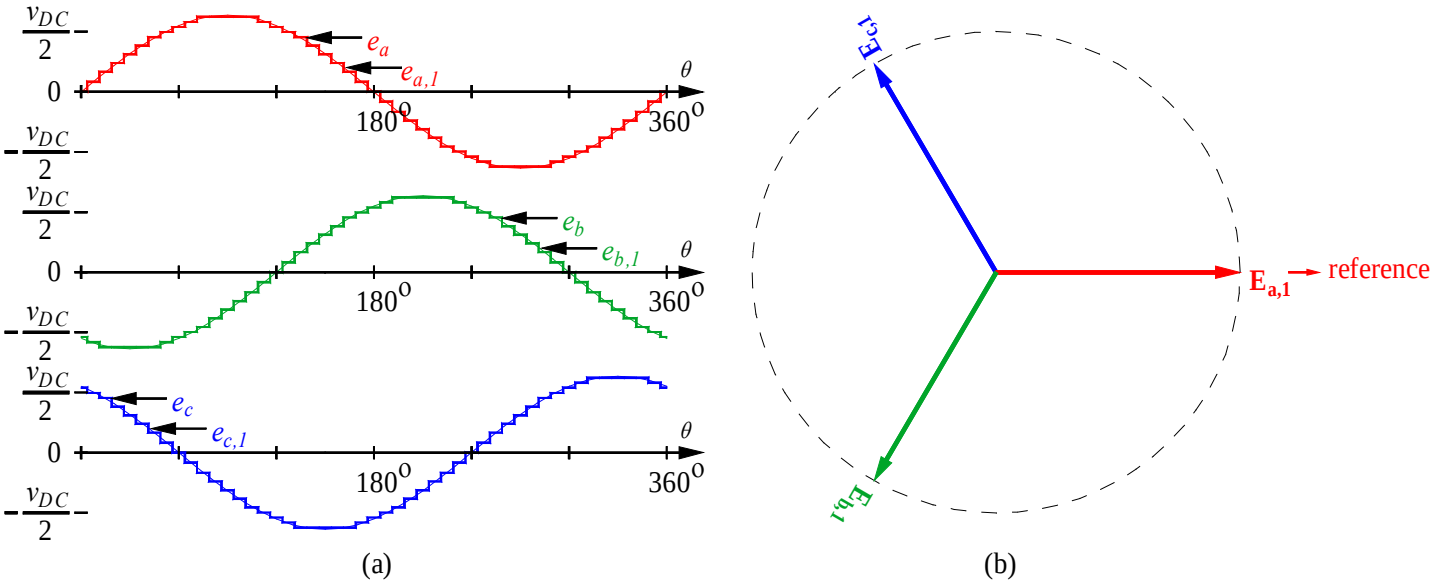


Figure 6-26. (a) Three 120° phase-shifted fundamental output voltages and the corresponding 48-pulse voltages. (b) Phasor diagram of fundamental output voltage phasors in a 48-pulse QHN-VSC configuration.

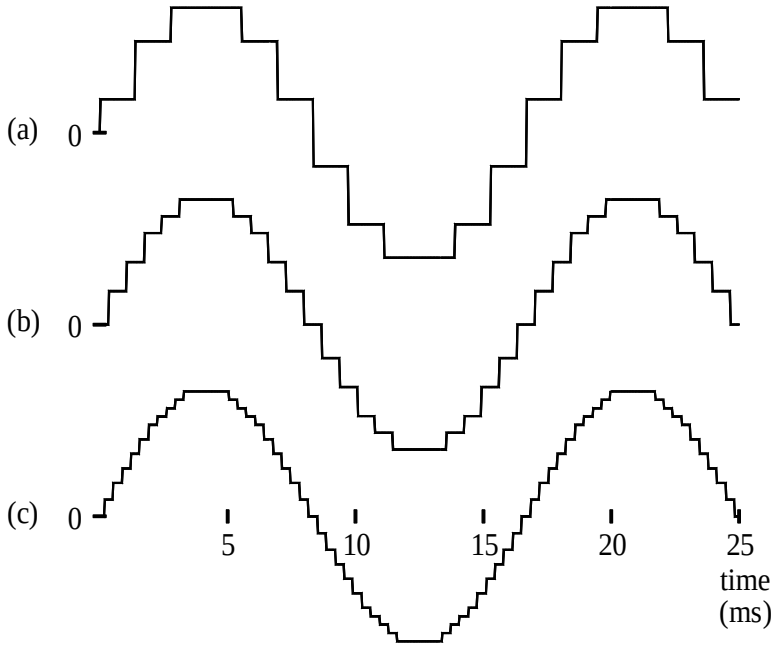


Figure 6-27. Output voltages from the simulation of (a) a 12-pulse HN-VSC, (b) a 24-pulse QHN-VSC, and (c) a 48-pulse QHN-VSC.

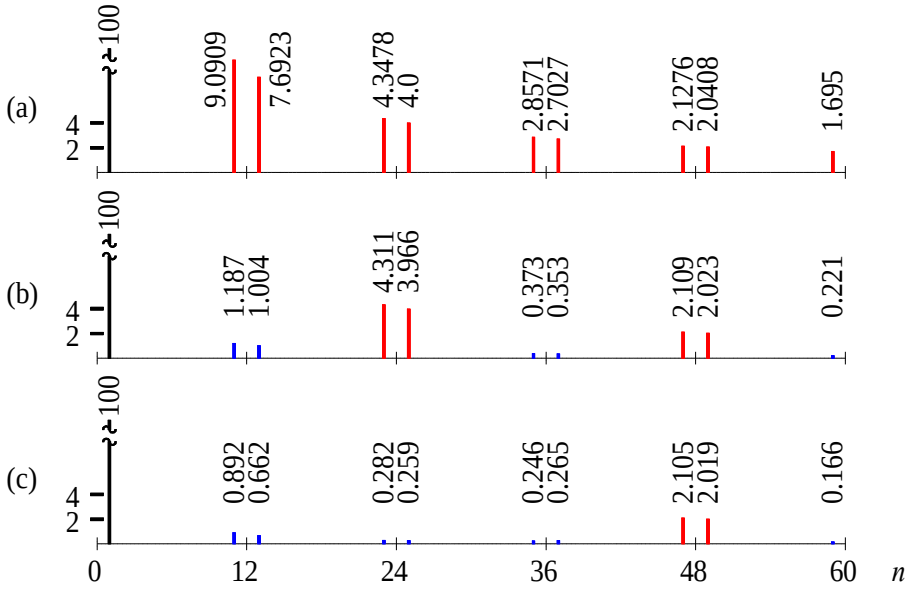


Figure 6-28. Normalized harmonic components of output voltages from (a) a 12-pulse HN-VSC, (b) a 24-pulse QHN-VSC, and (c) a 48-pulse QHN-VSC as a function of harmonic order (n).

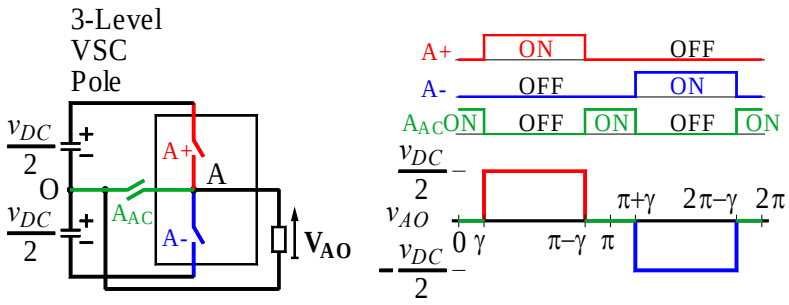


Figure 6-29. Three-level VSC “pole” and its output voltage (all angles are in radians).

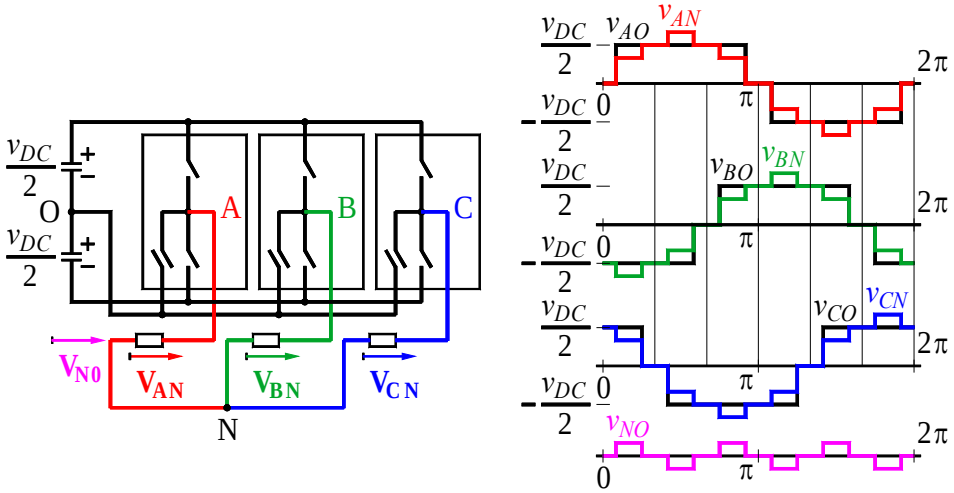


Figure 6-30. Six-pulse VSC with three-level poles and its output voltages (all angles are in radians).

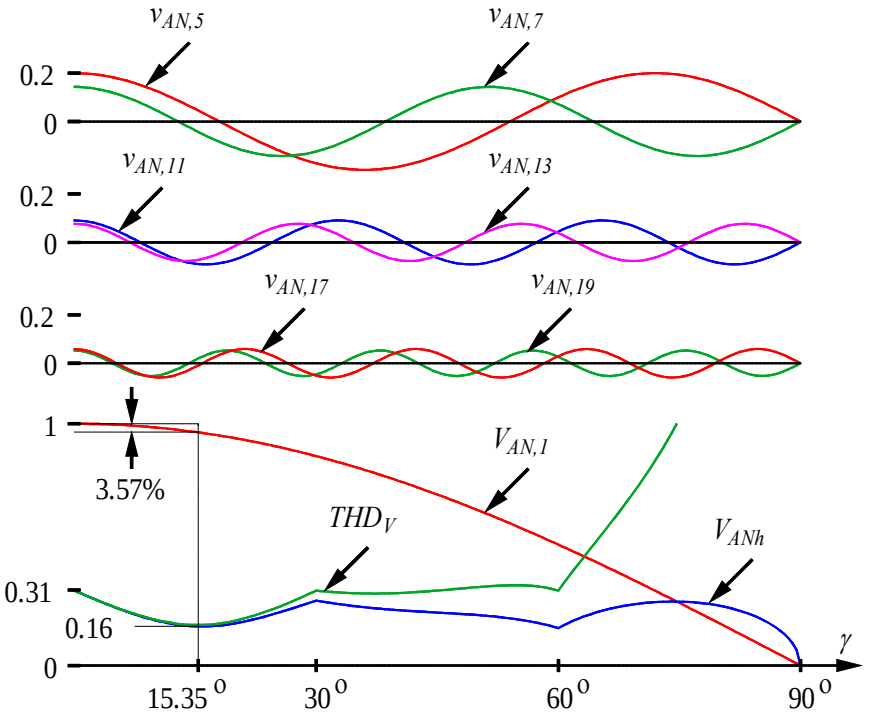


Figure 6-31. Variations of amplitudes of fundamental and harmonic components, harmonic content, and total harmonic distortion factor as a function of (γ), which is the dead angle of a three-level pole.

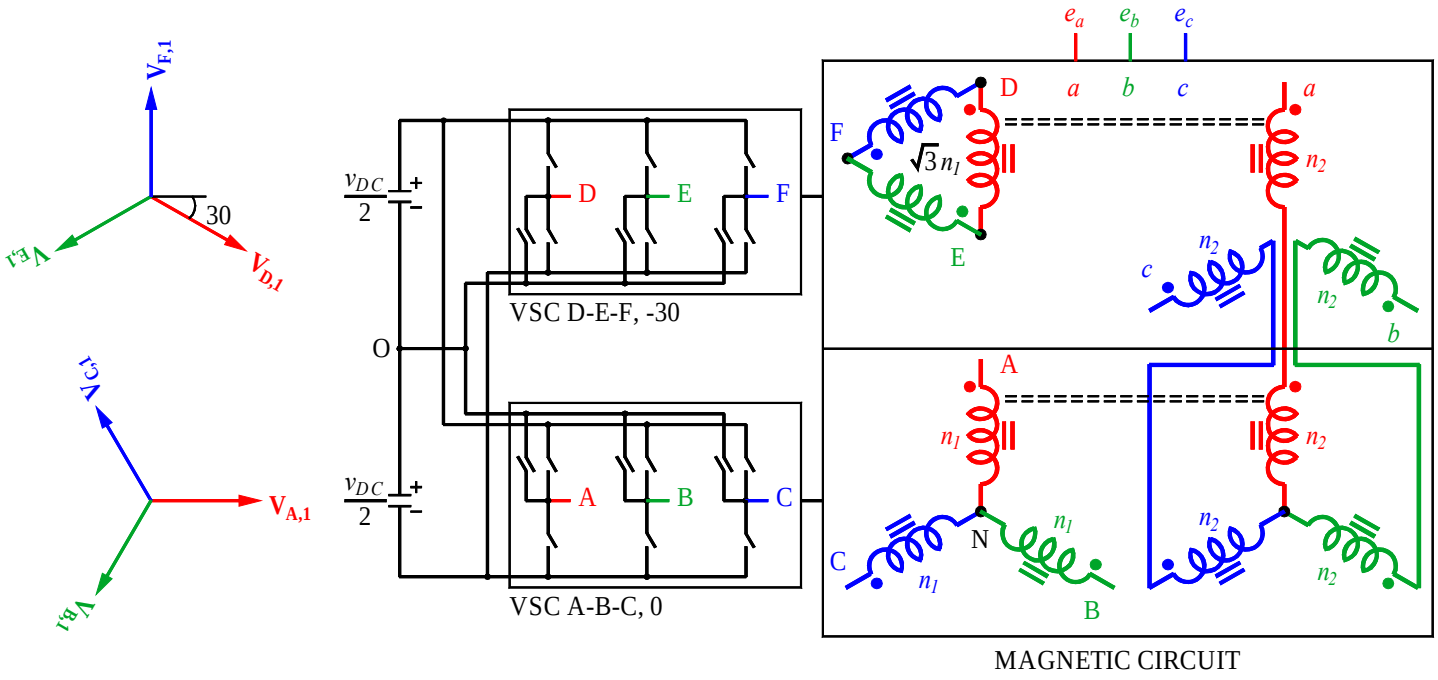


Figure 6-32. Twelve-pulse HN-VSC configuration with three-level poles (all angles are in degrees).

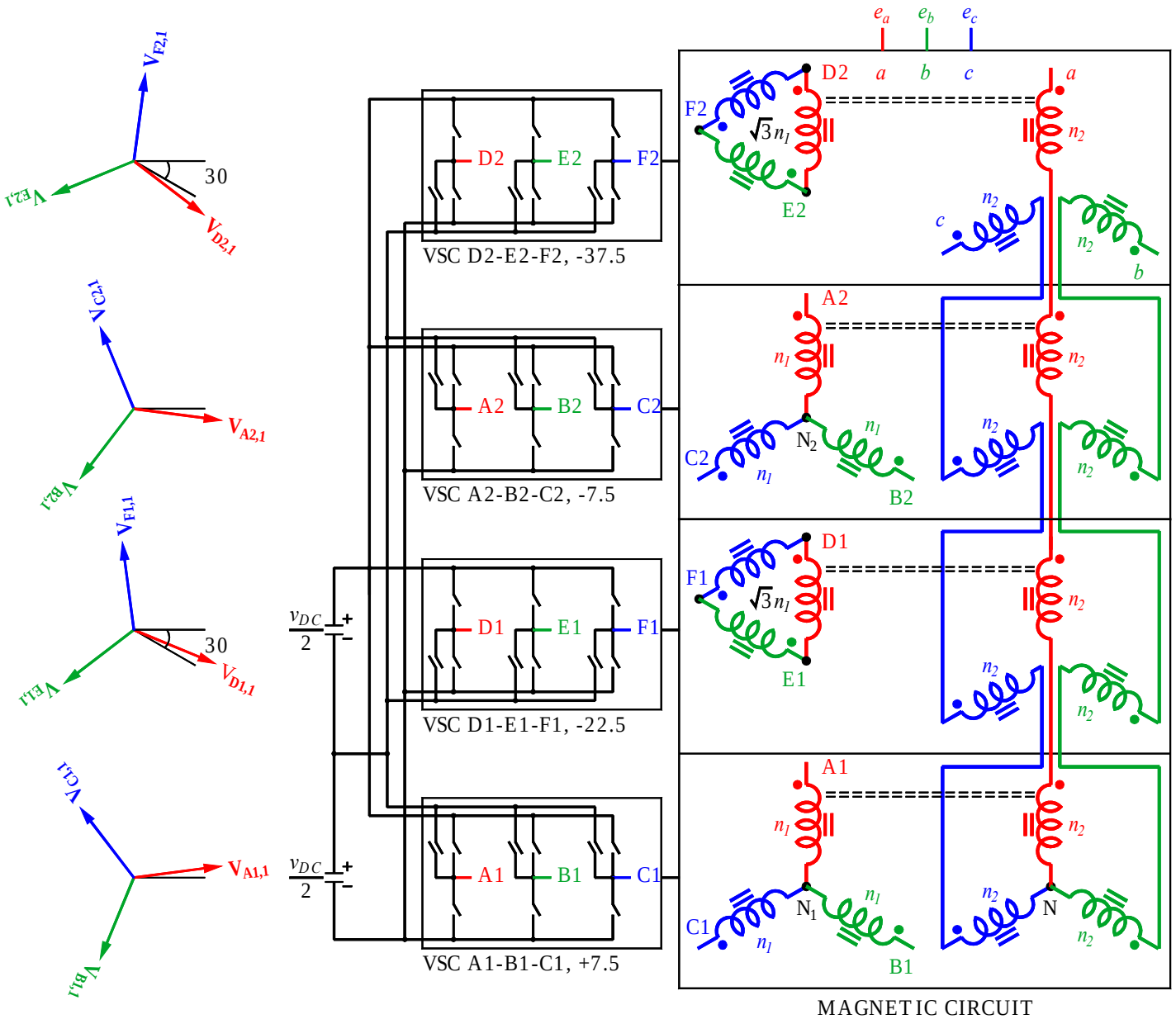


Figure 6-33. 24-pulse QHN-VSC configuration with three-level poles (all angles are in degrees).

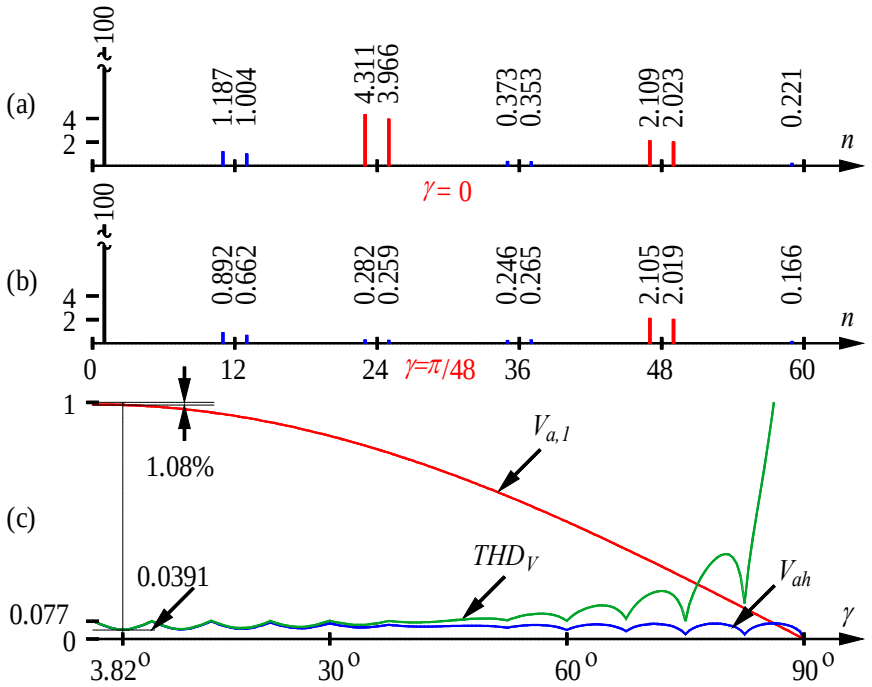


Figure 6-34. Normalized harmonic components of output voltages from (a) a 24-pulse QHN-VSC and (b) a 48-pulse QHN-VSC as a function of harmonic order. (c) Variations of amplitude of fundamental component, harmonic content, and THD as a function of γ, which is the dead angle of a three-level pole.

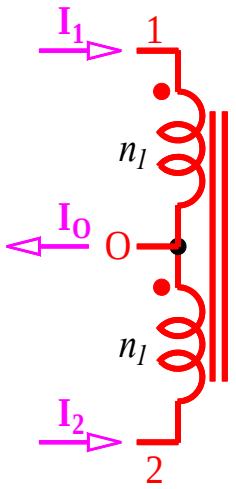


Figure 6-35. Interphase transformer.

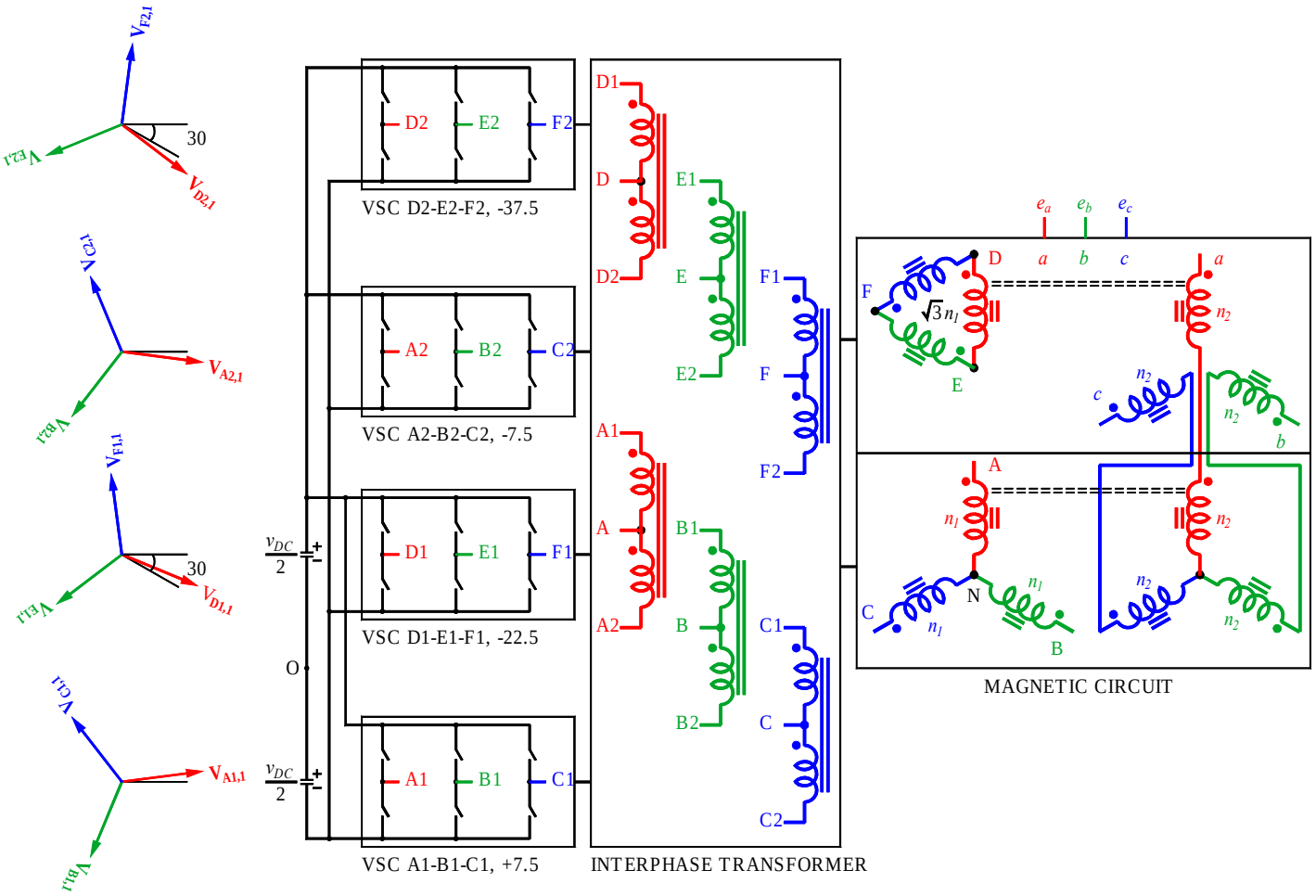


Figure 6-36. 24-pulse QHN-VSC configuration with interphase transformers (all angles are in degrees).

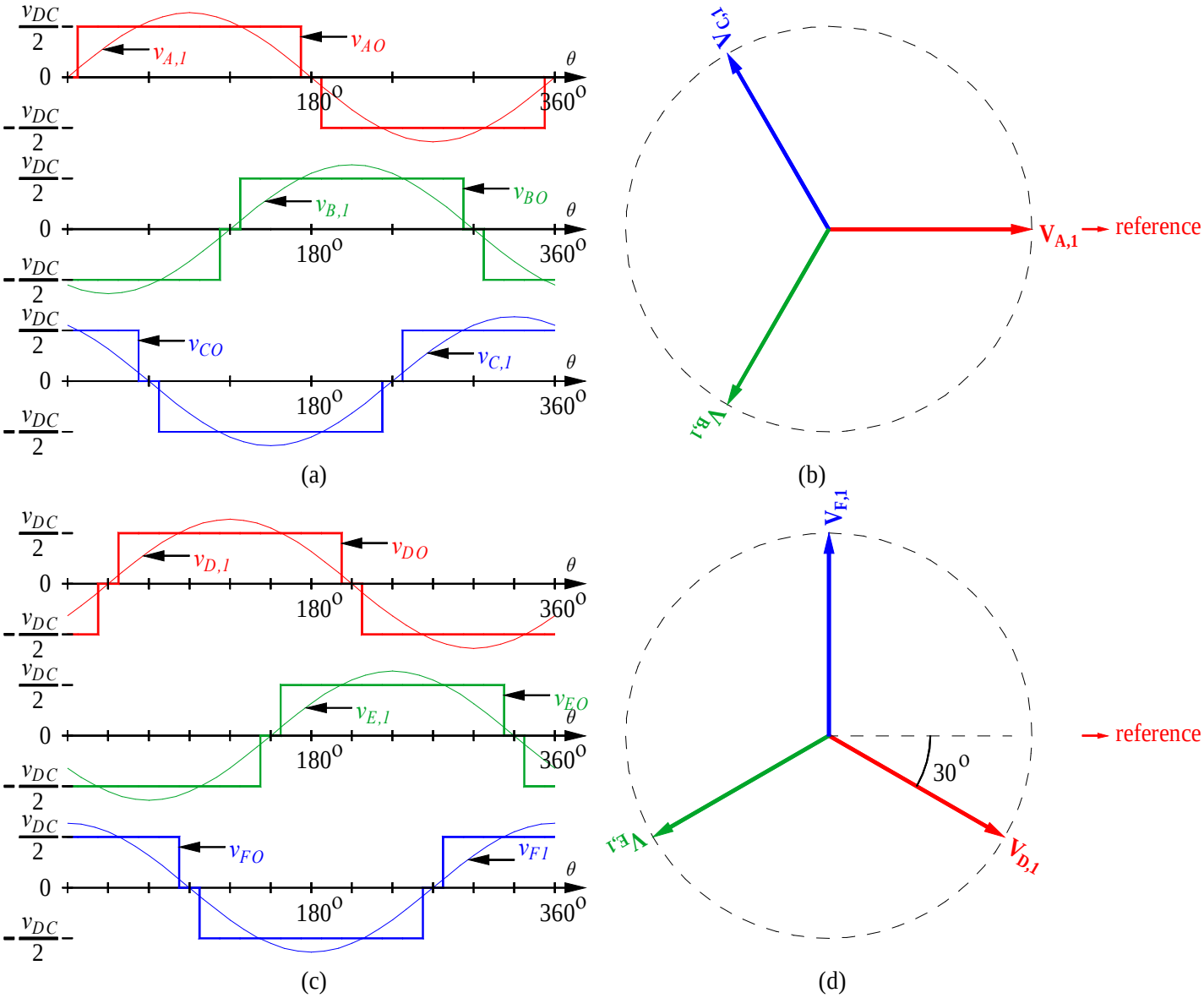


Figure 6-37. Two sets of IPT output voltages and fundamental voltage phasors in a 24-pulse QHN-VSC configuration. (a) Three 120° phase-shifted fundamental voltages and the corresponding quasisquare wave voltages at 0°. (b) Phasor diagram of fundamental voltages in A-B-C IPT output voltage. (c) Three 120° phase-shifted fundamental voltages and the corresponding quasisquare wave voltages at –30°. (d) Phasor diagram of fundamental voltages in D-E-F IPT output voltage.

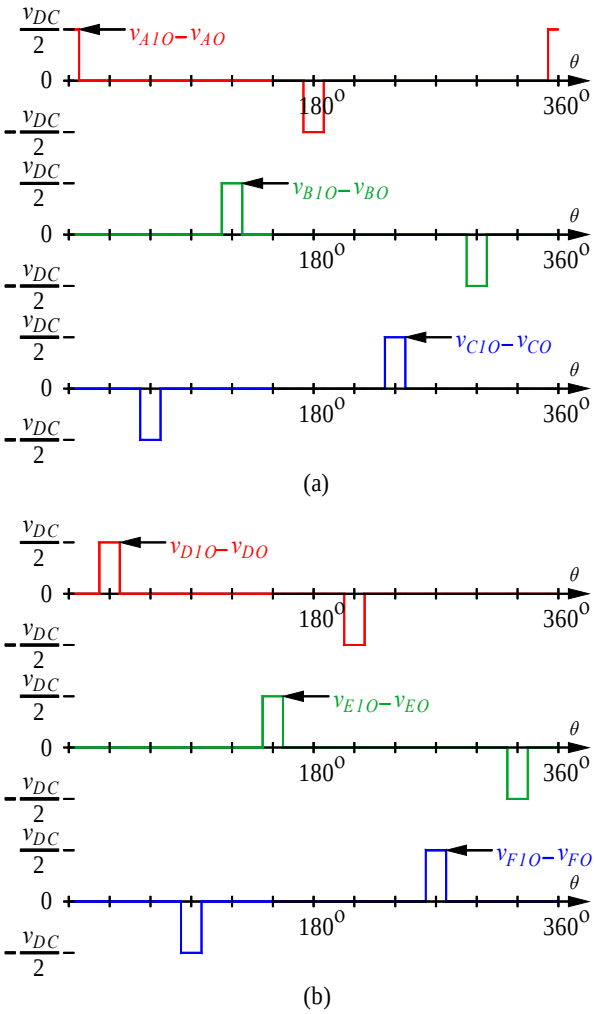


Figure 6-38. Interphase transformer voltages.

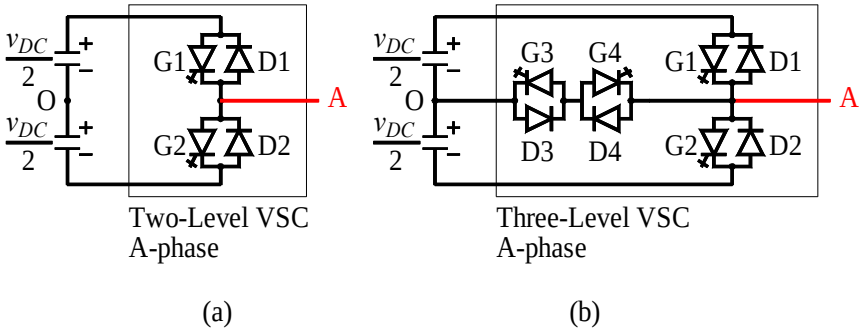


Figure 6-39. Single phase DC-to-AC VSC with (a) two levels and (b) three levels.

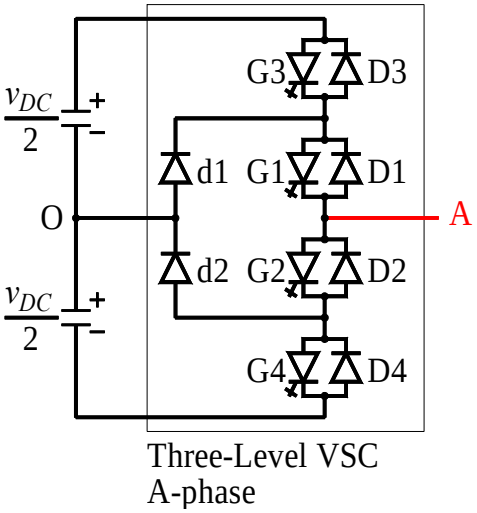


Figure 6-40. Single phase DC-to-AC VSC with three levels.

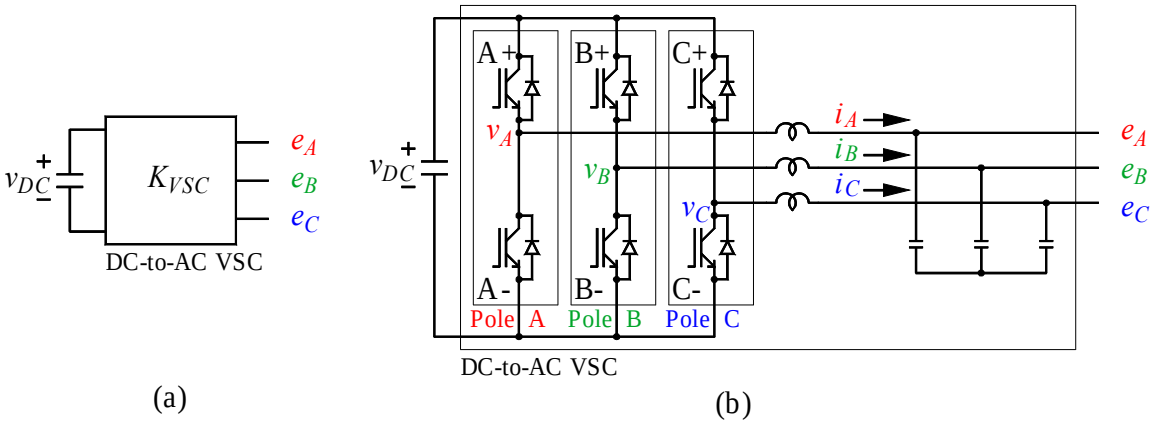


Figure 6-41. DC-to-AC VSC operated with the PWM technique.

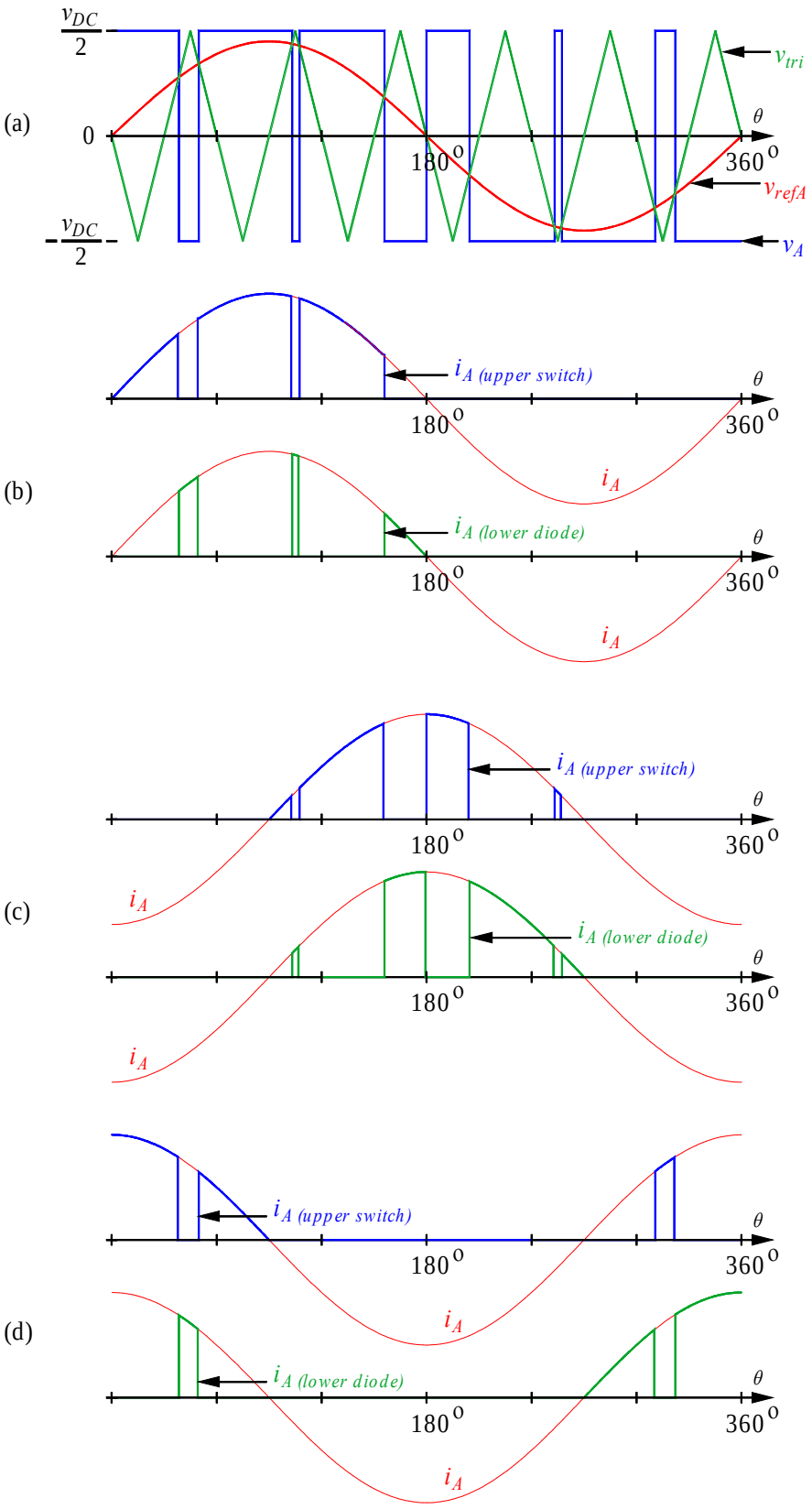


Figure 6-42. (a) Carrier voltage, pole A reference voltage, and pole A output voltage. (b) Currents through upper switch, lower diode, and pole A for unity power factor. (c) Currents through upper switch, lower diode, and pole A for zero power factor lagging. (d) Currents through upper switch, lower diode, and pole A for zero power factor leading.

CHAPTER 7

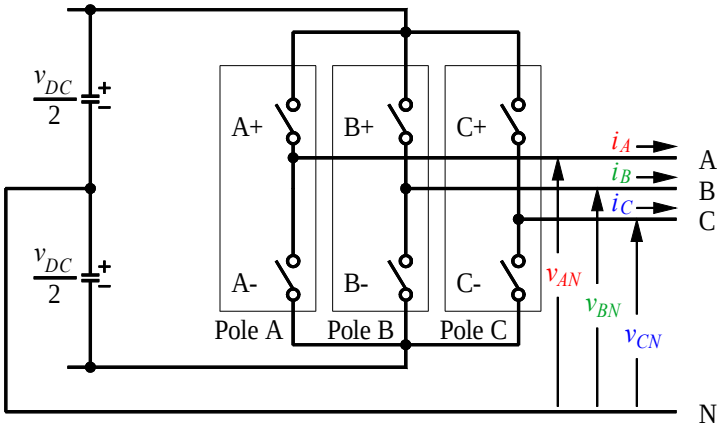


Figure 7-1. Three-phase, six-pulse VSC with two-level poles.

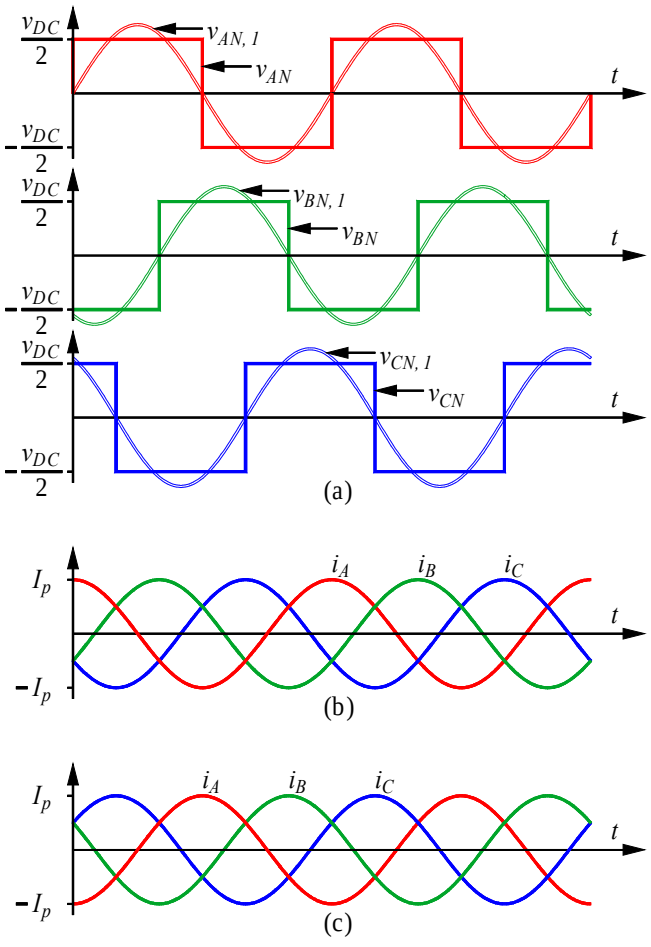


Figure 7-2. (a) Pole output to neutral square wave voltages with their fundamental components. (b) Pole output currents during absorbing VARs. (c) Pole output currents during generating VARs.

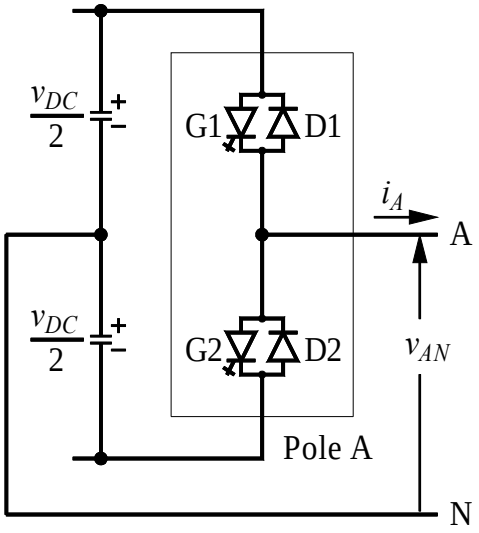


Figure 7-3. Realization of a two-level pole A with GTOs and antiparallel diodes.

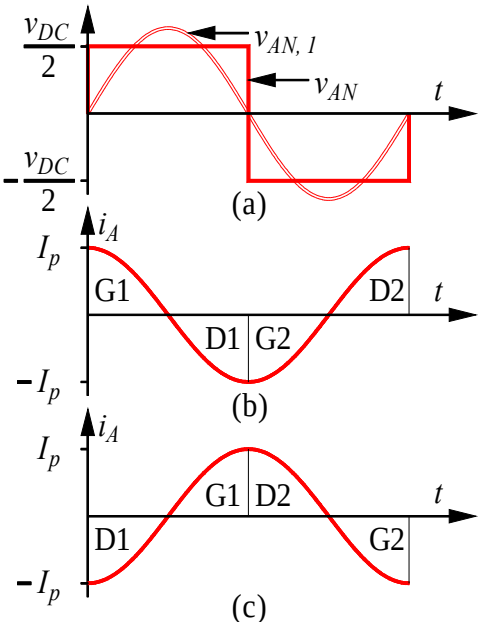


Figure 7-4. (a) Pole A to neutral voltage and its fundamental component. (b) Pole A current during absorbing VARs. (c) Pole A current during generating VARs.

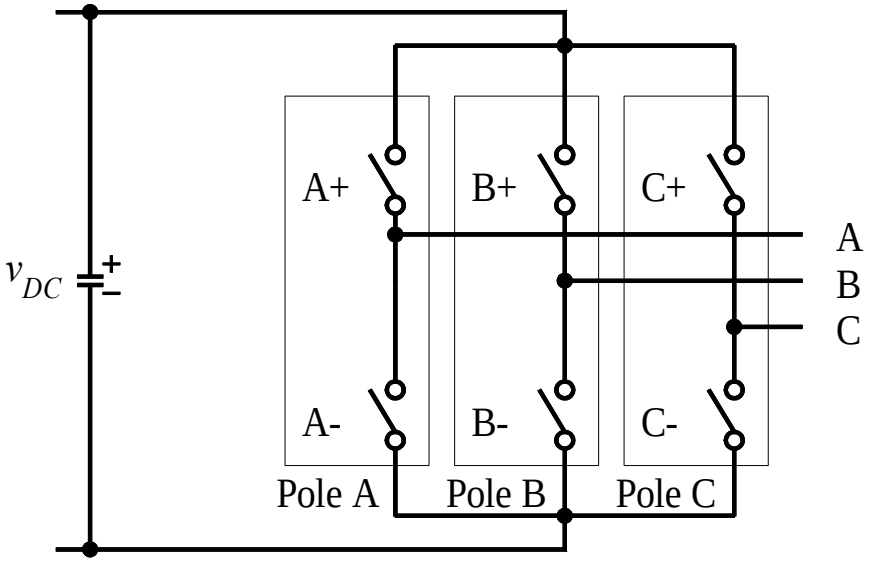


Figure 7-5 Three-phase, six-pulse VSC and its poles.

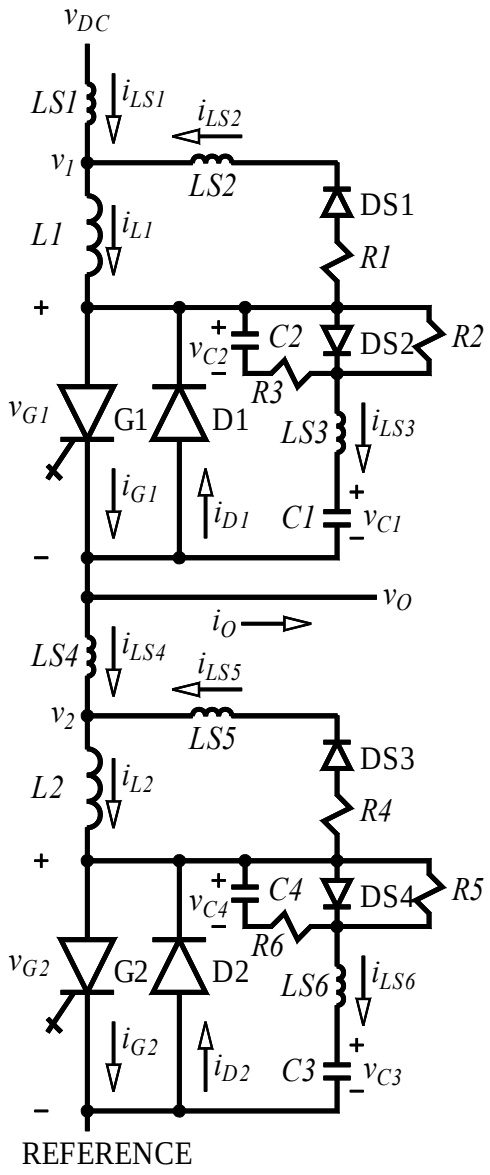
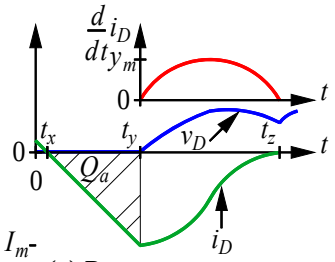
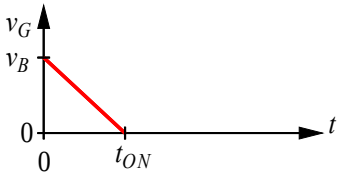


Figure 7-6. Details of a two-level pole circuit.



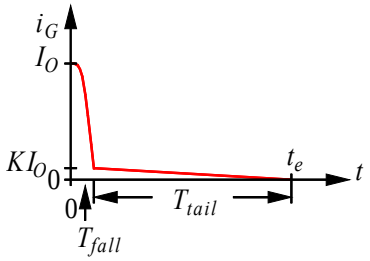
I_m = peak reverse current
y_m = slope of i_D at $t_y + T$
T = $(t_z - t_y)/2$

(a) Reverse recovery model of a diode



v_D = forward blocking voltage
t_{ON} = on time

(b) Turn on model of a GTO



I_O = forward carrying current
T_{fall} = fall time
T_{tail} = tail time

(c) Turn off model of a GTO

Figure 7-7. Switching characteristics of a diode and a GTO.

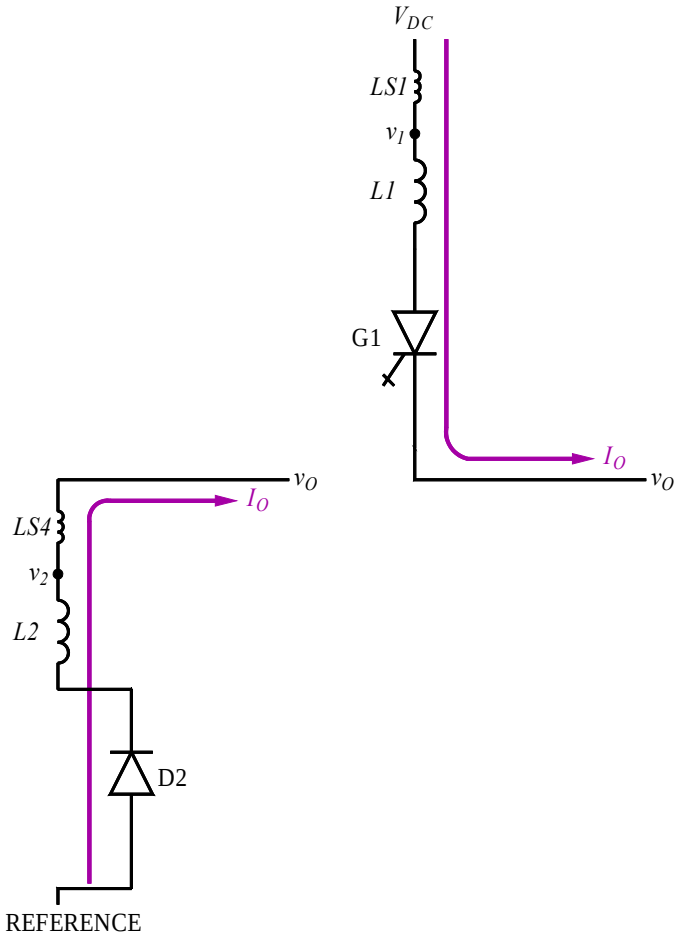


Figure 7-8. Commutation from D2 to G1.

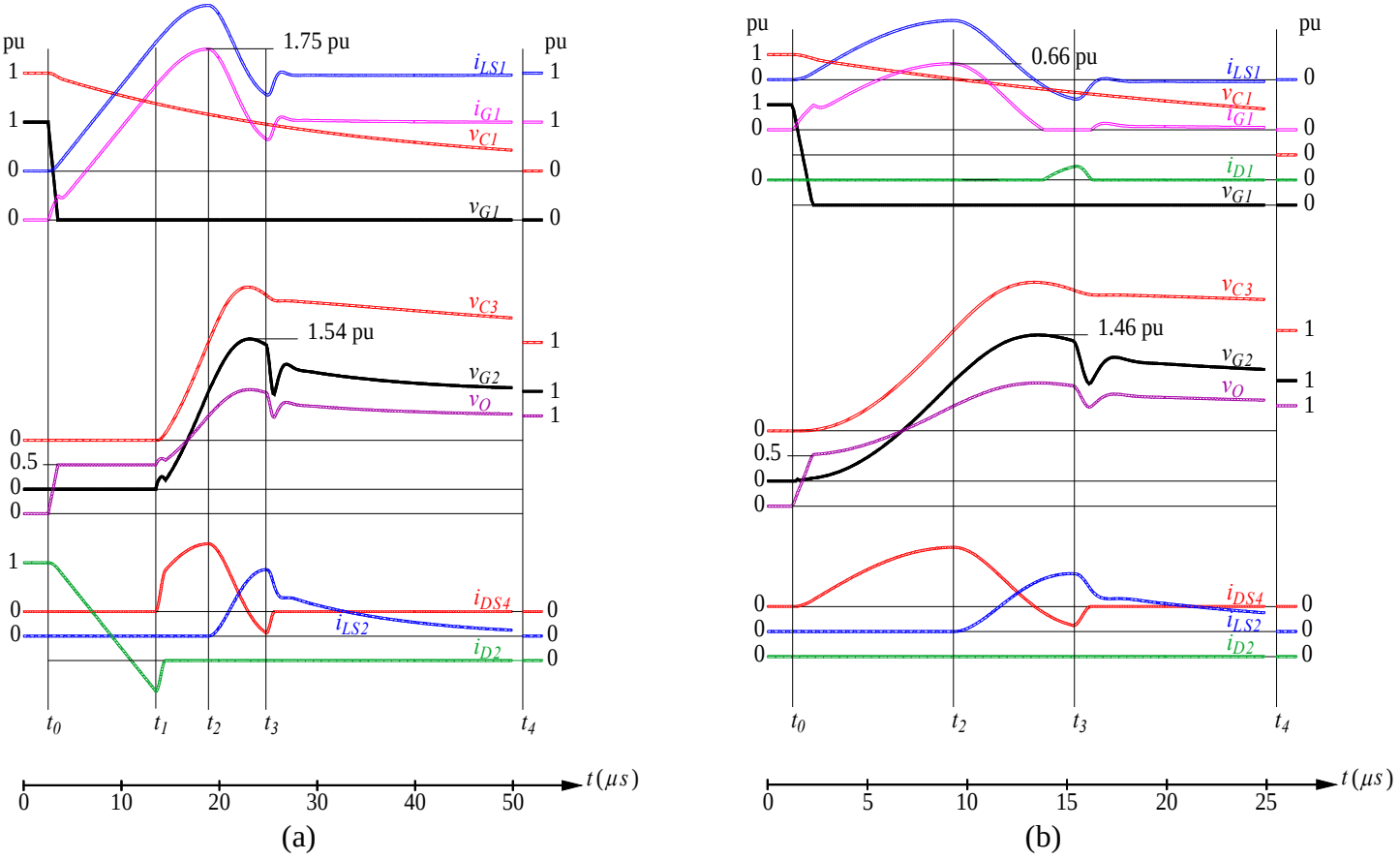


Figure 7-9. Transients from commutation from D2 to G1 under (a) full load and (b) no load conditions.

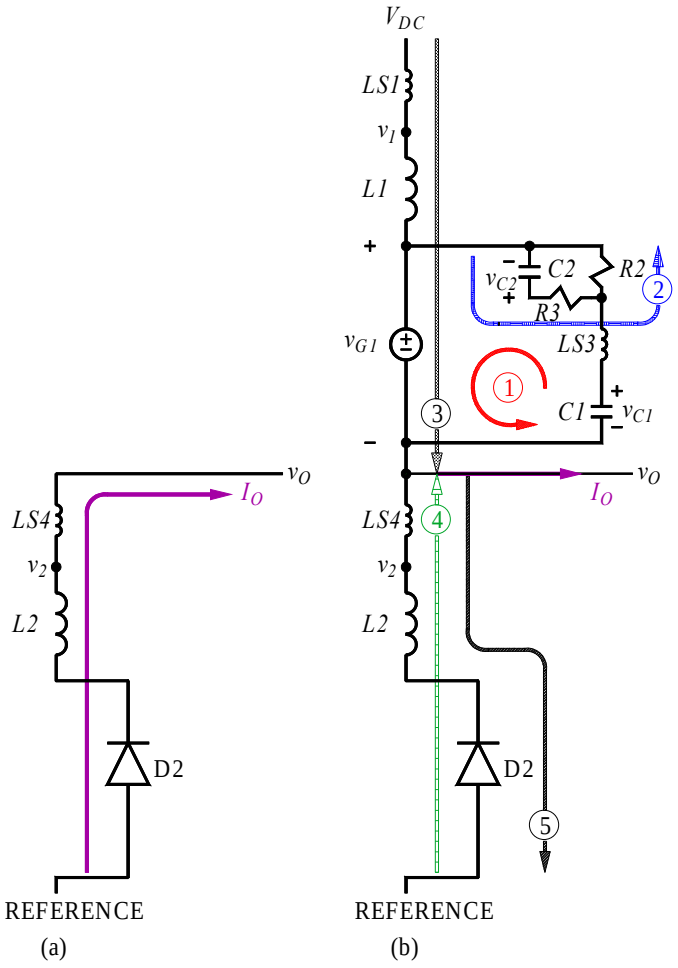


Figure 7-10(a, b). Transients from commutation from D2 to G1 during (a) $t<t_0$ and (b) $t_0<=t<t_1$.

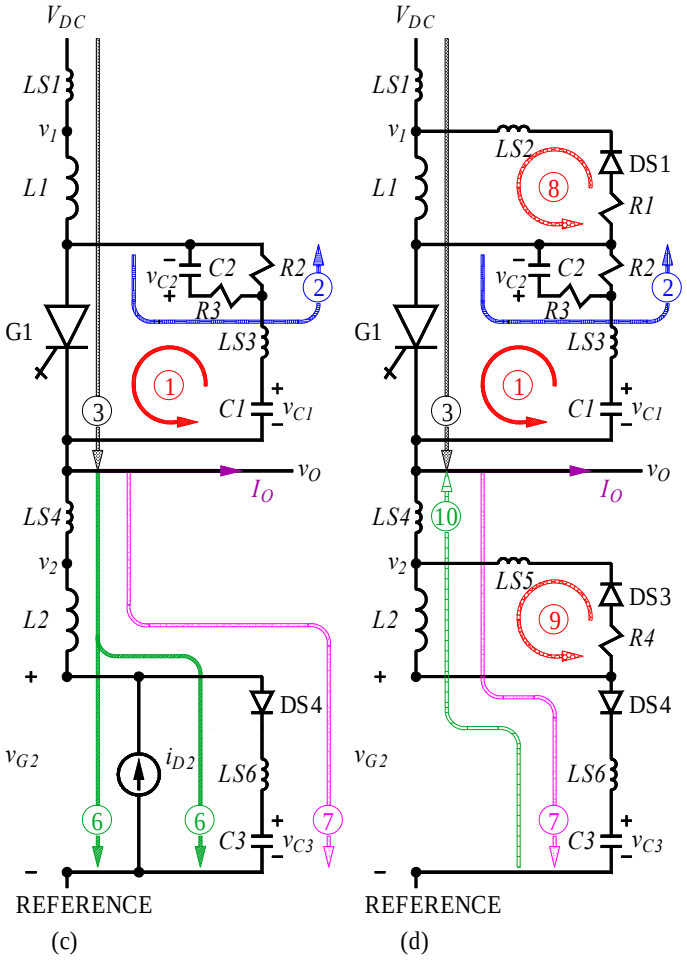


Figure 7-10(c, d). Transients from commutation from D2 to G1 during (c) $t_1<=t<t_2$ and (d) $t_2<=t<t_3$.

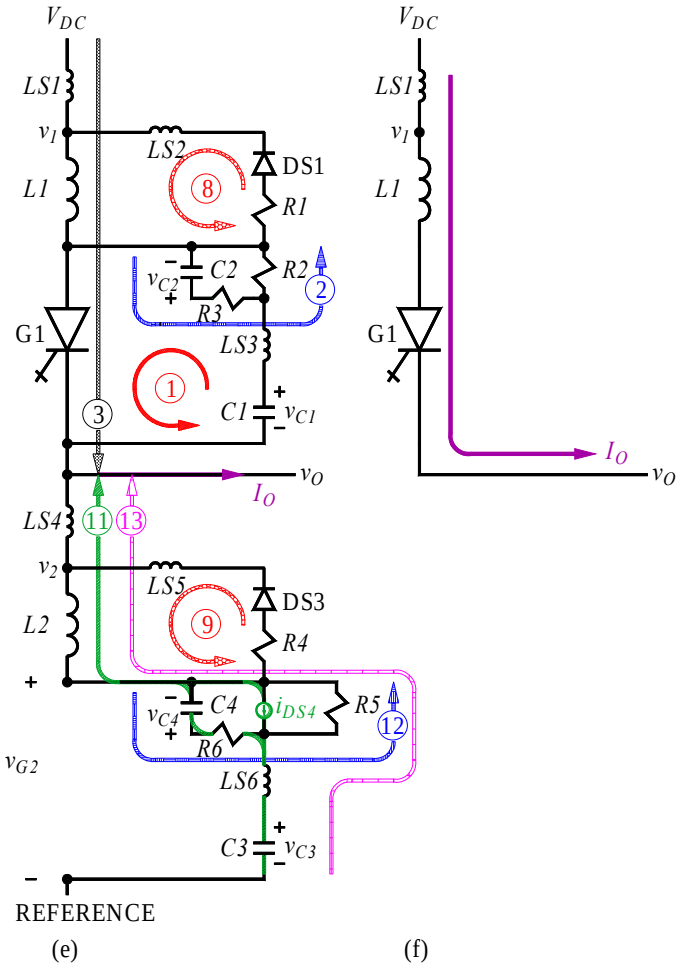


Figure 7-10(e, f). Transients from commutation from D2 to G1 during (e) $t_3<=t<t_4$, and (f) $t_4<=t$.

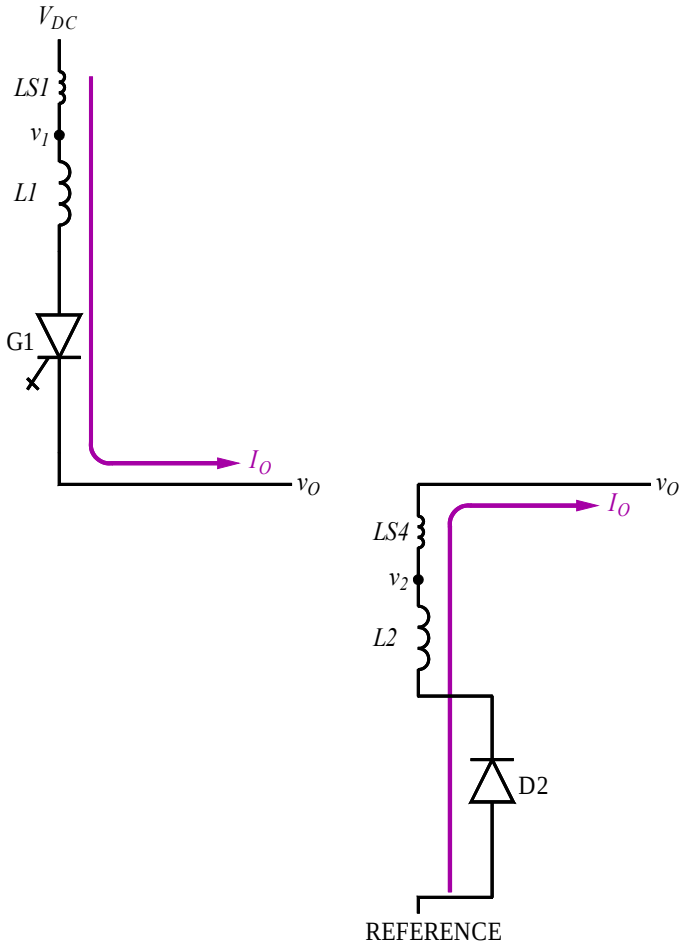


Figure 7-11. Commutation from G1 to G2 to D2.

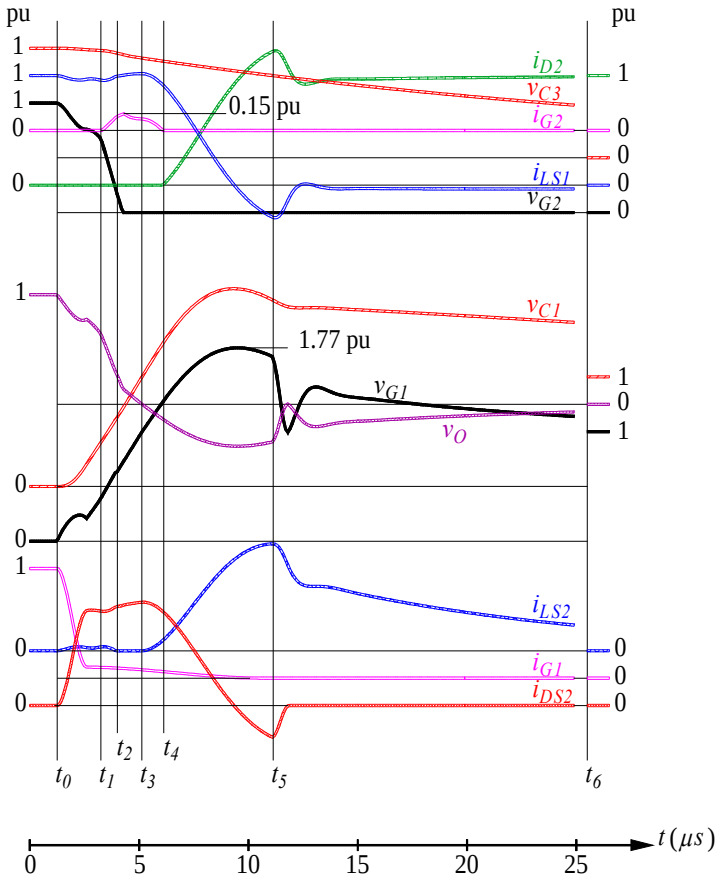


Figure 7-12. Commutation from G1 to G2 to D2 under full load with t_{delay} = 2 μs.

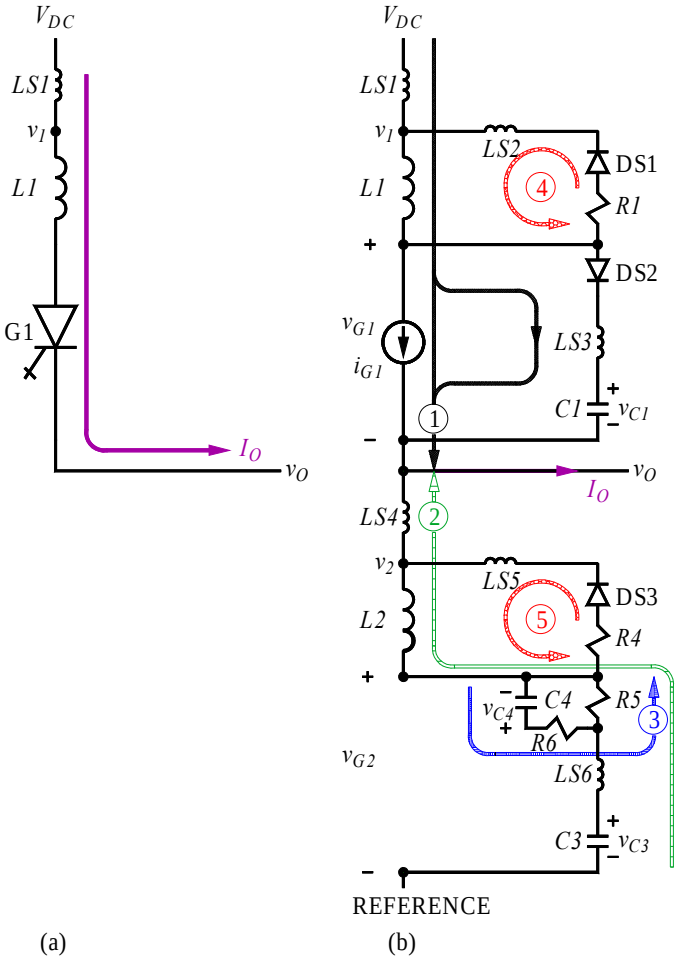


Figure 7-13(a, b). Commutation from G1 to G2 to D2 under full load with t_{delay} = 2 μs during (a) $t<t_0$, and (b) $t_0<=t<t_1$.

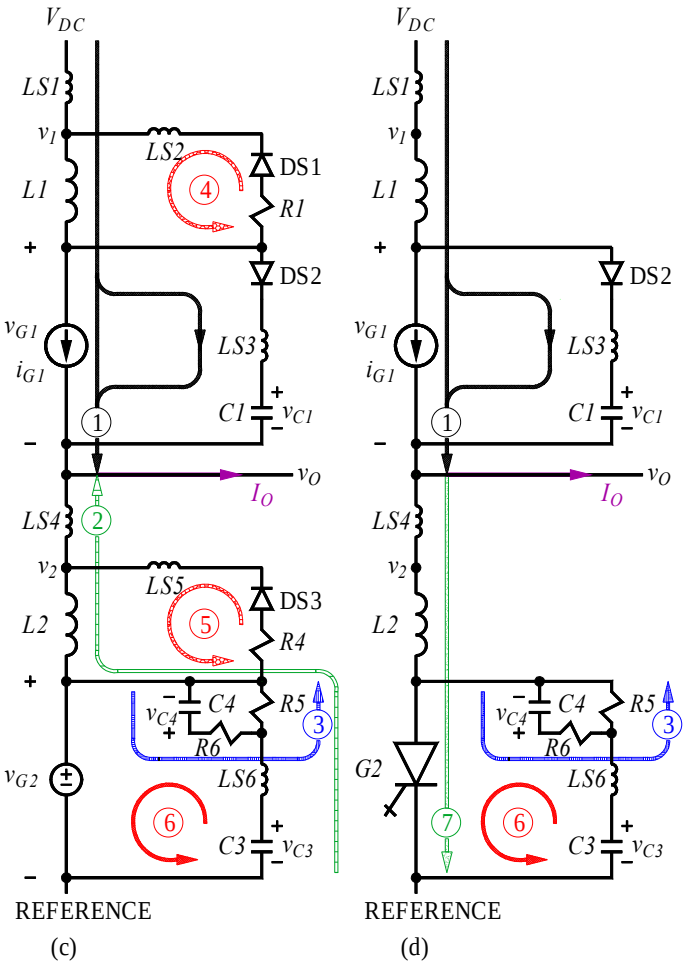


Figure 7-13(c, d). Commutation from G1 to G2 to D2 under full load with t_{delay} = 2 μs during (c) $t_1<=t<t_2$, and (d) $t_2<=t<t_3$.

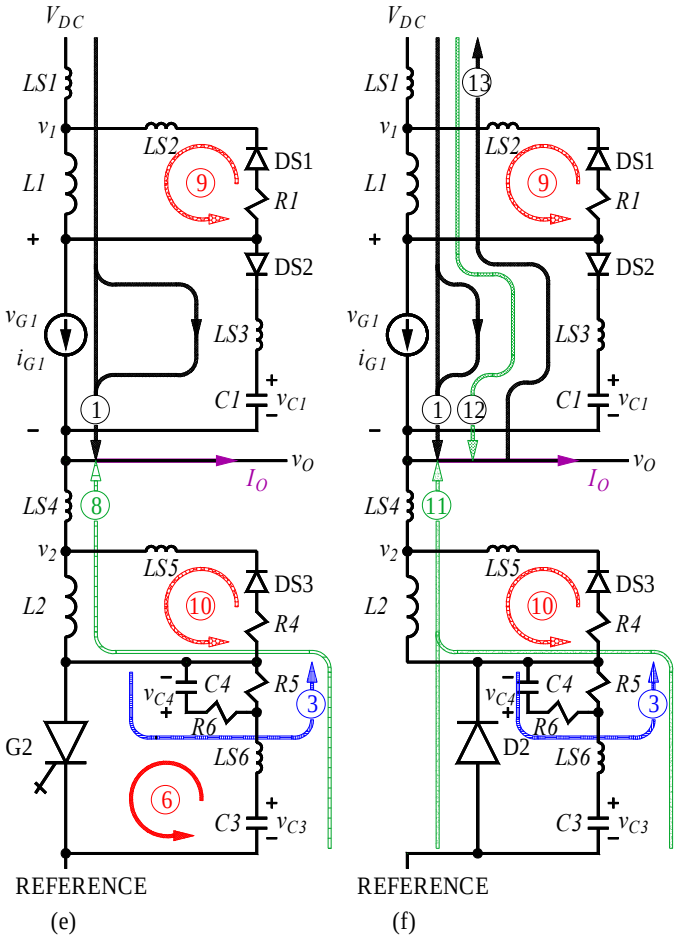


Figure 7-13(e, f). Commutation from G1 to G2 to D2 under full load with t_{delay} = 2 μs during (e) t_3<=t<t_4, and (f) t_4<=t<t_5.

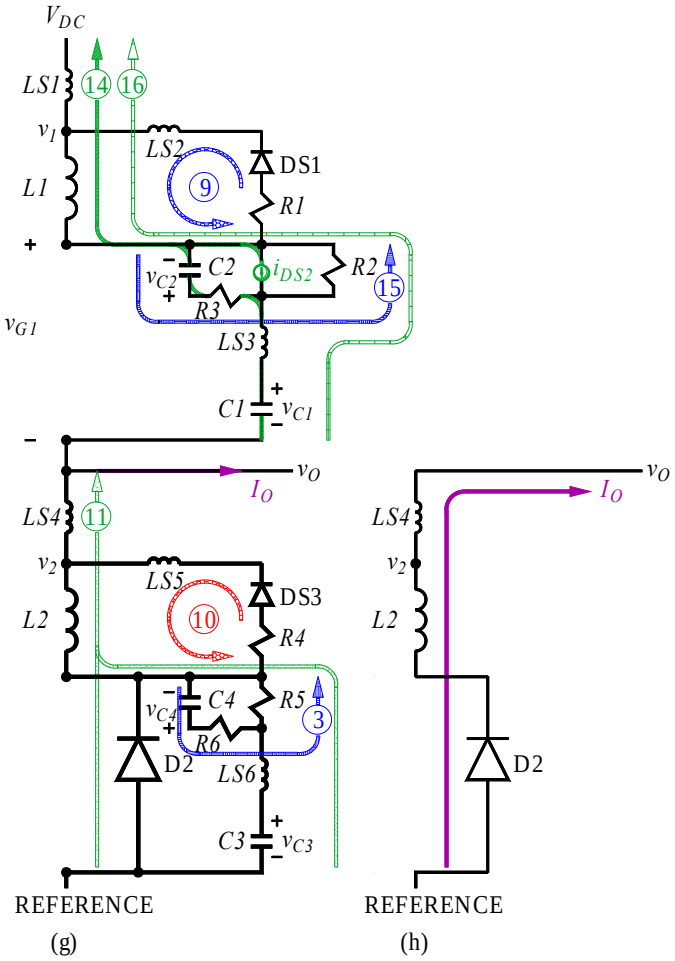


Figure 7-13(g, h). Commutation from G1 to G2 to D2 under full load with t_{delay} = 2 μs during (g) $t_5 <= t < t_6$, and (h) $t_6 <= t$.

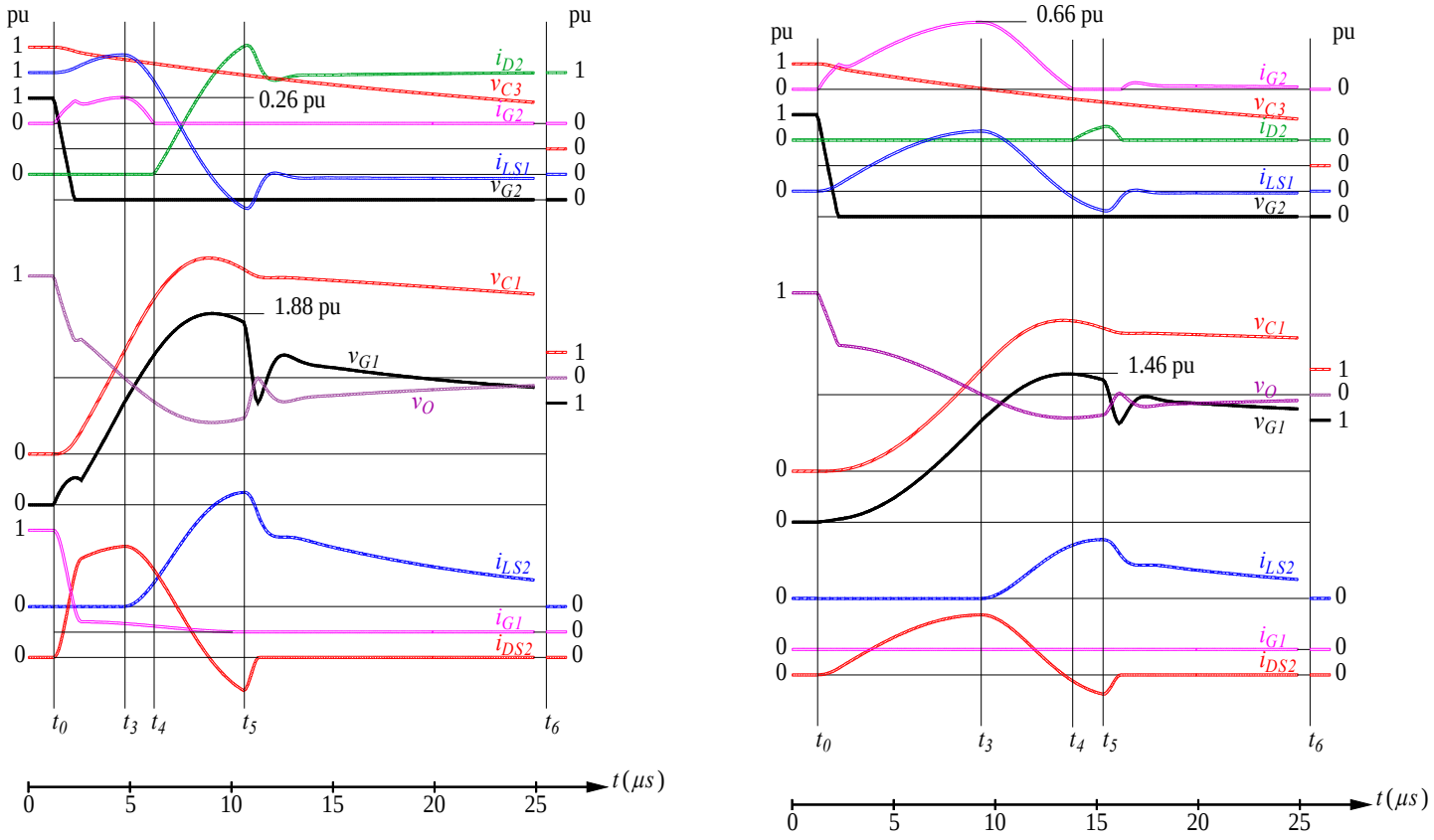


Figure 7-14. Transients from commutation from G1 to G2 to D2 under (a) full load and (b) no load conditions $t_{delay} = 0$.

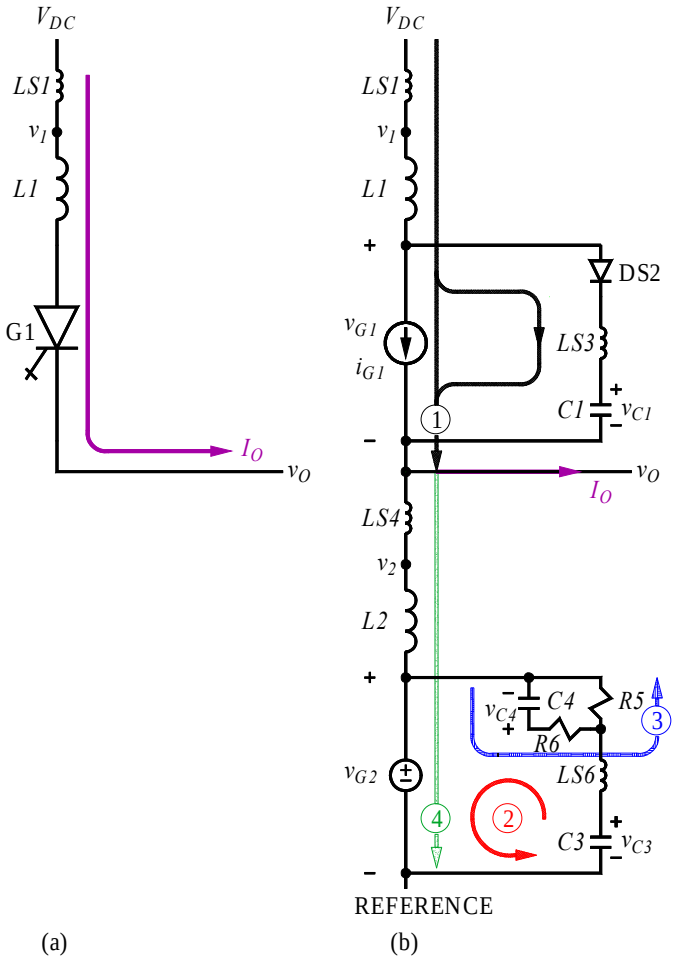


Figure 7-15. Commutation from G1 to G2 to D2 with t_{delay} = 0 μs during (a) $t<t_0$, and (b) $t_0<=t<t_3$.

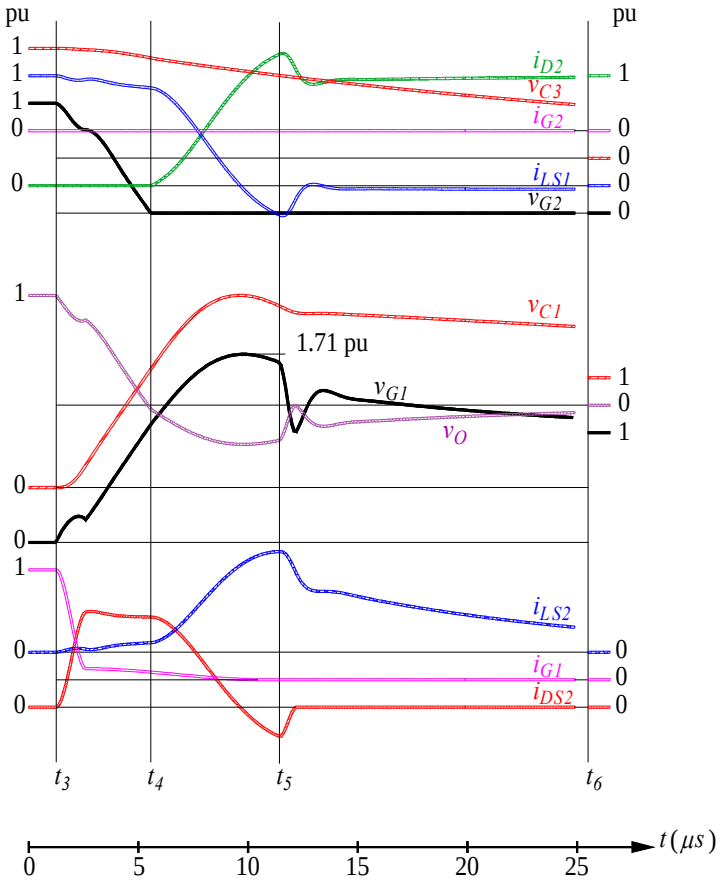


Figure 7-16. Commutation from G1 to G2 to D2 under full load with t_{delay} = 20 μs.

CHAPTER 8

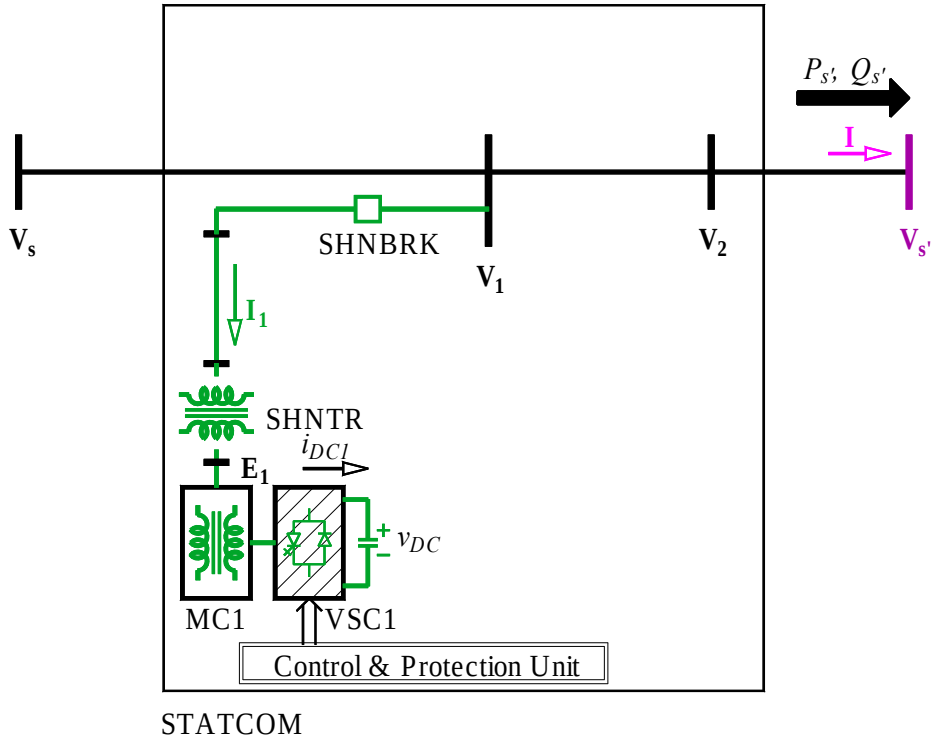


Figure 8-1. Static synchronous compensator (STATCOM).

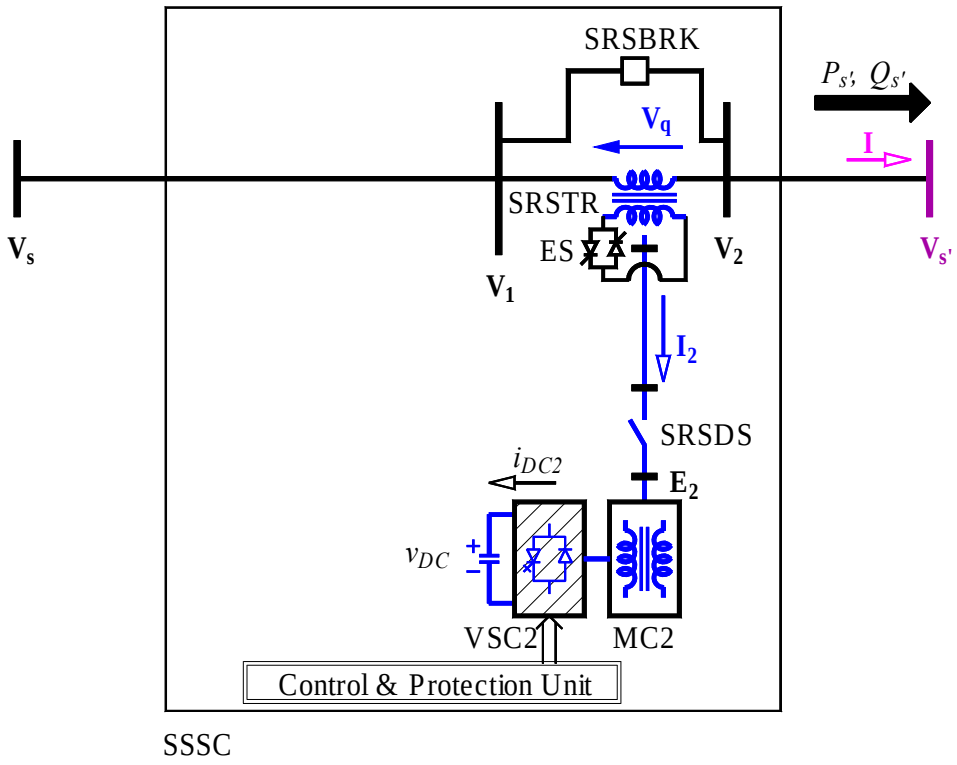


Figure 8-2. Static synchronous series compensator (SSSC).

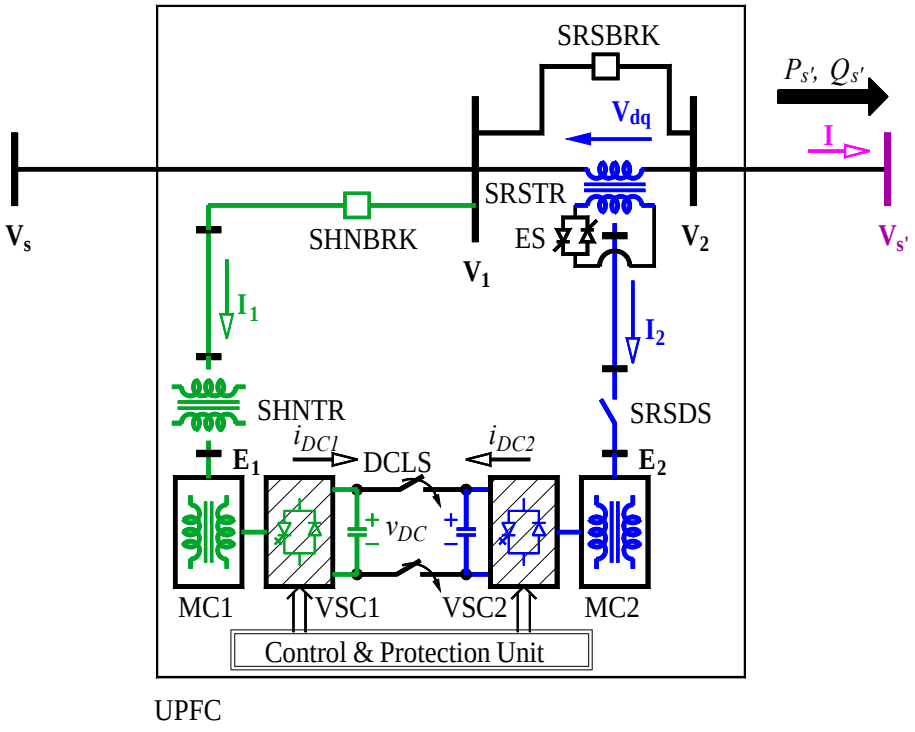


Figure 8-3. Unified power flow controller (UPFC).

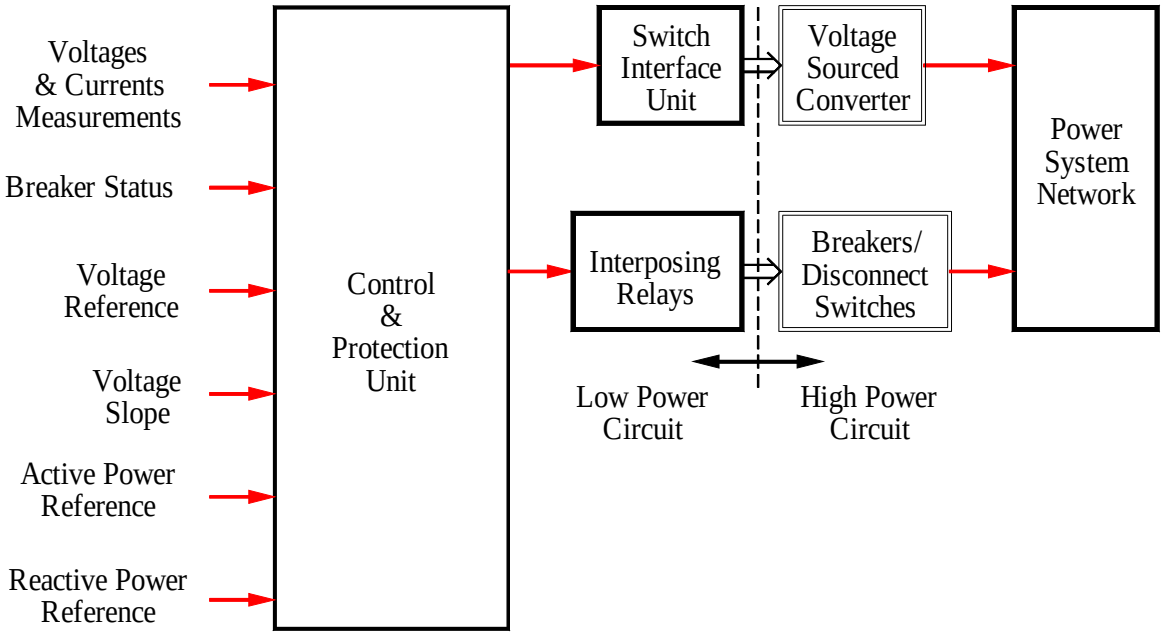


Figure 8-4. Modeling structure of a FACTS controller.

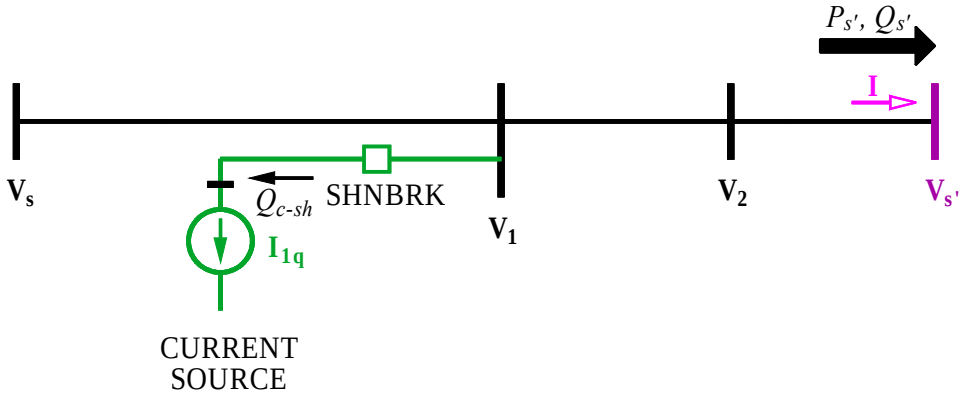


Figure 8-5. Injection of shunt reactive current into the transmission line.

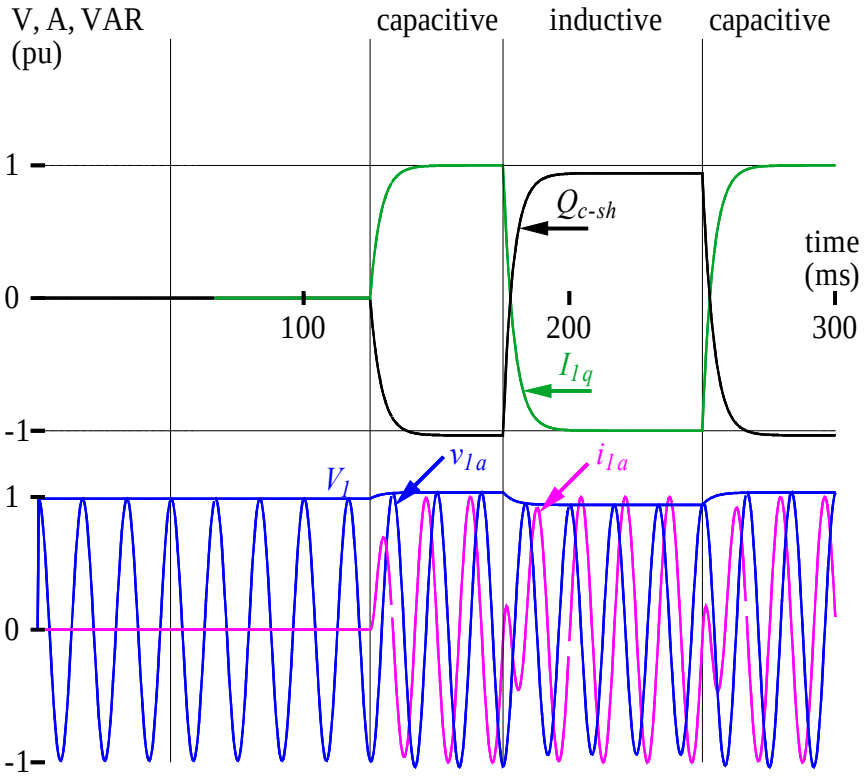


Figure 8-6. Exchanged reactive power and the resulting voltages and currents due to an injection of shunt current into the transmission line.

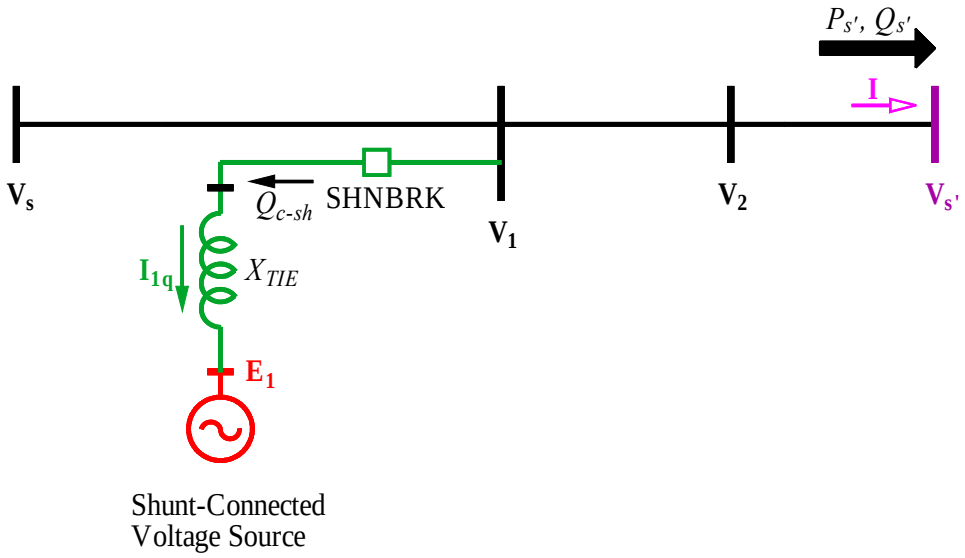


Figure 8-7. Transmission line voltage control using a shunt-connected compensating voltage.

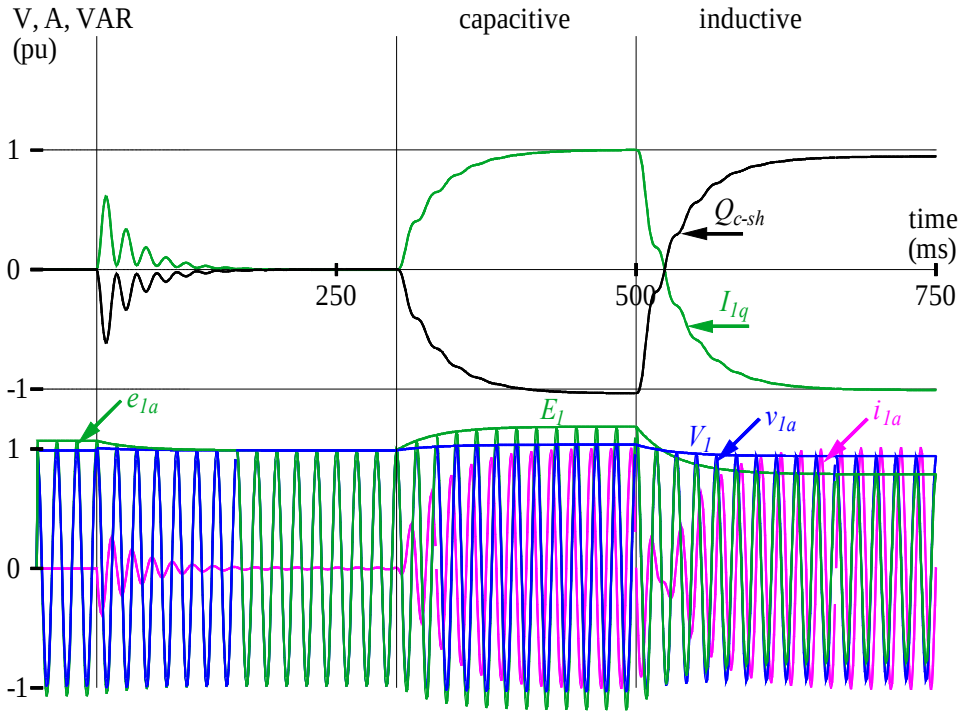


Figure 8-8. Exchanged reactive power and the resulting voltages and currents due to a shunt-connected voltage into the transmission line through a tie reactance.

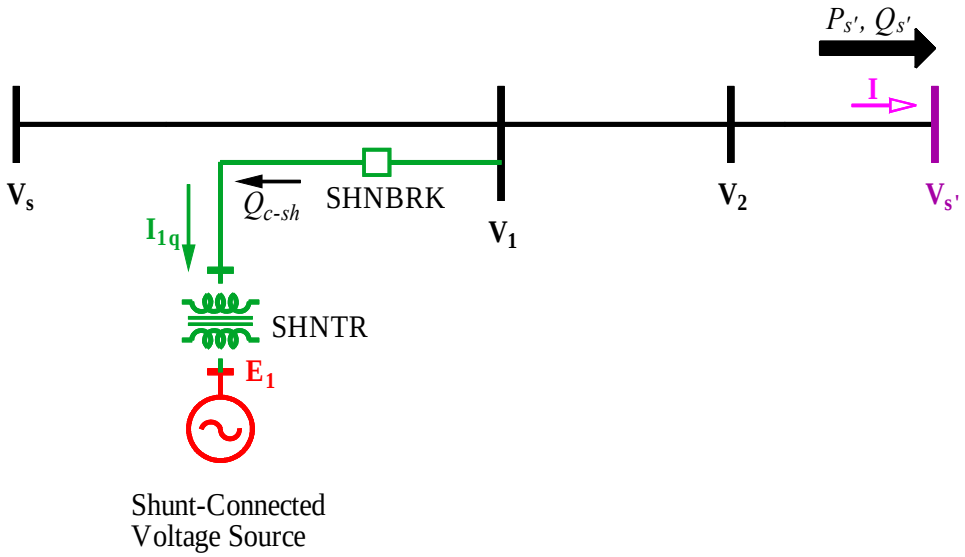


Figure 8-9. Transmission line voltage control using a shunt-connected compensating voltage through a coupling transformer.

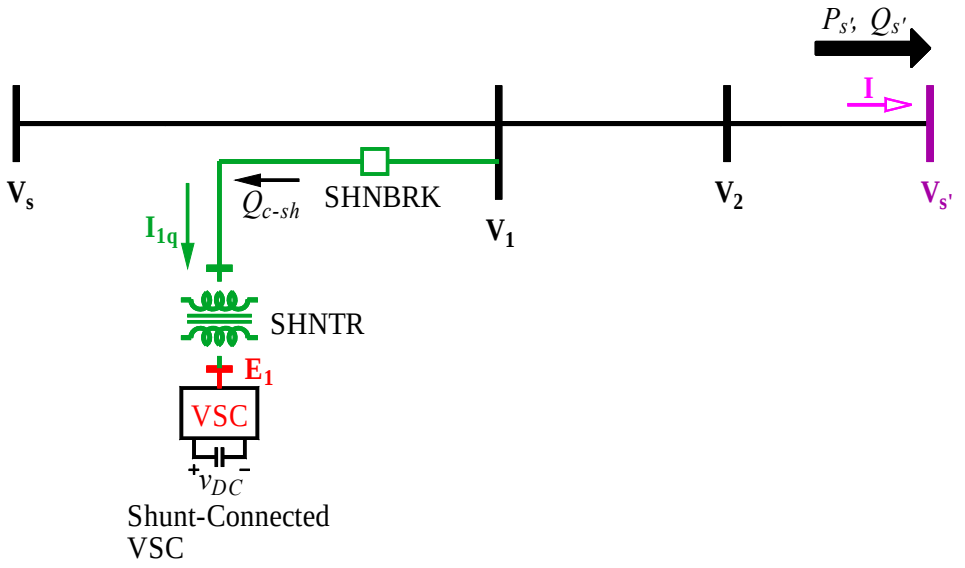


Figure 8-10. Transmission line voltage control using a shunt-connected VSC.

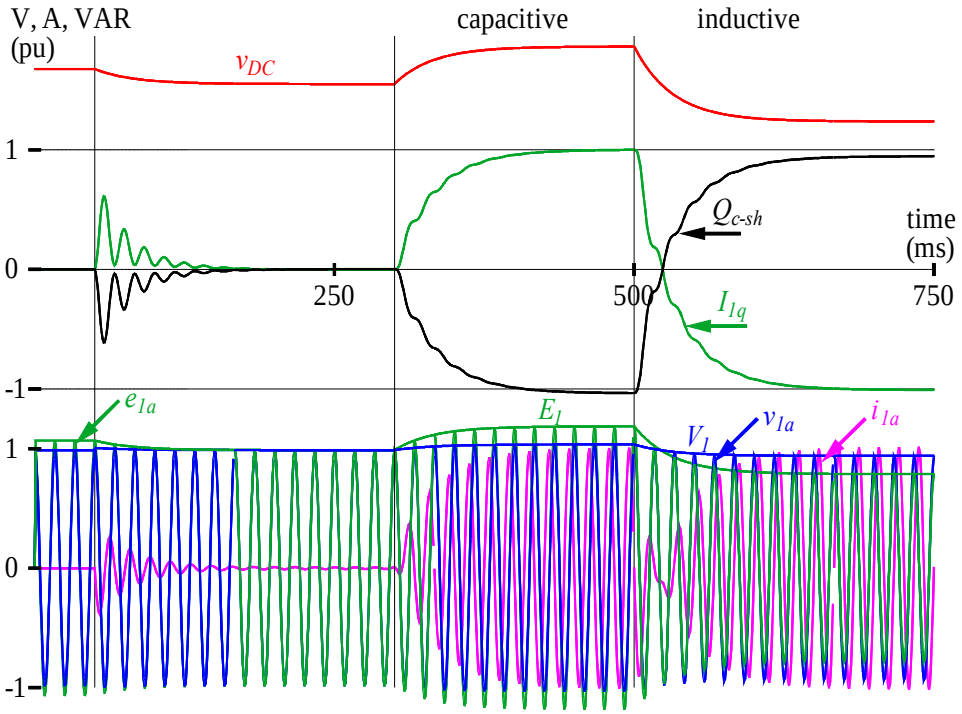


Figure 8-11. Exchanged reactive power and the resulting voltages and currents due to a shunt-connected VSC into the transmission line through a tie reactance.

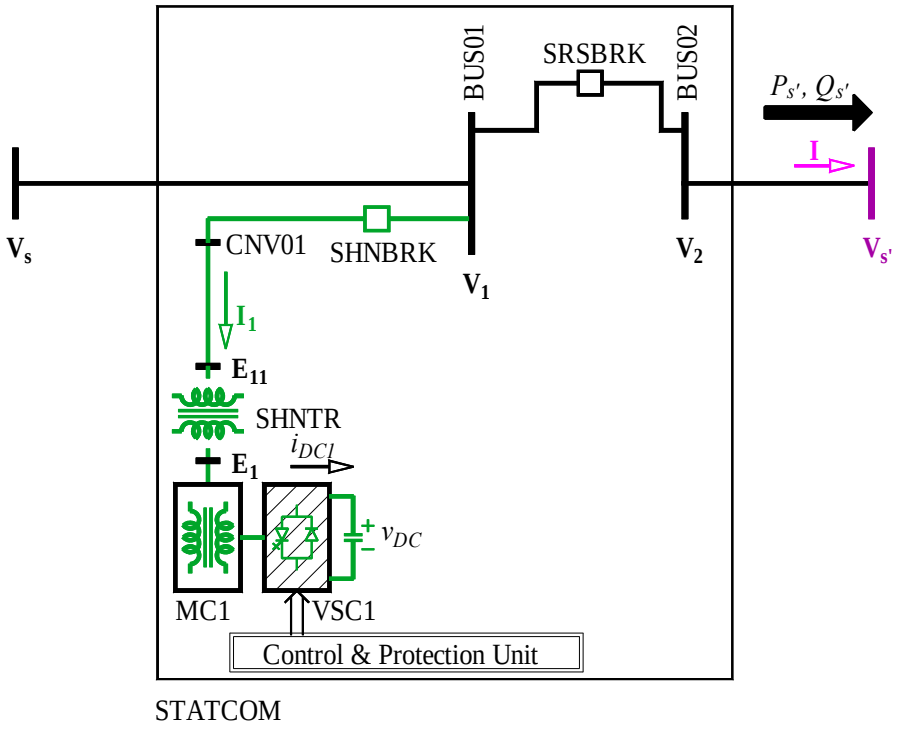


Figure 8-12. STATCOM model in EMTP.

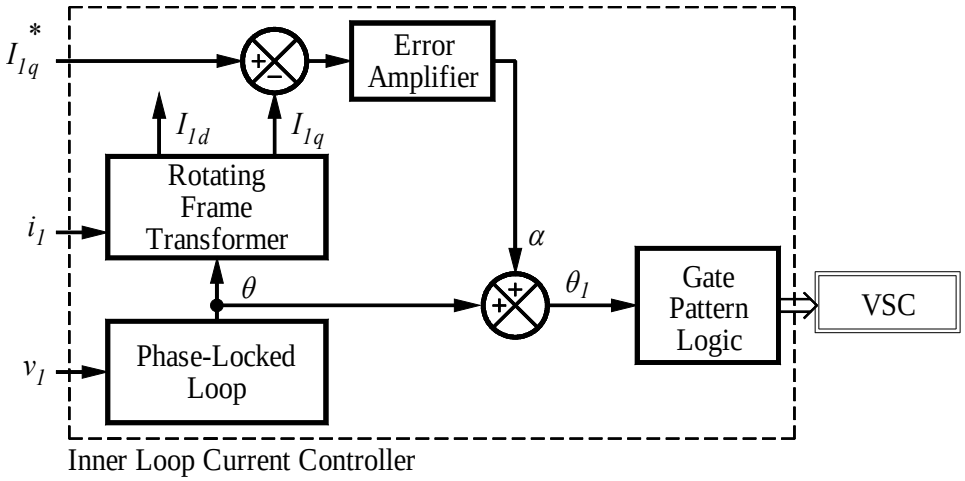


Figure 8-13. Reactive current control block diagram of the STATCOM.

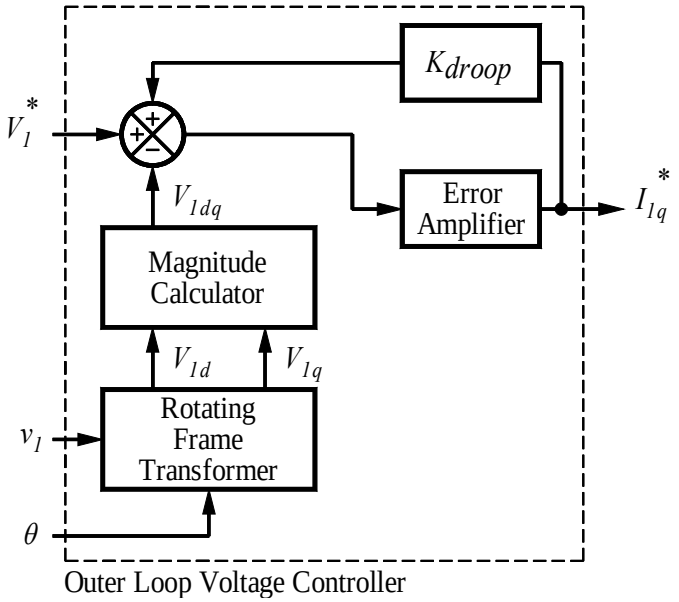


Figure 8-14. Voltage control block diagram of the STATCOM.

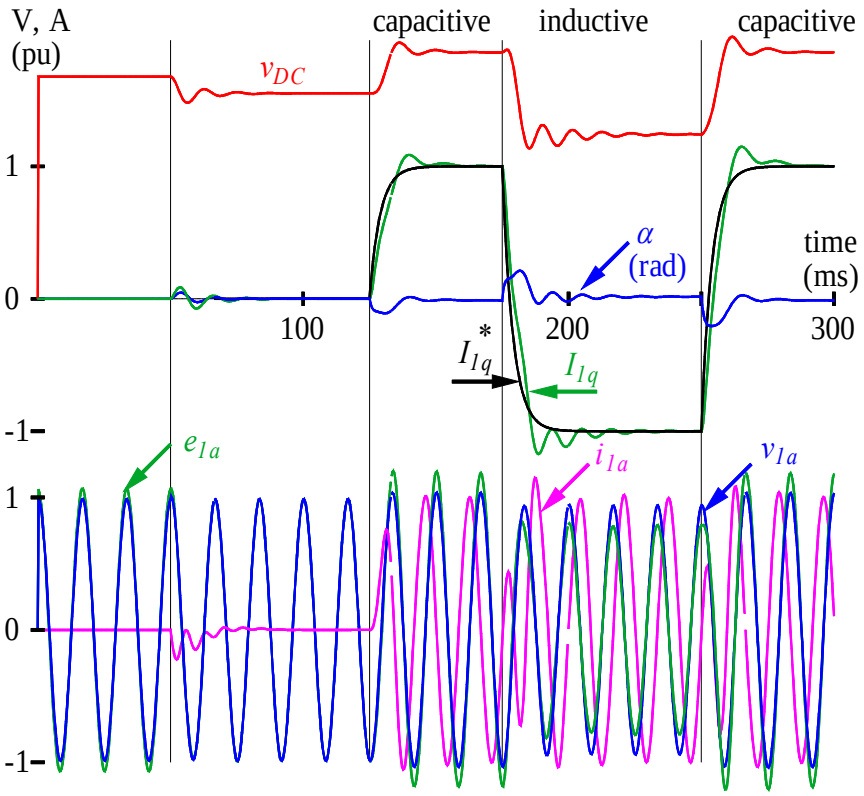


Figure 8-15. Performance of the STATCOM with an infinite pulse VSC operating in a reactive current control mode.

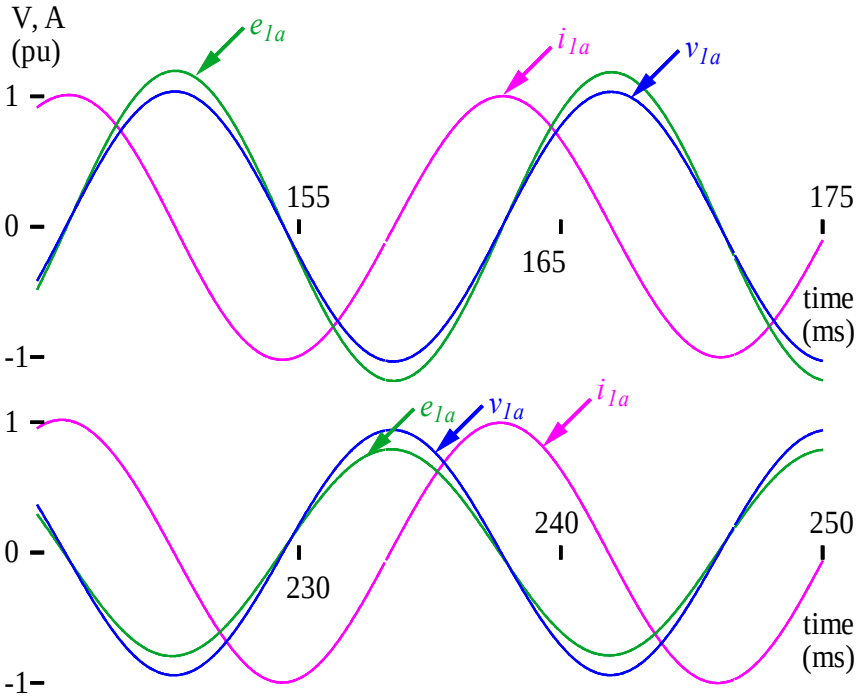


Figure 8-16. Waveforms of the STATCOM with an infinite pulse VSC operating in a reactive current control mode.

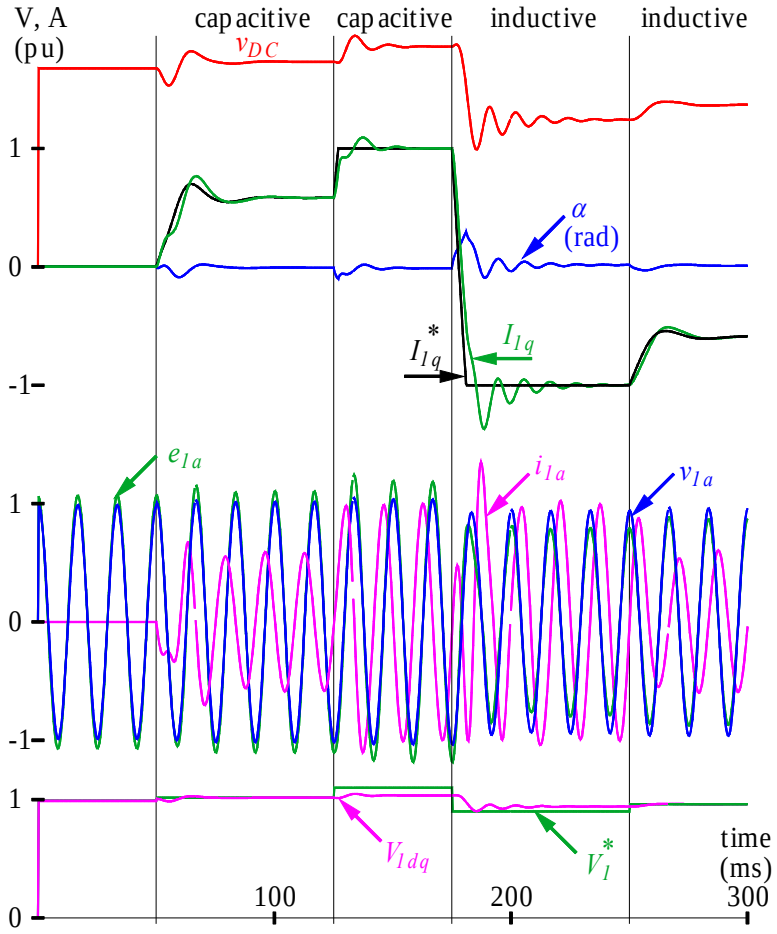


Figure 8-17. Performance of the STATCOM with an infinite pulse VSC operating in a voltage control mode.

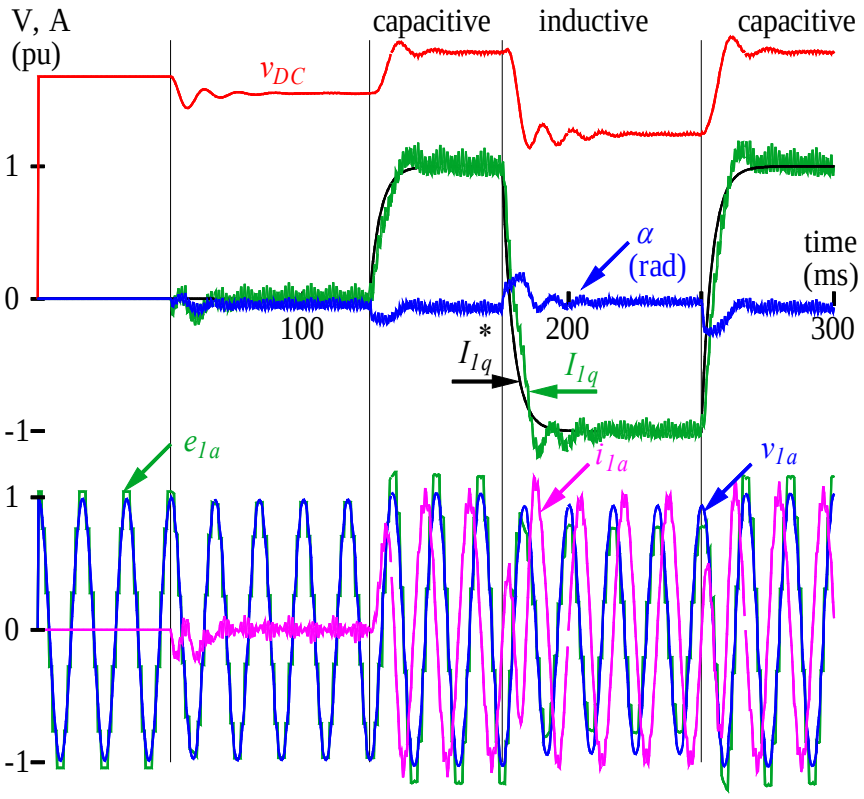


Figure 8-18. Performance of the STATCOM with a 12-pulse HN-VSC operating in a reactive current control mode.

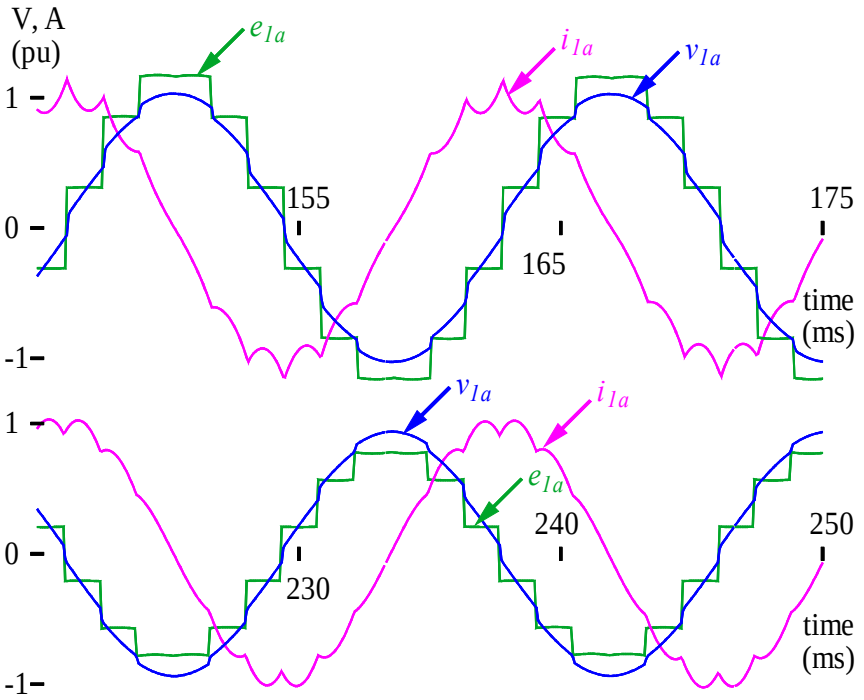


Figure 8-19. Waveforms of the STATCOM with a 12-pulse HN-VSC operating in a reactive current control mode.

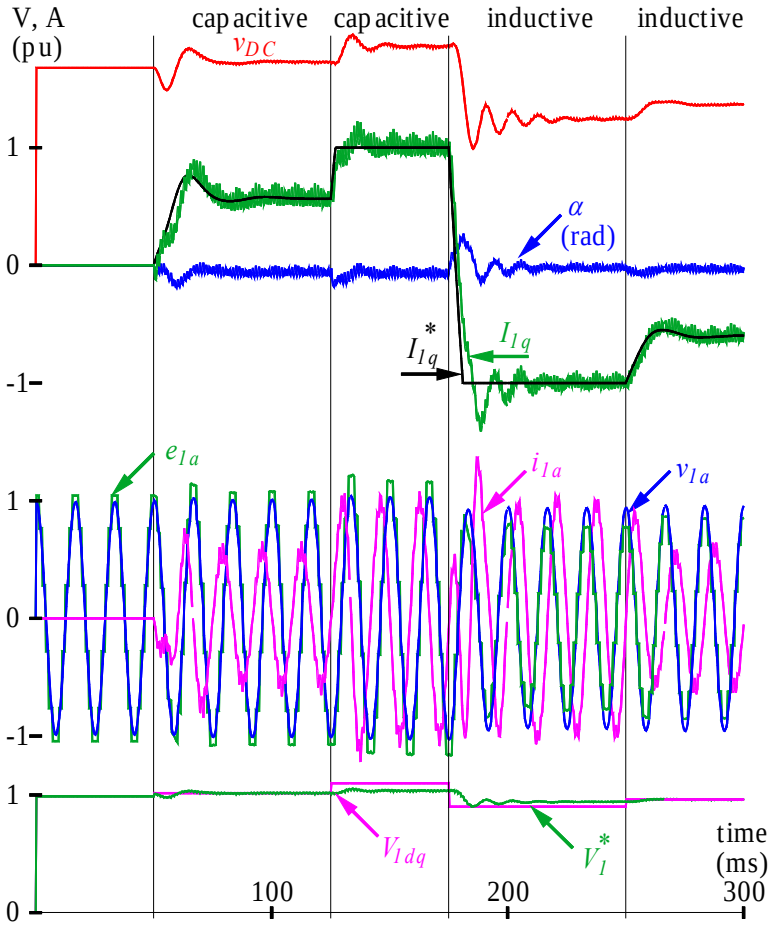


Figure 8-20. Performance of the STATCOM with a 12-pulse HN-VSC operating in a voltage control mode.

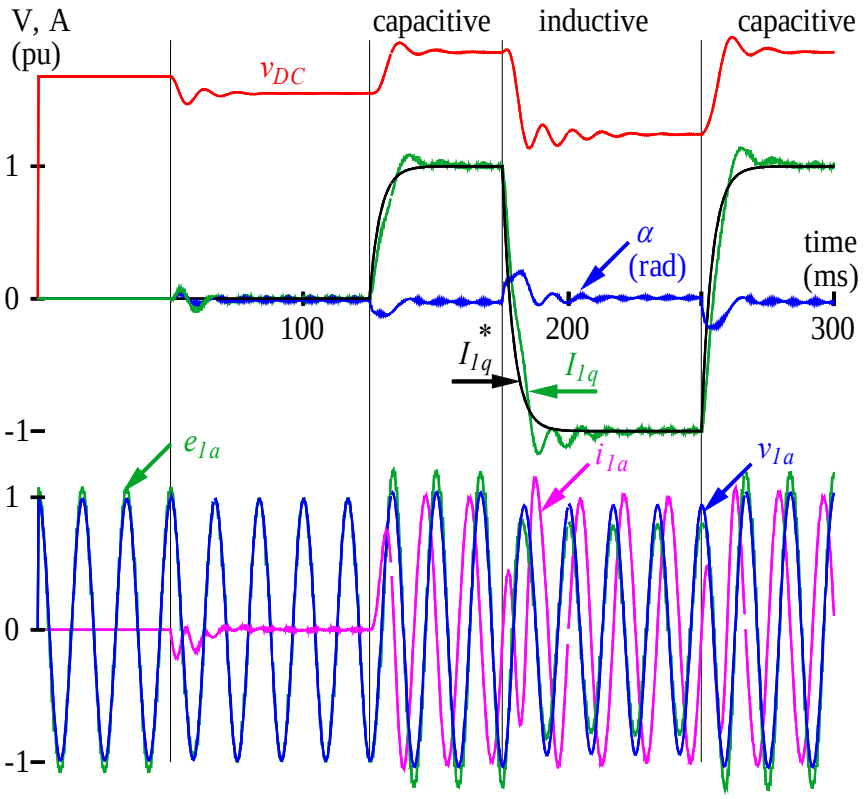


Figure 8-21. Performance of the STATCOM with a 24-pulse HN-VSC operating in a reactive current control mode.

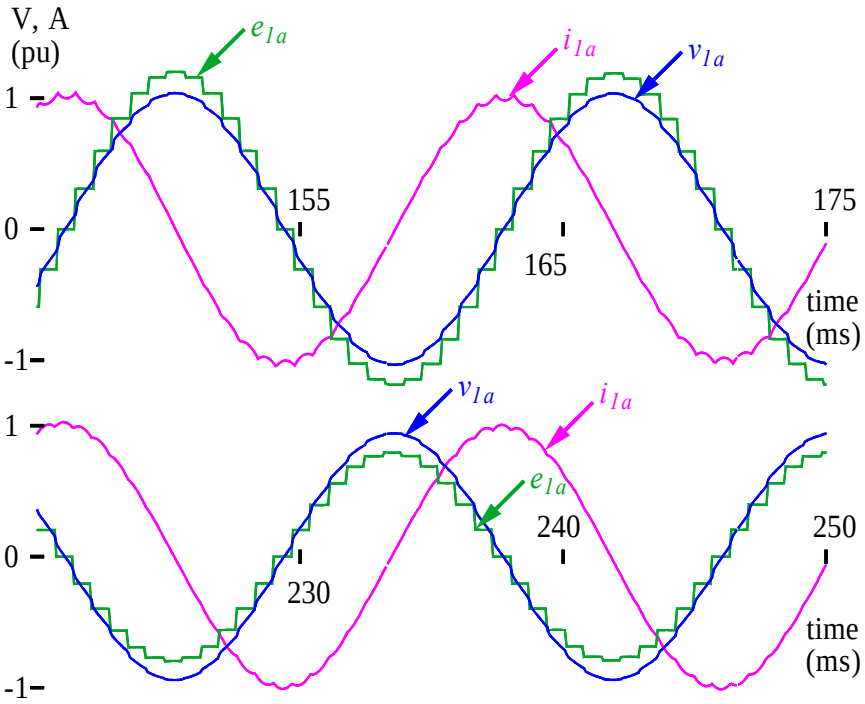


Figure 8-22. Waveforms of the STATCOM with a 24-pulse HN-VSC operating in a reactive current control mode.

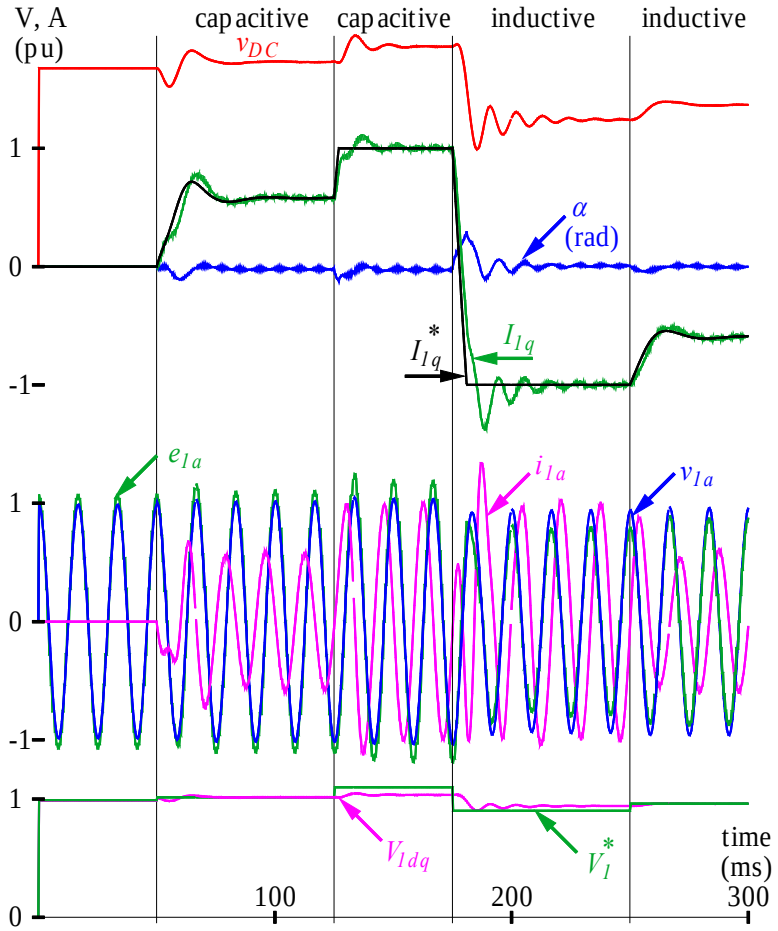


Figure 8-23. Performance of the STATCOM with a 24-pulse HN-VSC operating in a voltage control mode.

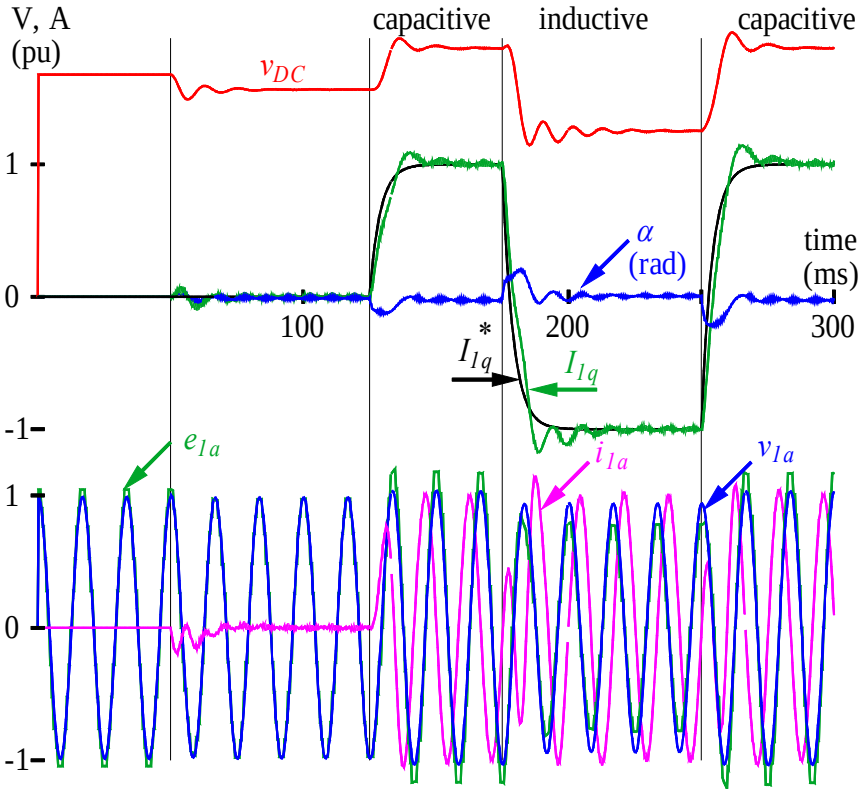


Figure 8-24. Performance of the STATCOM with a 24-pulse QHN-VSC operating in a reactive current control mode.

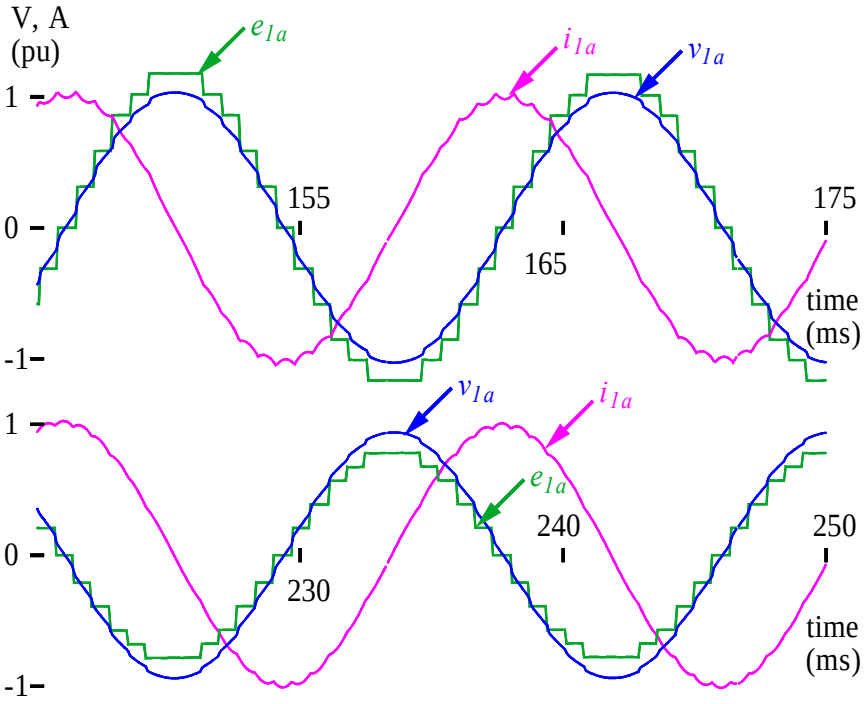


Figure 8-25. Waveforms of the STATCOM with a 24-pulse QHN-VSC operating in a reactive current control mode.

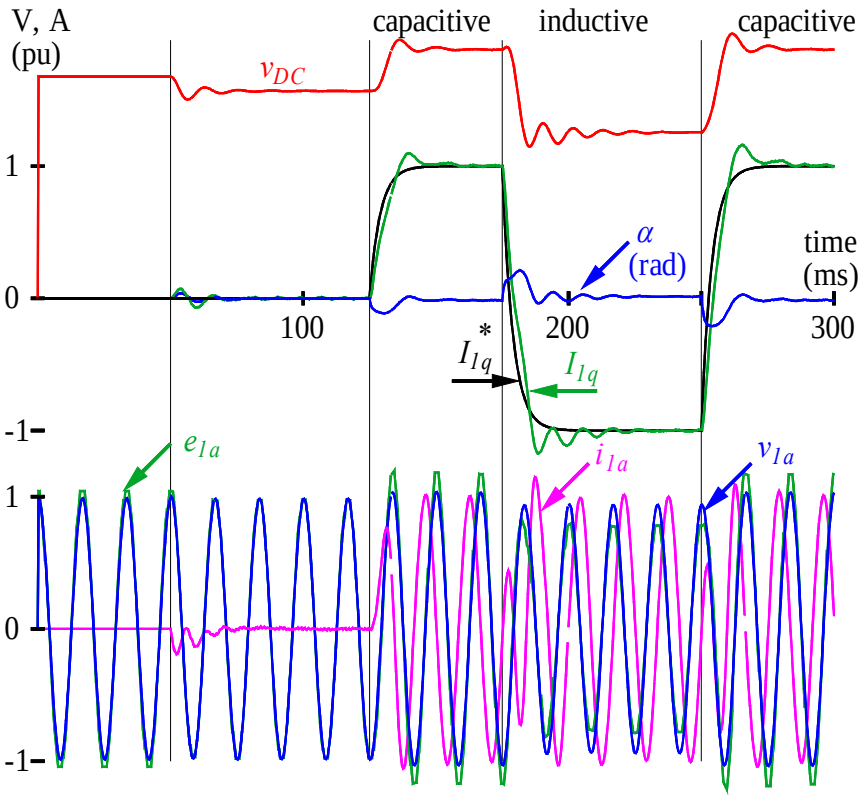


Figure 8-26. Performance of the STATCOM with a 48-pulse QHN-VSC operating in a reactive current control mode.

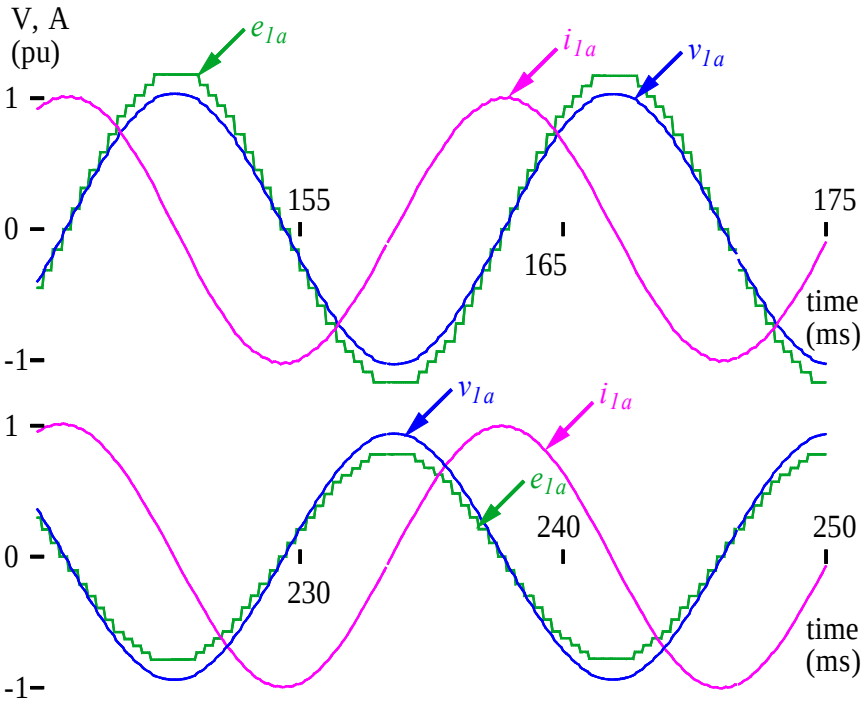


Figure 8-27. Waveforms of the STATCOM with a 48-pulse QHN-VSC operating in a reactive current control mode.

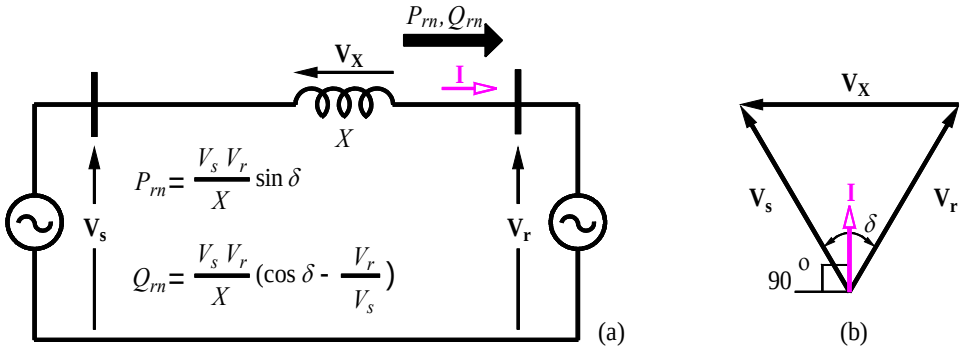


Figure 8-28. Elementary power transmission system.

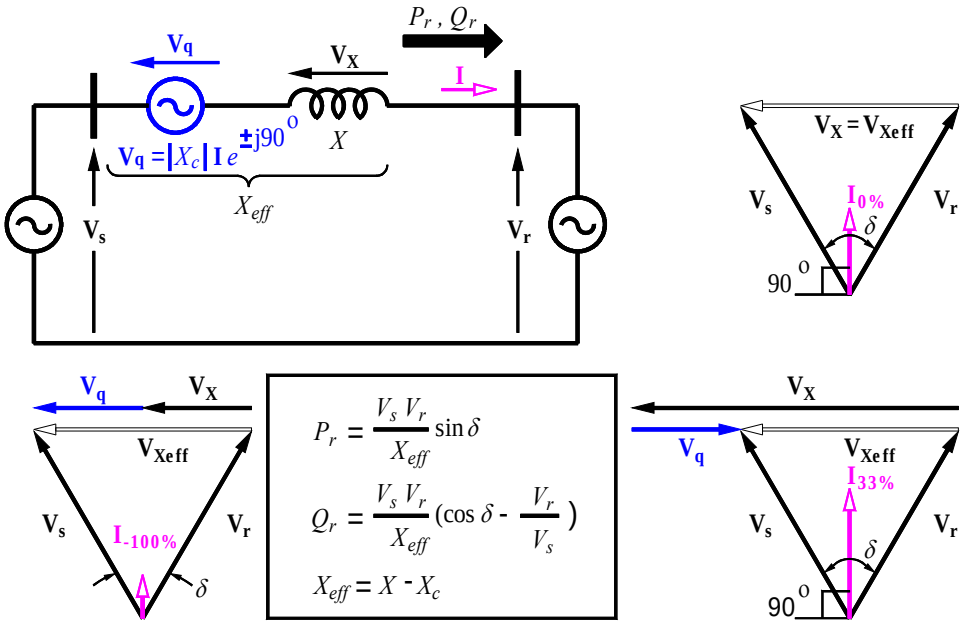


Figure 8-29. SSSC operated in inductive and capacitive modes and the related phasor diagrams.

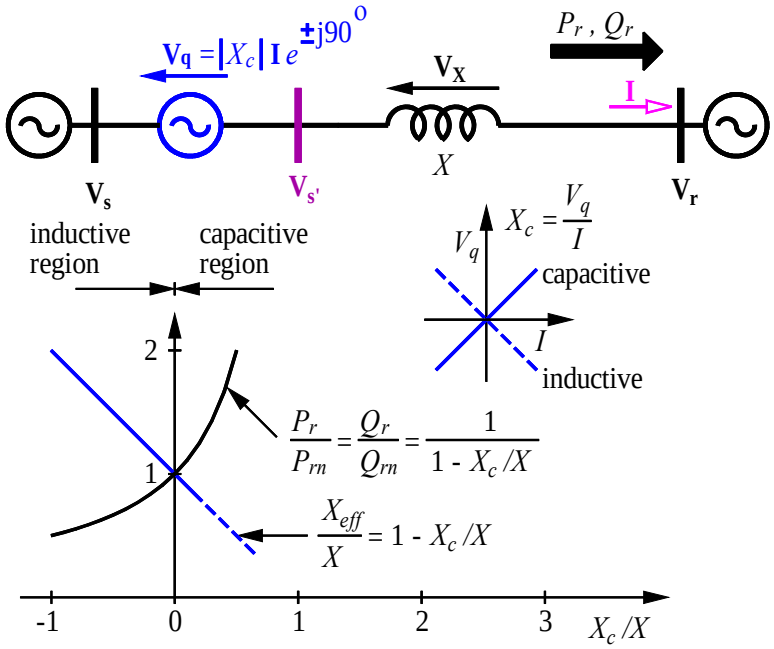


Figure 8-30. Effect of compensating reactance on power flow and effective reactance.

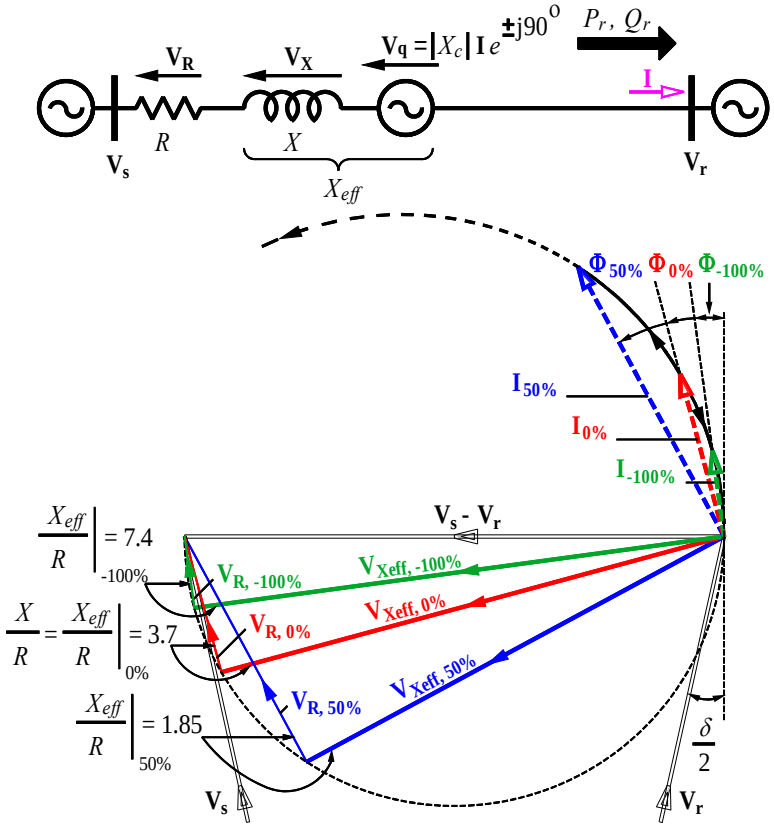


Figure 8-31. Reactance compensation of a lossy transmission line.

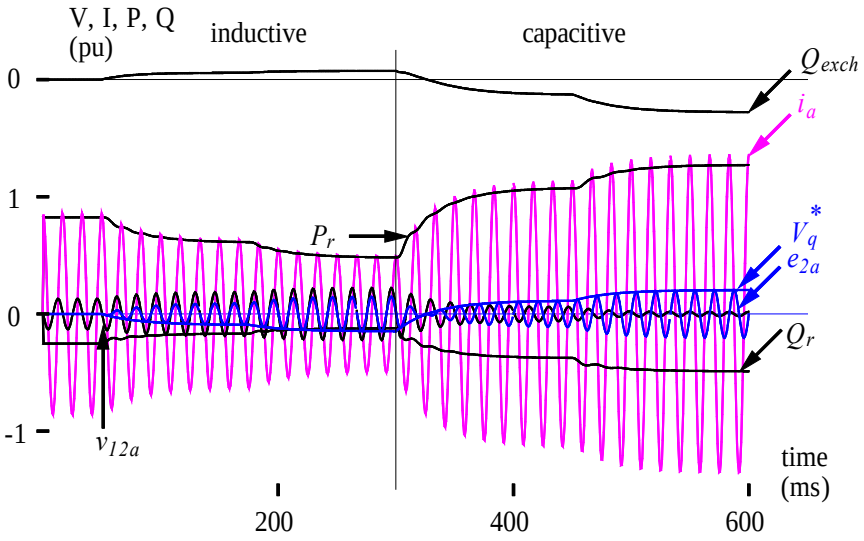


Figure 8-32. Exchanged reactive power and the resulting voltages and currents due to a series-connected compensating voltage into the transmission line through a coupling transformer.

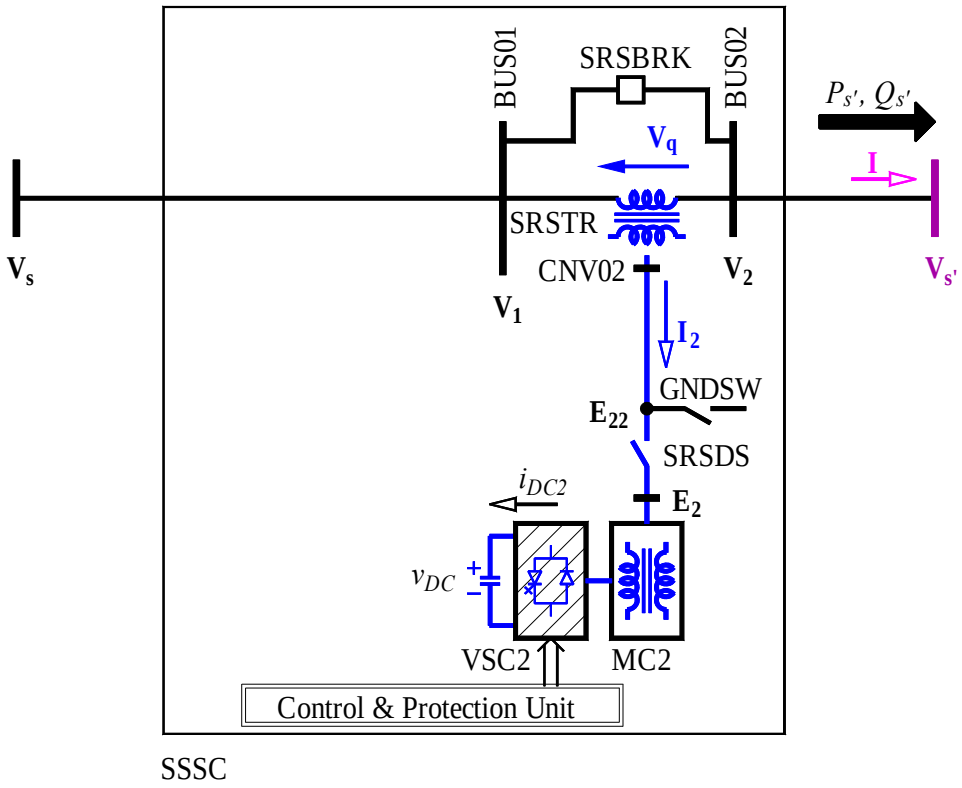


Figure 8-33. Static synchronous series compensator.

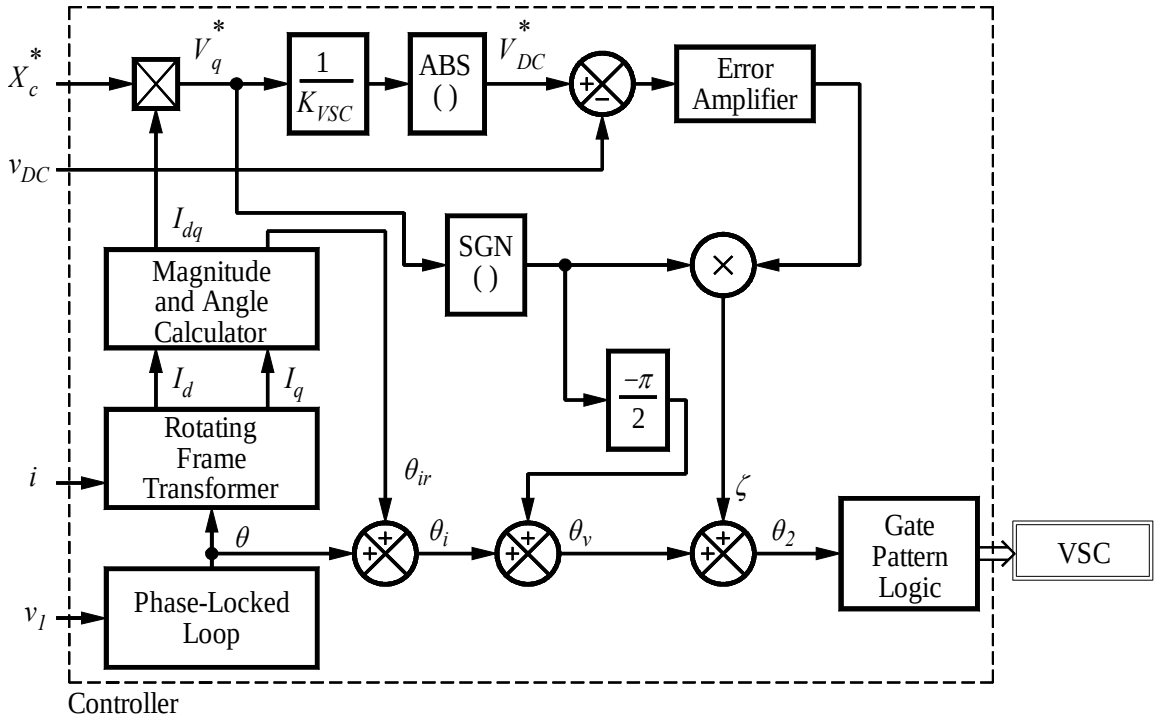


Figure 8-34. Reactance control block diagram of the static synchronous series compensator.

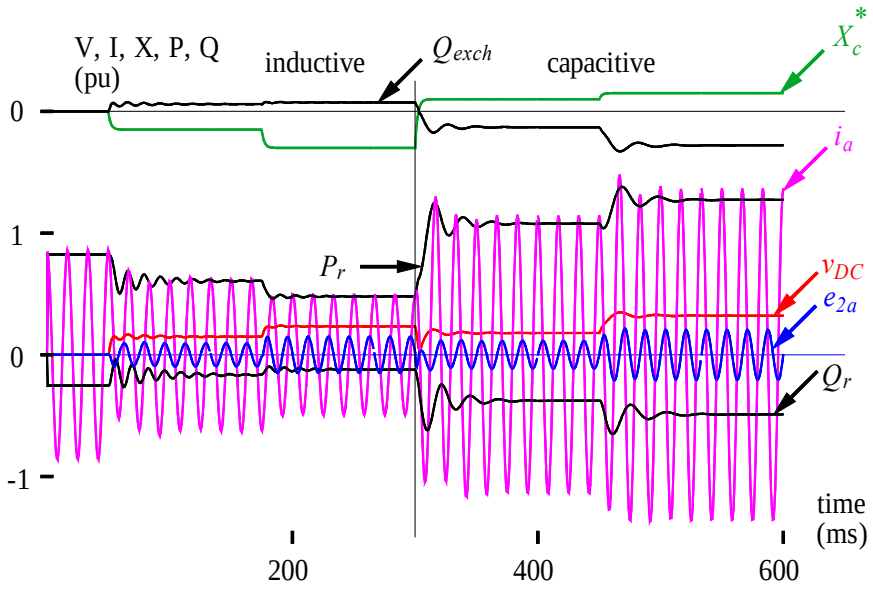


Figure 8-35. Performance of the SSSC with an infinite pulse VSC operating in inductive and capacitive modes.

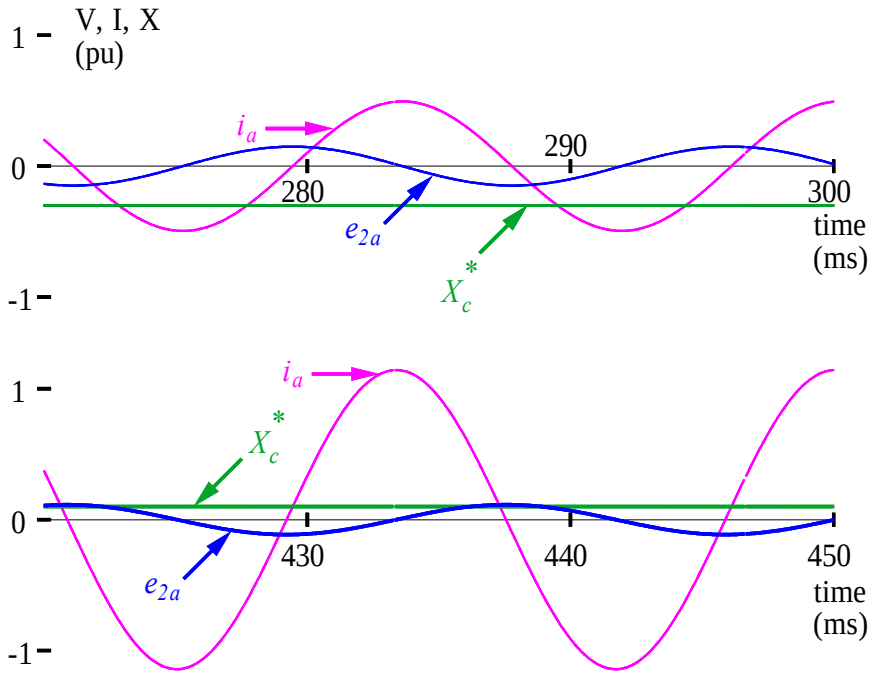


Figure 8-36. Waveforms from the SSSC with an infinite pulse VSC operating in inductive and capacitive modes.

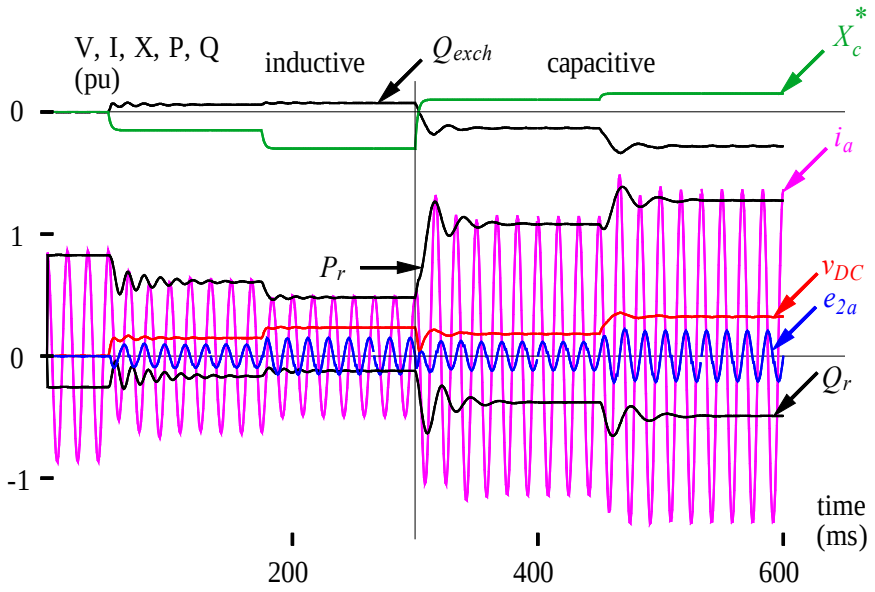


Figure 8-37. Performance of the SSSC with a 24-pulse HN-VSC operating in inductive and capacitive modes.

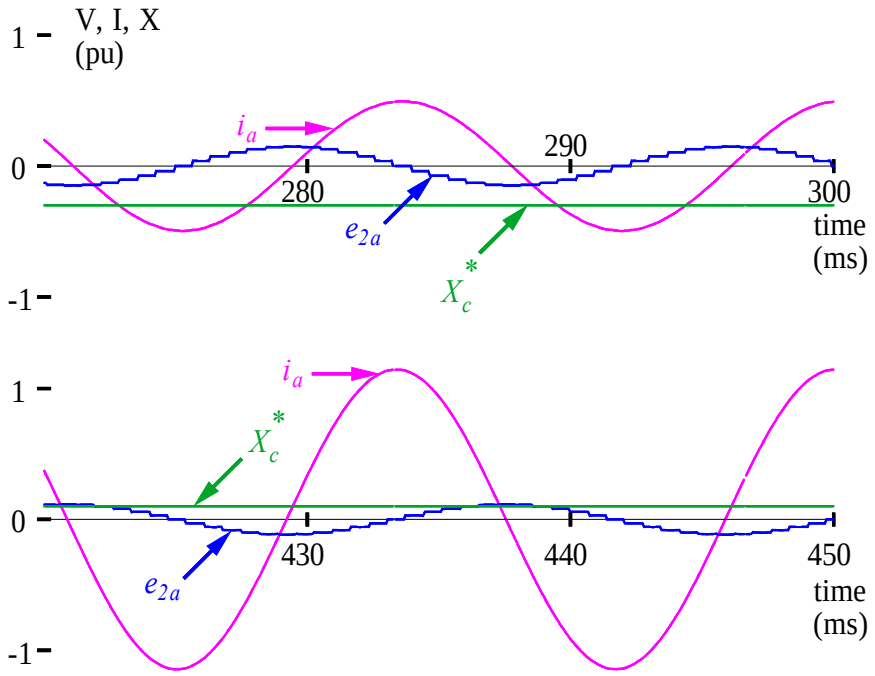


Figure 8-38. Waveforms from the SSSC with a 24-pulse HN-VSC operating in inductive and capacitive modes.

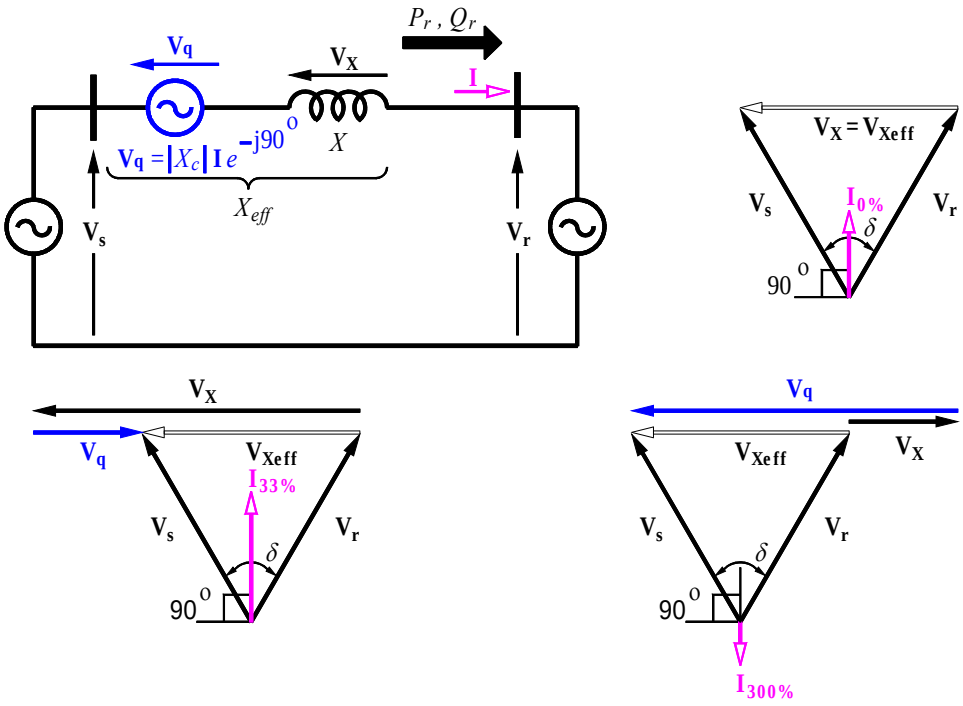


Figure 8-39. SSSC operating with a capacitive reactance control method and the related phasor diagrams.

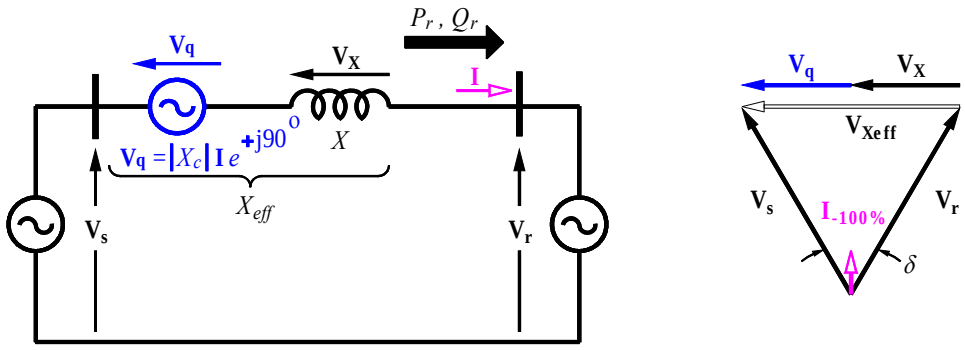


Figure 8-40. SSSC operating with an inductive reactance control method and the related phasor diagram.

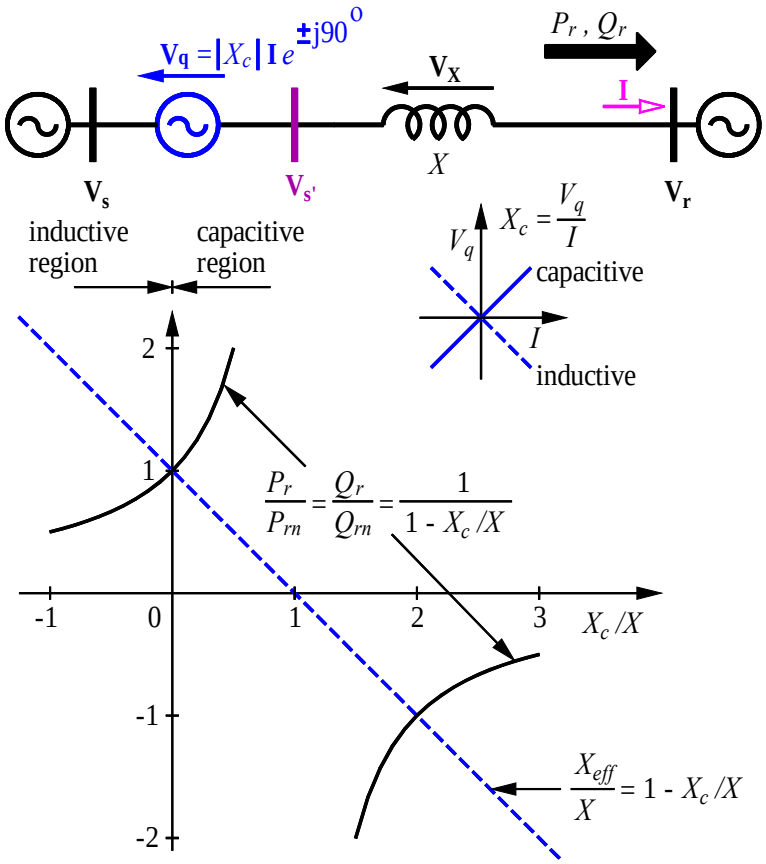


Figure 8-41. Effect of compensating reactance on effective reactance and power flow.

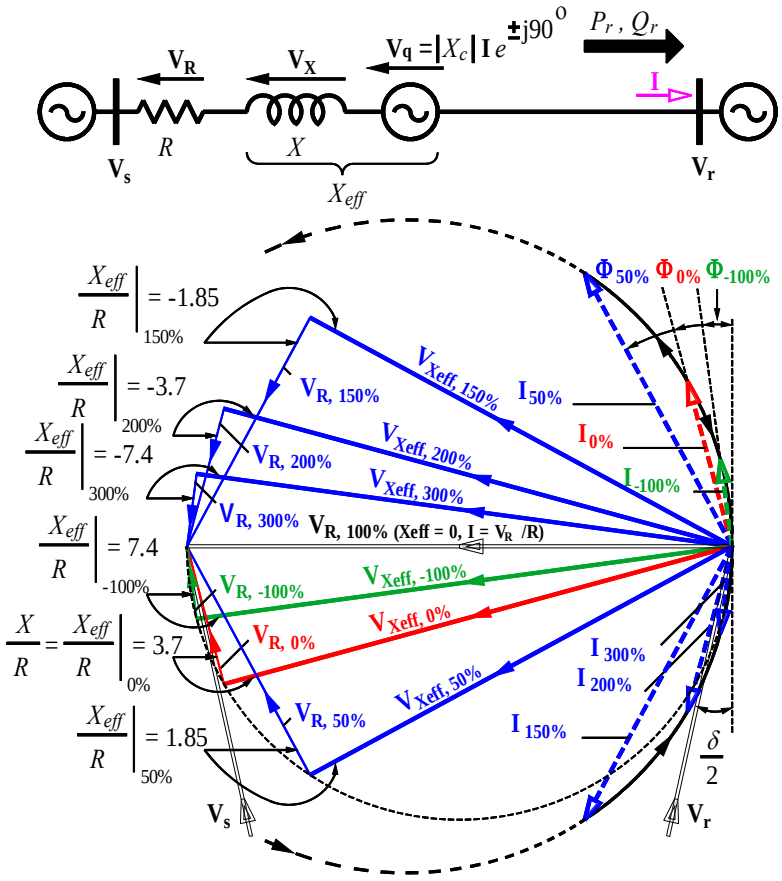


Figure 8-42. SSSC operating with reactance control method.

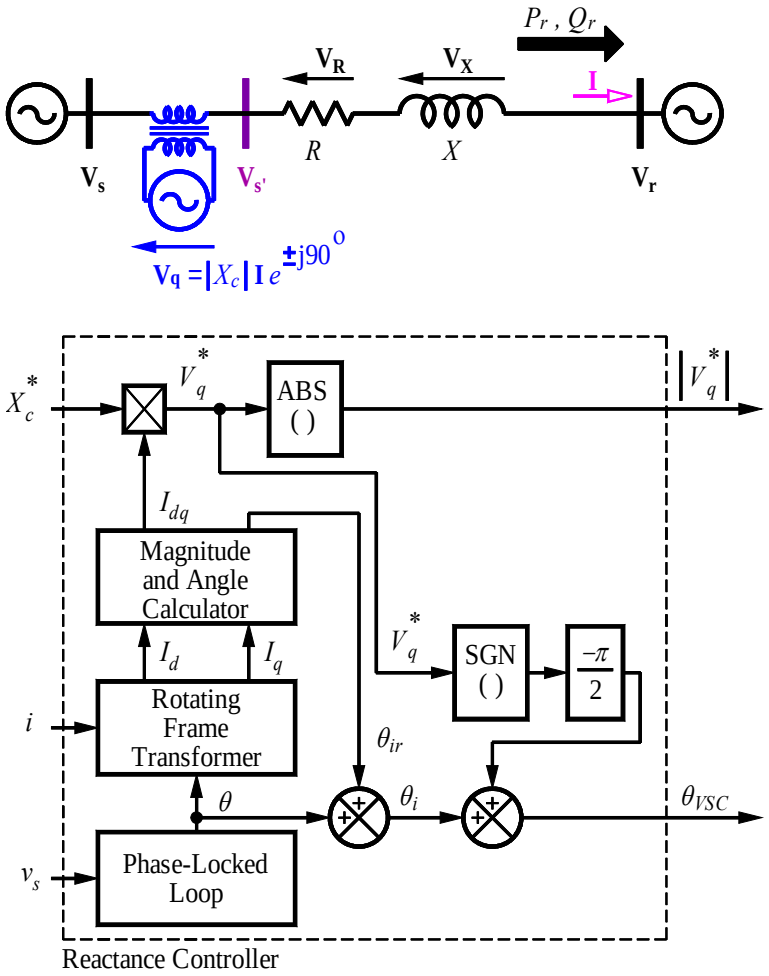


Figure 8-43. Reactance control scheme of the SSSC.

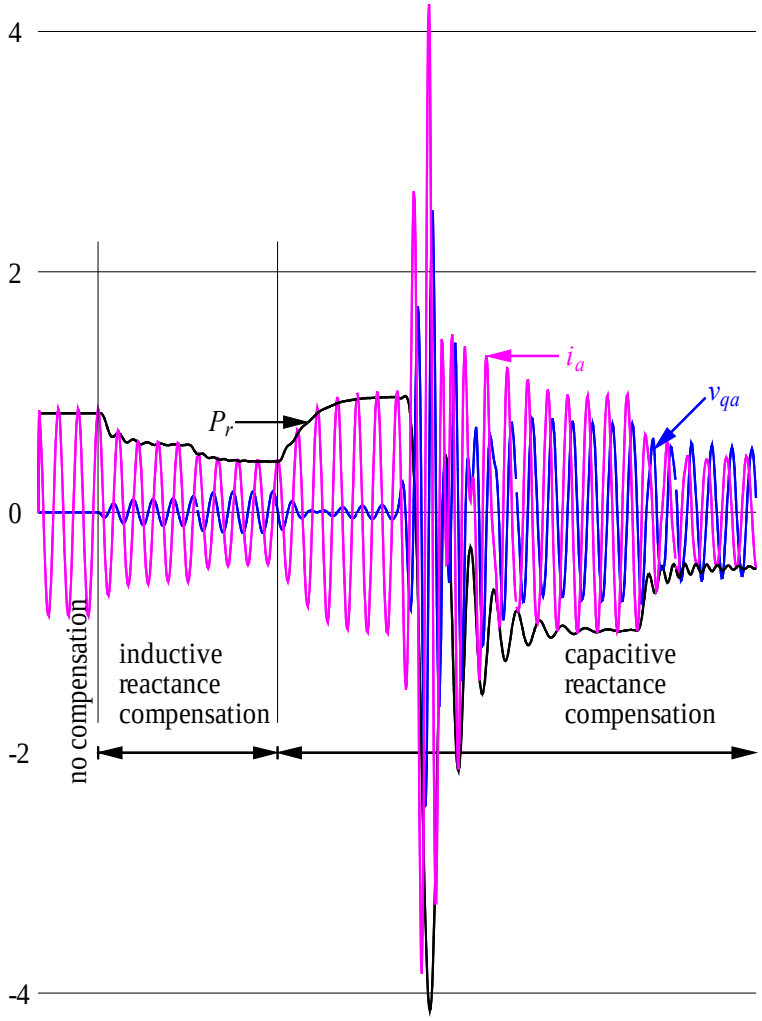


Figure 8-44. Performance of the SSSC with reactance control method.

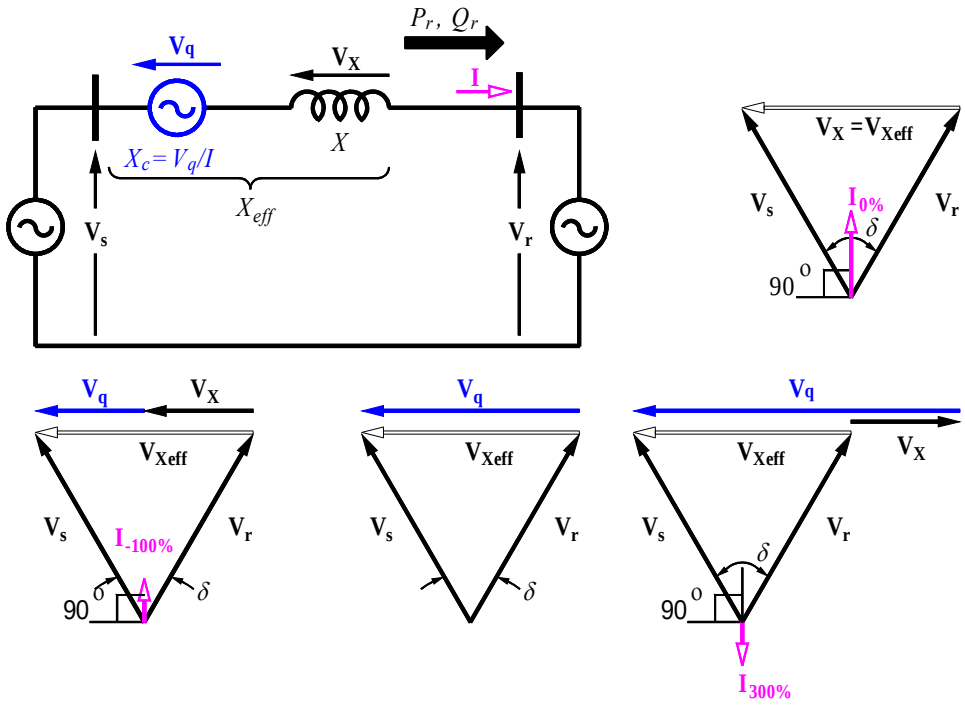


Figure 8-45. SSSC operating with a voltage control method with a compensating voltage in phase with voltage across transmission line effective reactance and the related phasor diagrams.

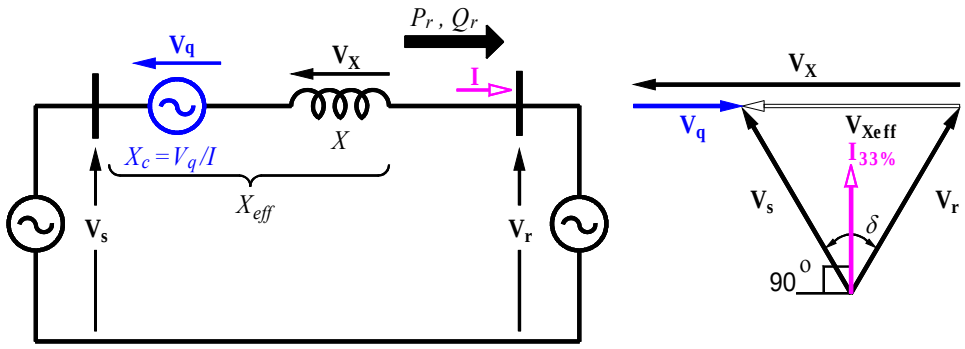


Figure 8-46. SSSC operating with a voltage control method with a compensating voltage in opposite phase with voltage across transmission line effective reactance and the related phasor diagram.

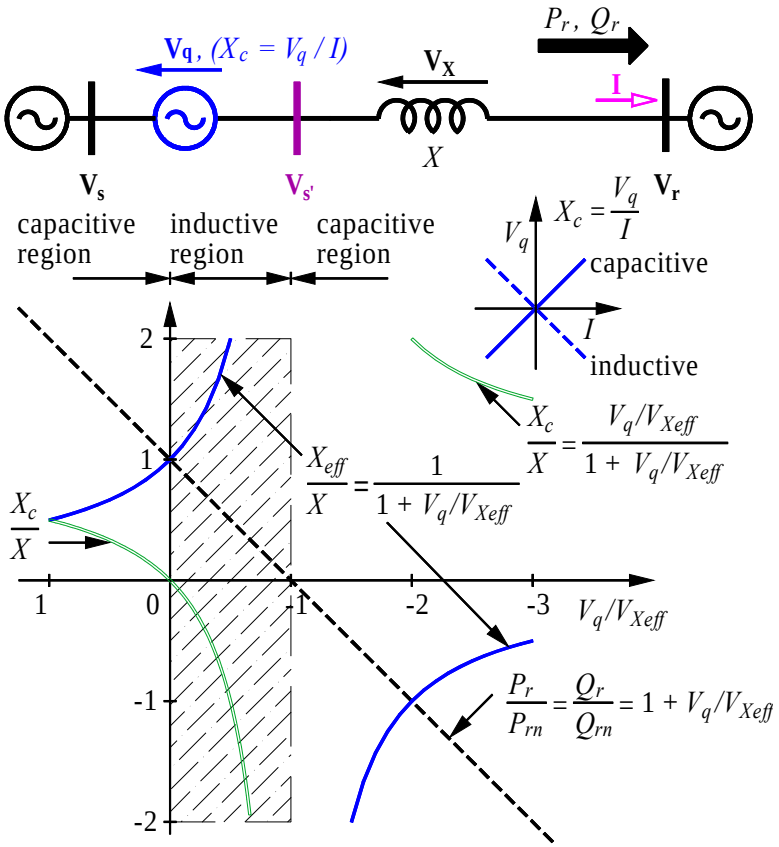


Figure 8-47. Effect of compensating voltage on power flow, effective reactance, and compensating reactance.

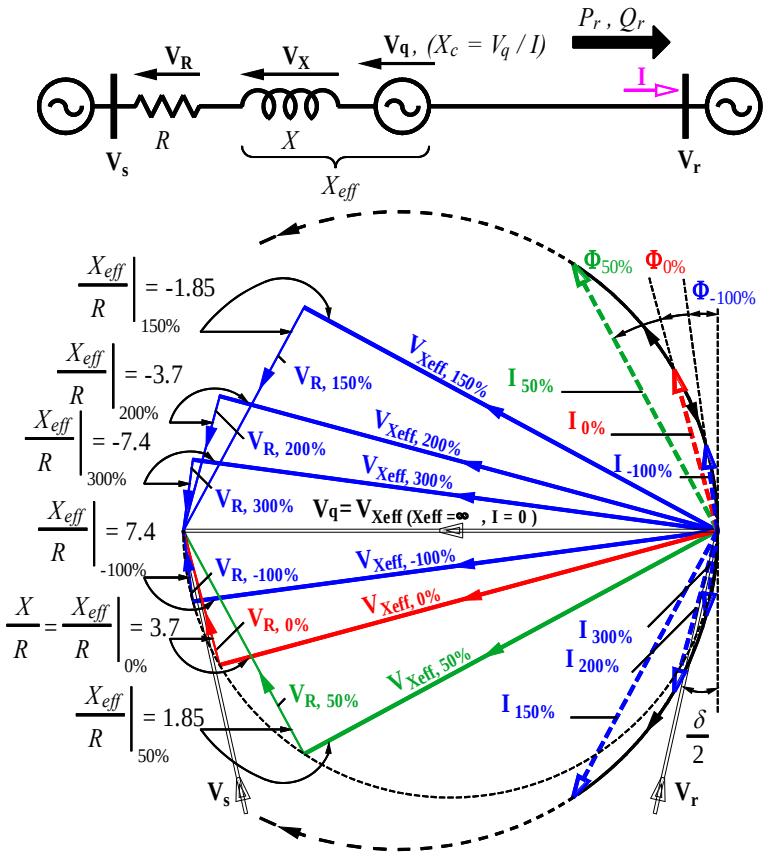


Figure 8-48. SSSC operating with voltage control method.

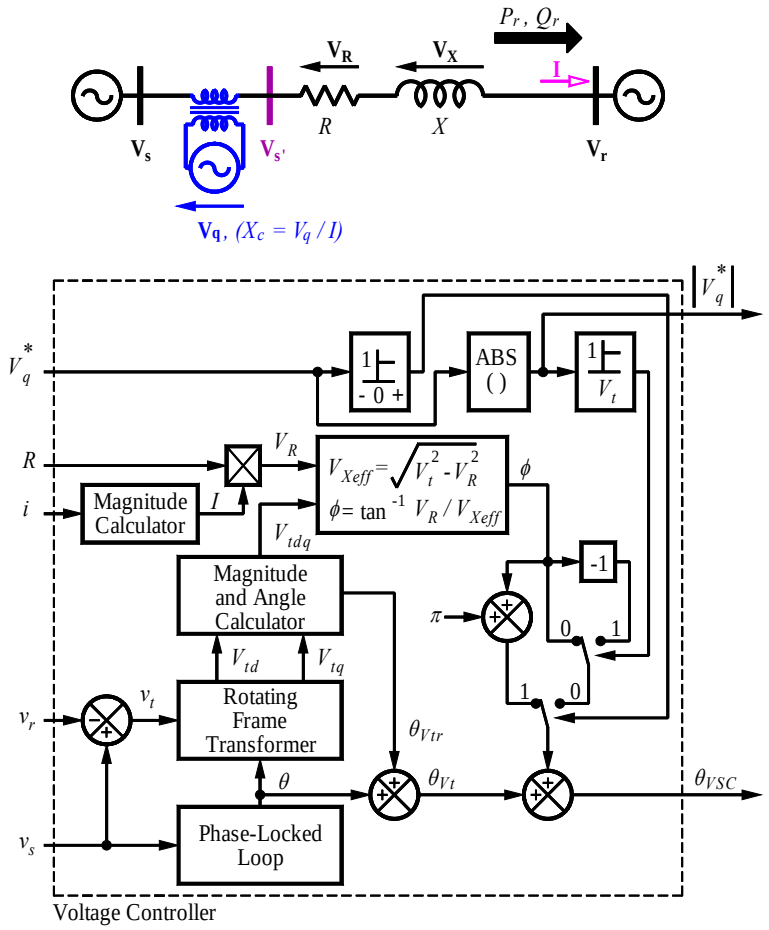


Figure 8-49. Voltage control scheme of the SSSC.

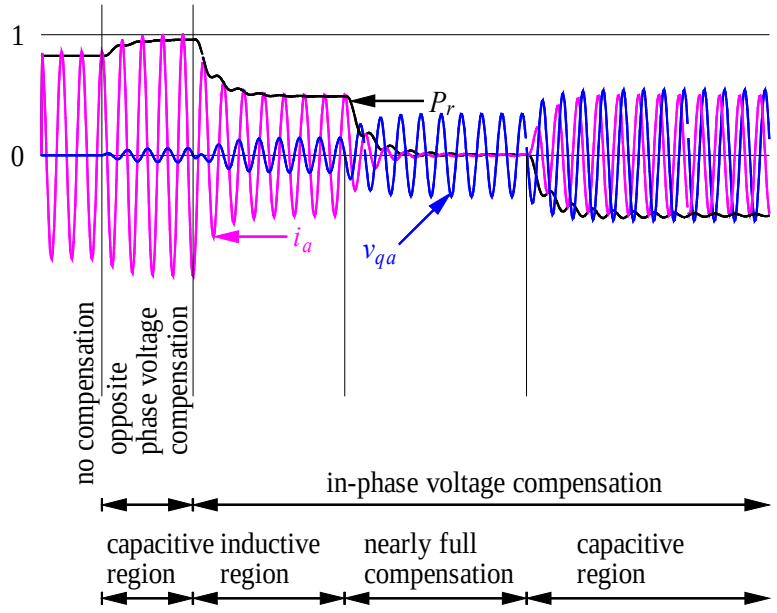


Figure 8-50. Performance of the SSSC with voltage control method.

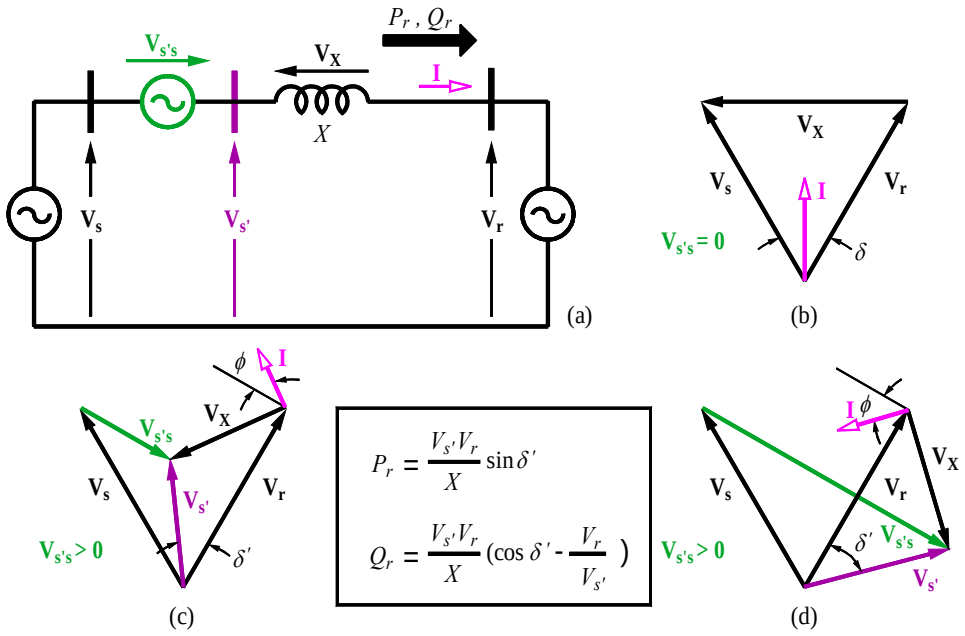


Figure 8-51. UPFC operating with an open loop compensating voltage and the related phasor diagrams.

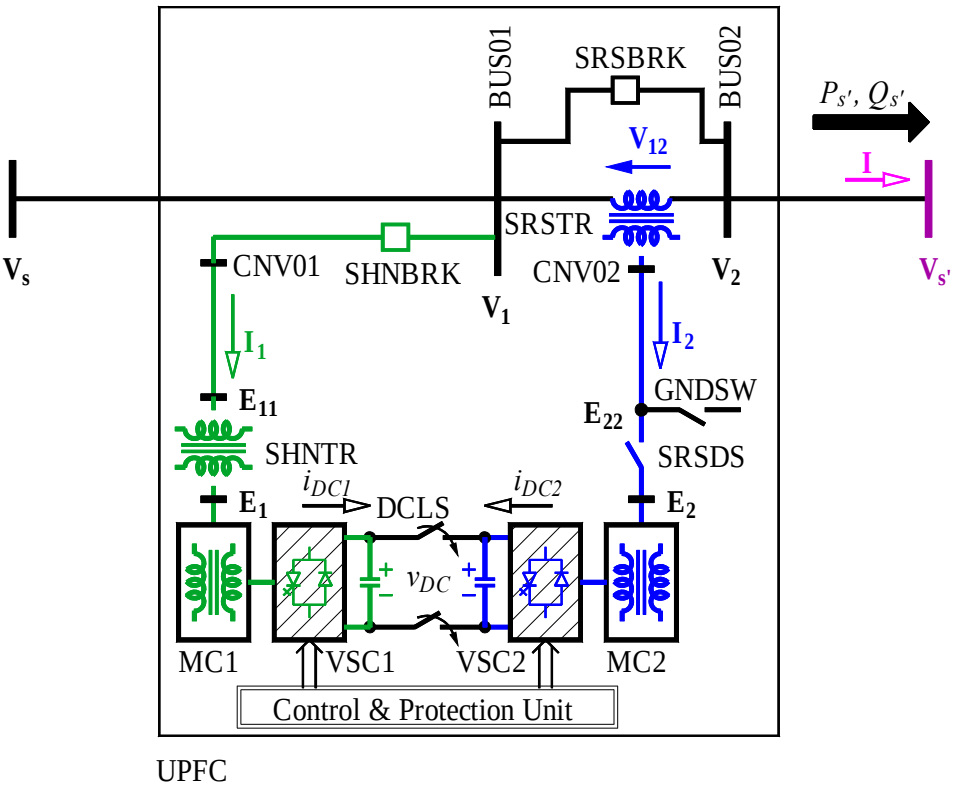


Figure 8-52. UPFC model in EMTP.

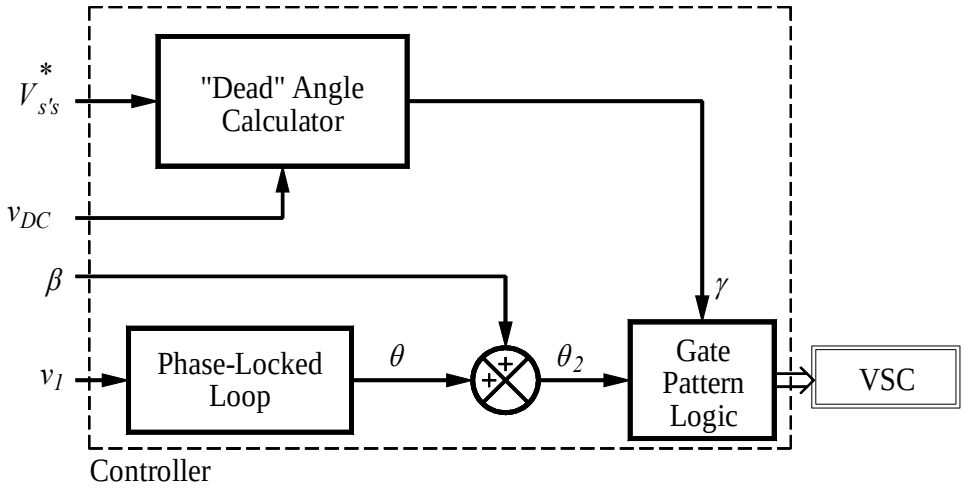


Figure 8-53. Control block diagram of the SSSC in an open loop voltage injection mode of operation of the UPFC.

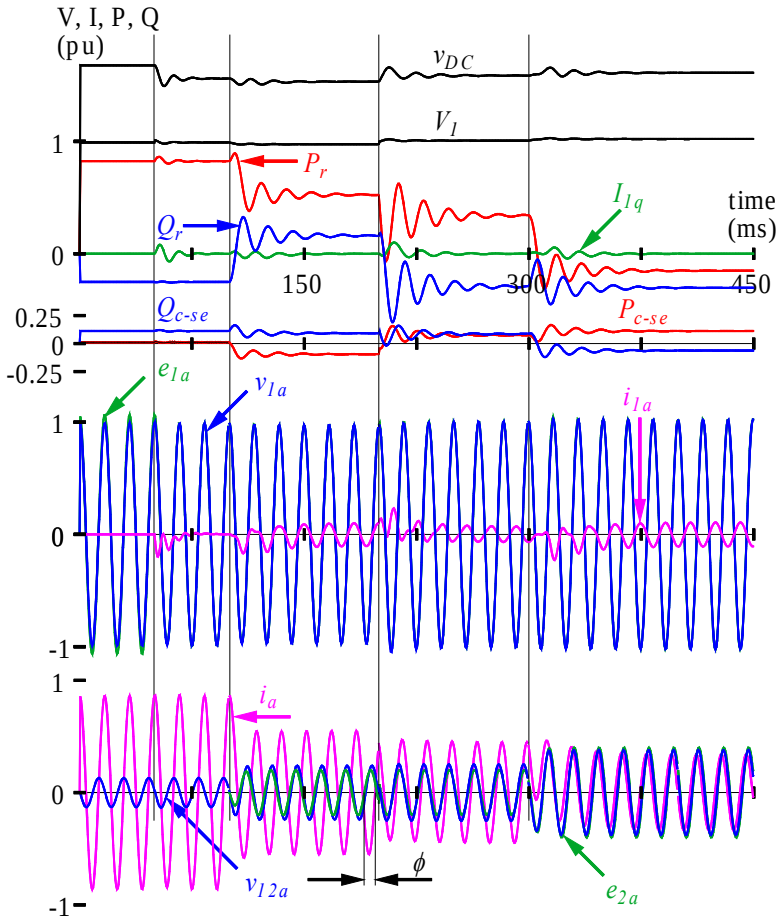


Figure 8-54. Performance of the UPFC with an infinite pulse VSC2 operating in an open loop voltage injection mode while regulating a zero reactive current through an infinite pulse VSC1.

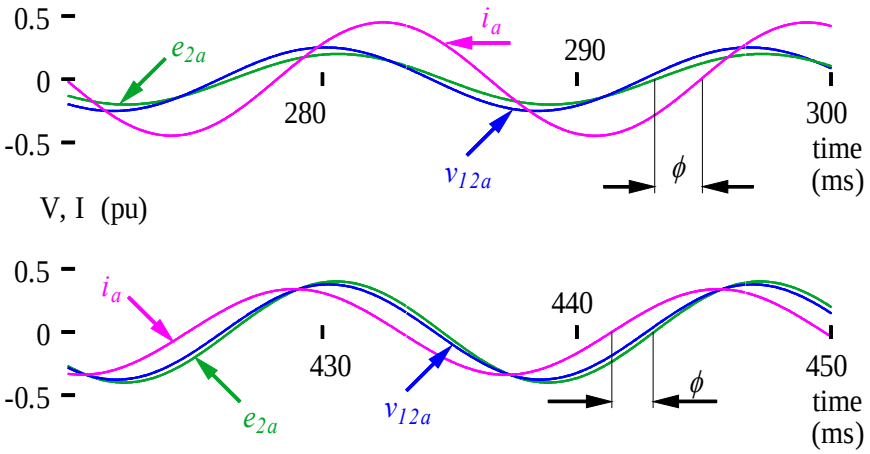


Figure 8-55. Waveforms from the UPFC with an infinite pulse VSC2 operating in an open loop voltage injection mode.

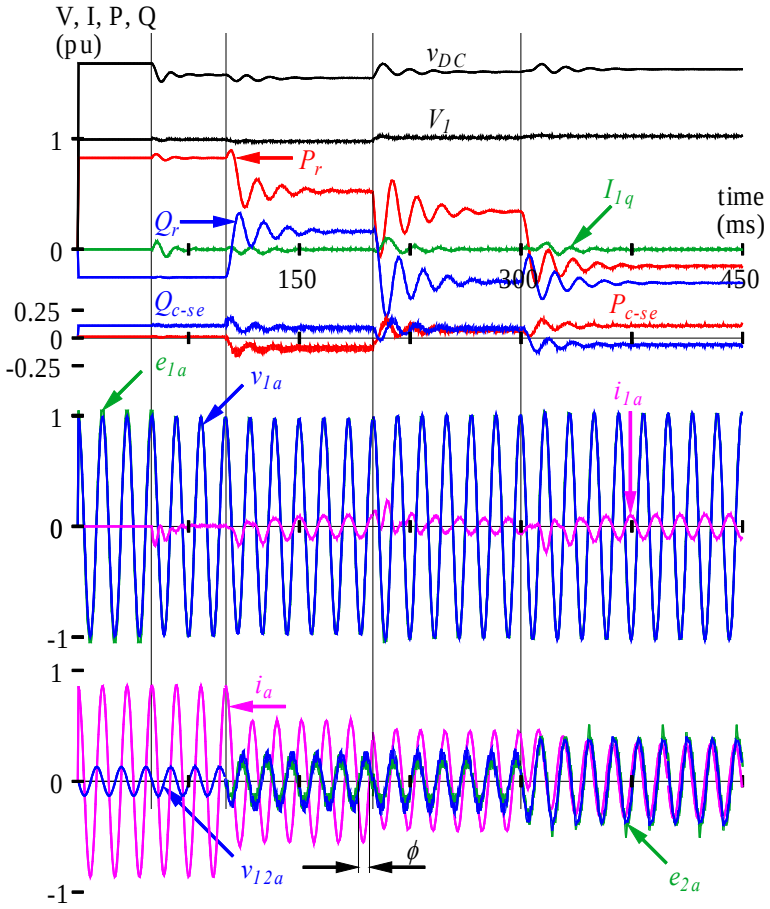


Figure 8-56. Performance of the UPFC with a 24-pulse QHN-VSC2 with three-level poles operating in an open loop voltage injection mode while regulating a zero reactive current through a 24-pulse QHN-VSC1 with three-level poles operating at a fixed dead angle to act as a 48-pulse QHN.

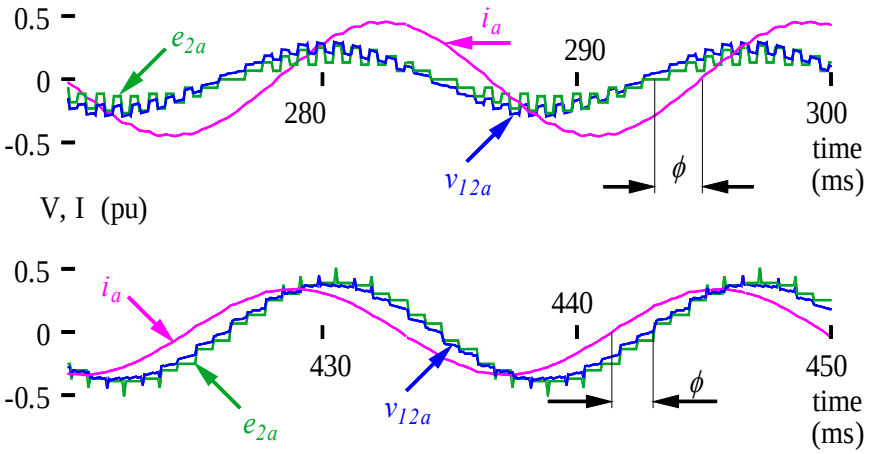


Figure 8-57. Waveforms from the UPFC with a 24-pulse QHN-VSC2 with three-level poles operating in an open loop voltage injection mode.

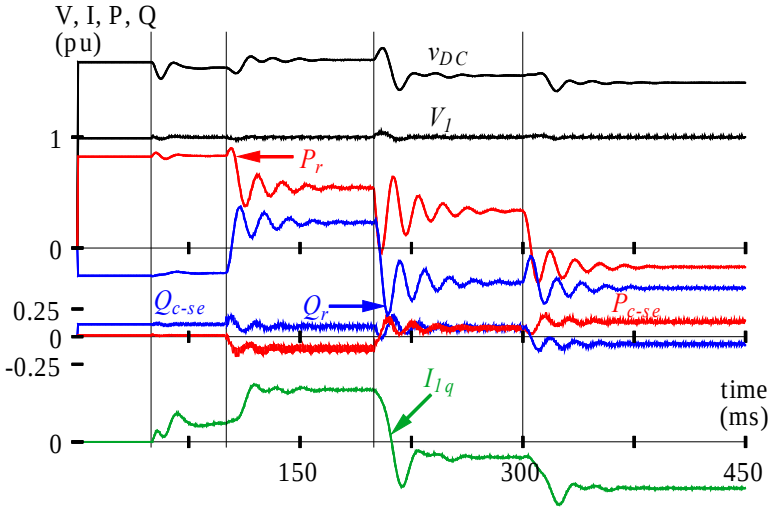


Figure 8-58. Performance of the UPFC with a 24-pulse QHN-VSC2 with three-level poles operating in an open loop voltage injection mode while regulating the BUS01 voltage with a 24-pulse QHN-VSC1 with three-level poles operating at a fixed dead angle to act as a 48-pulse QHN.

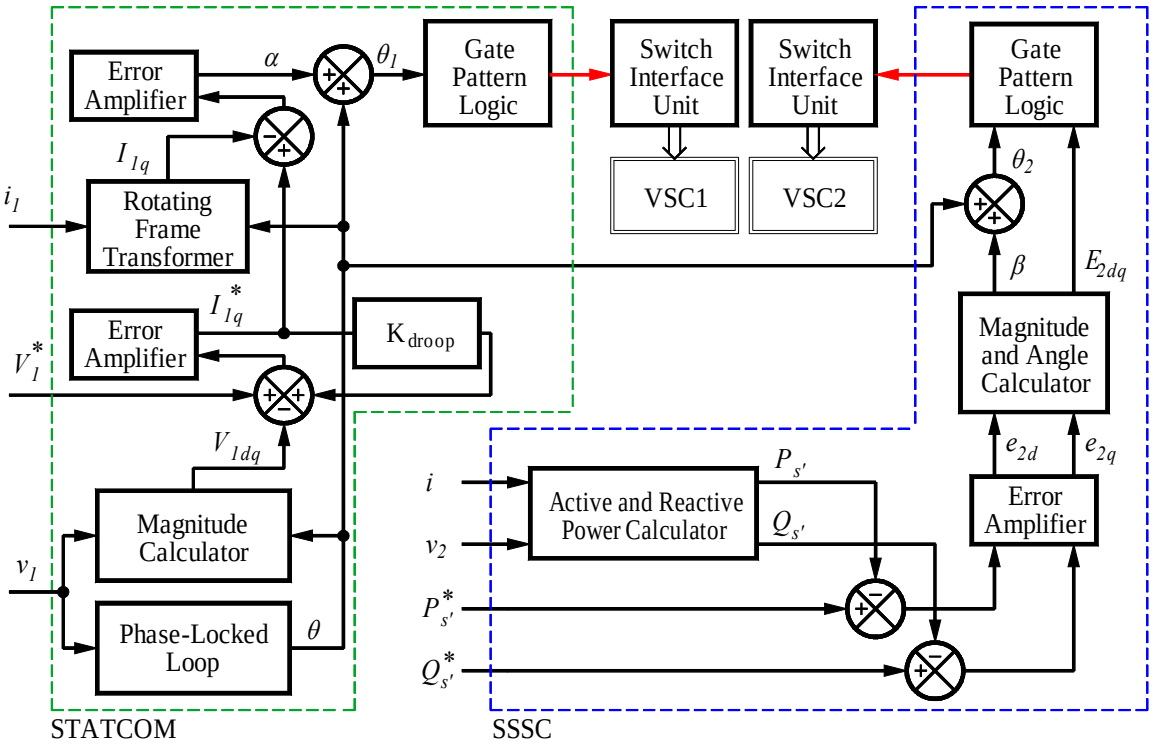


Figure 8-59. Closed loop automatic power flow control block diagram of the UPFC.

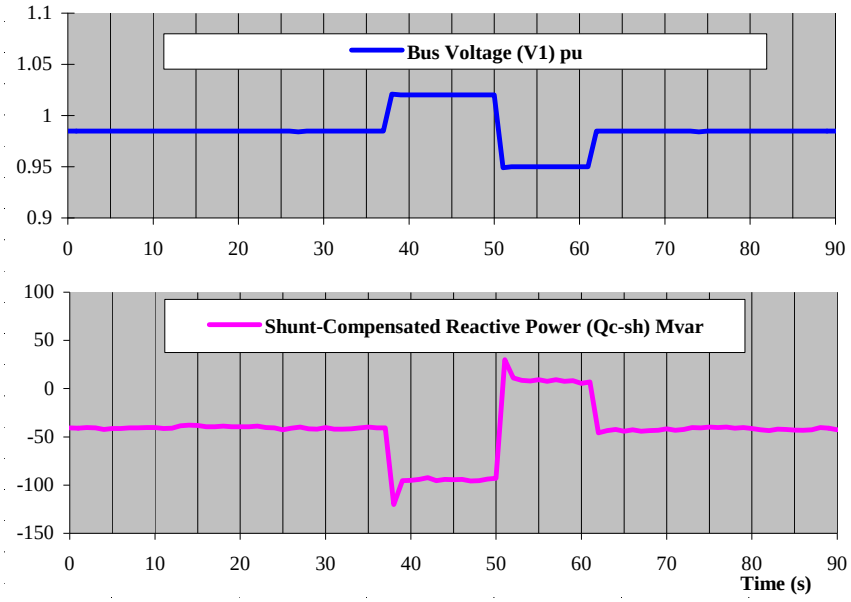


Figure 8-60. STATCOM test results for voltage control mode of operation (Sen & Keri-2002).

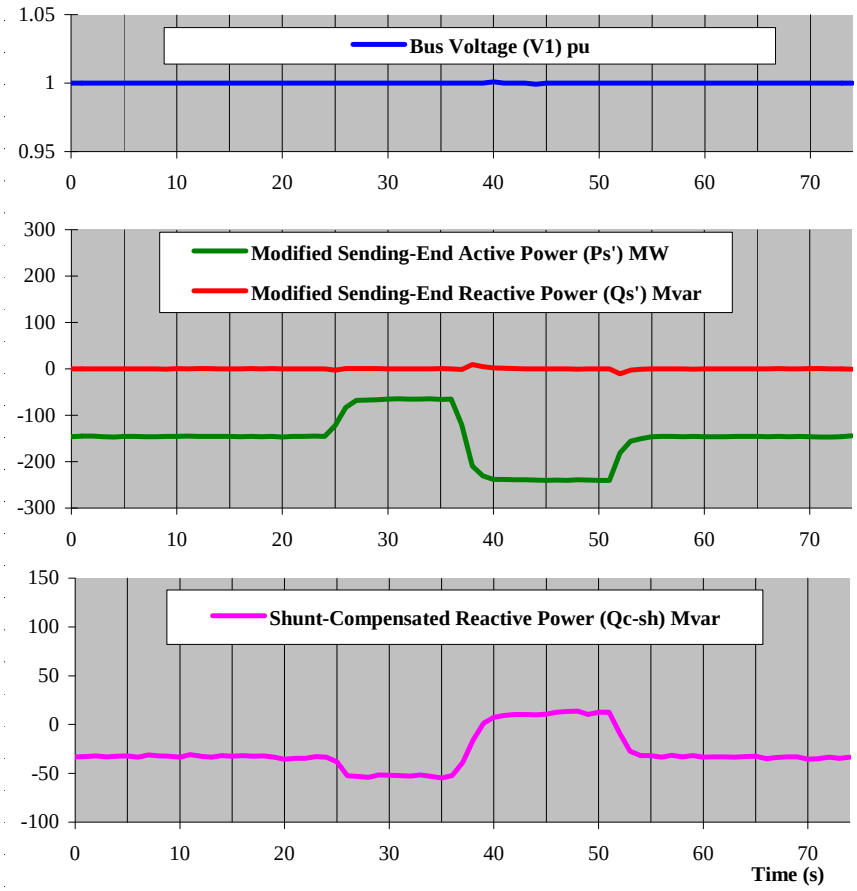


Figure 8-61. UPFC test results for automatic power flow control mode of operation with maintaining unity power factor and one pu bus voltage while regulating the line active power (Sen & Keri-2002).

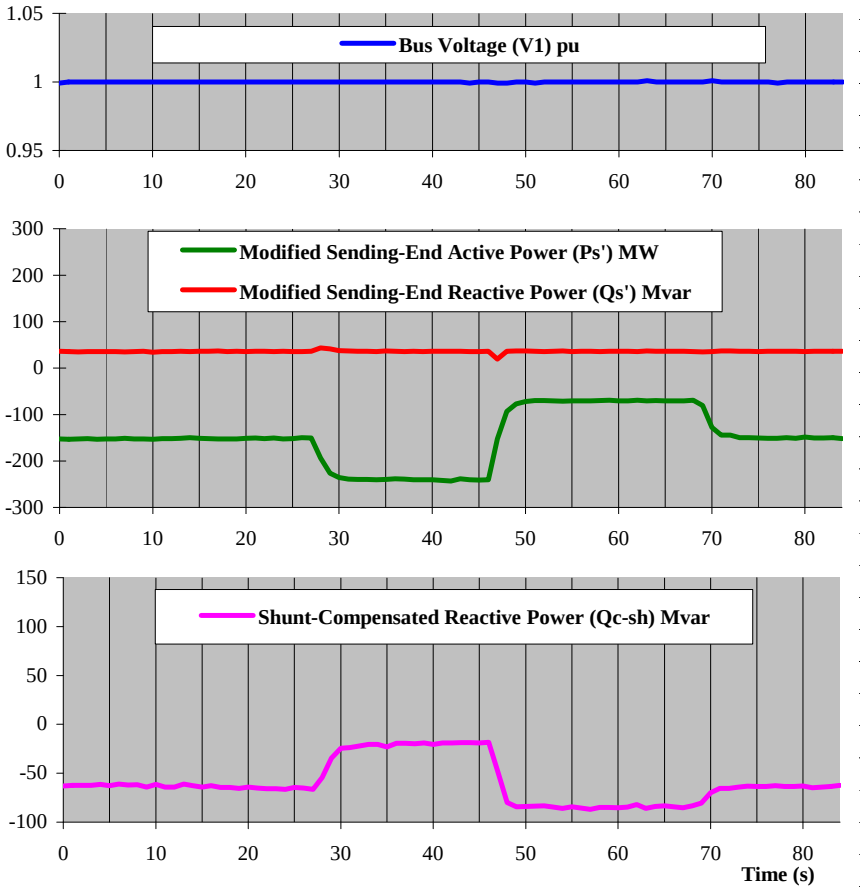


Figure 8-62. UPFC test results for automatic power flow control mode of operation while regulating only active power of the line and maintaining one pu bus voltage (Sen & Keri-2002).

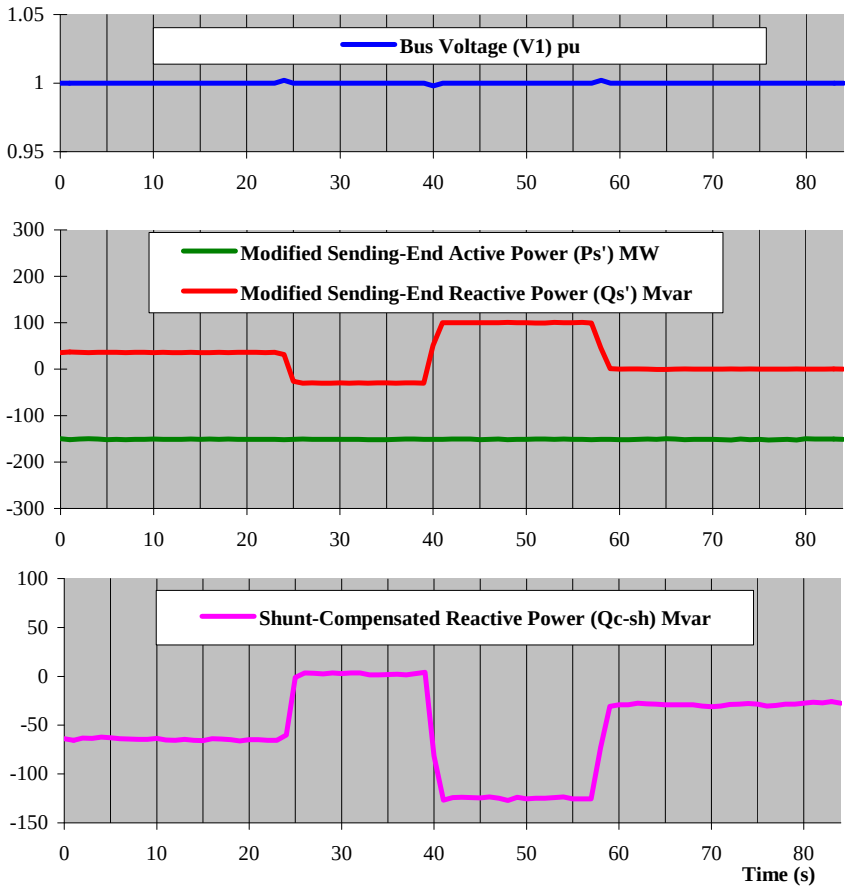


Figure 8-63. UPFC test results for automatic power flow control mode of operation while regulating only reactive power of the line and maintaining one pu bus voltage (Sen & Keri-2002).

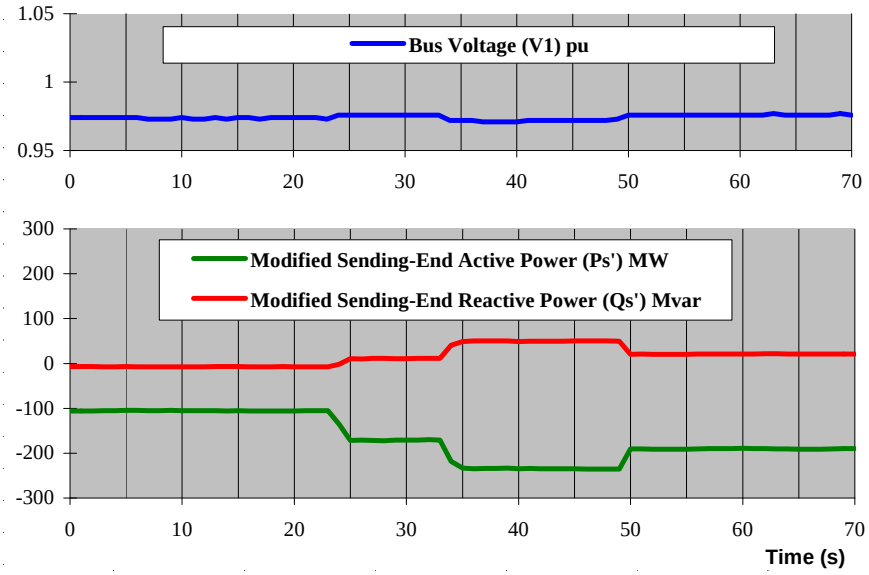


Figure 8-64. SSSC test results for reactance control mode of operation (Sen & Keri-2002).

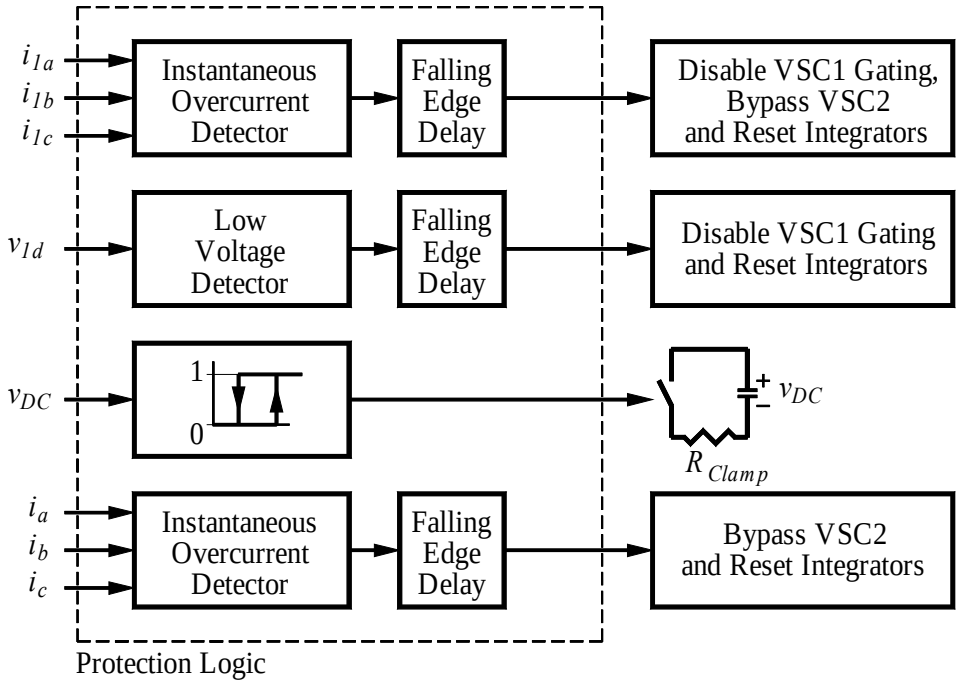


Figure 8-65. Protection scheme of the UPFC.

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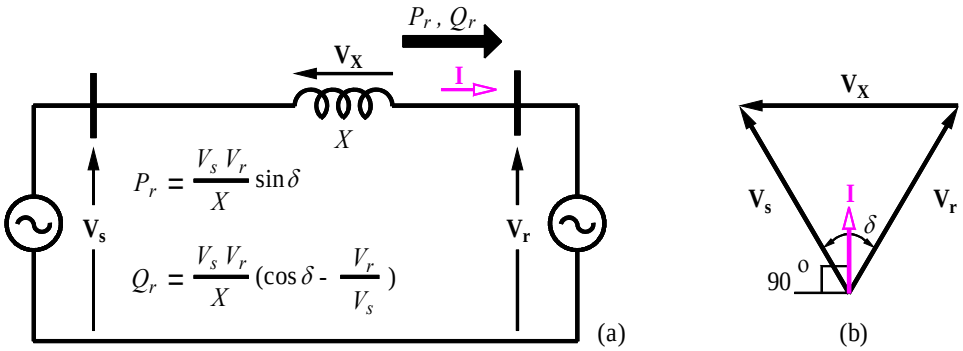


Figure 9-1. (a) Power transmission system. (b) Phasor diagram.

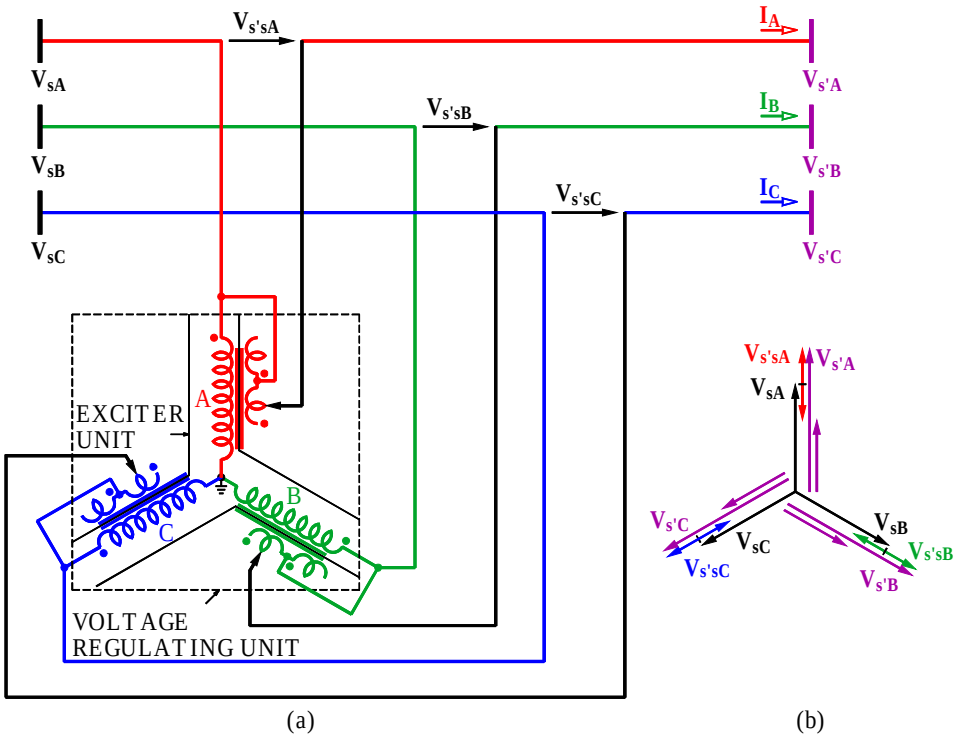


Figure 9-2. (a) Voltage regulating transformer (autotransformer). (b) Phasor diagram.

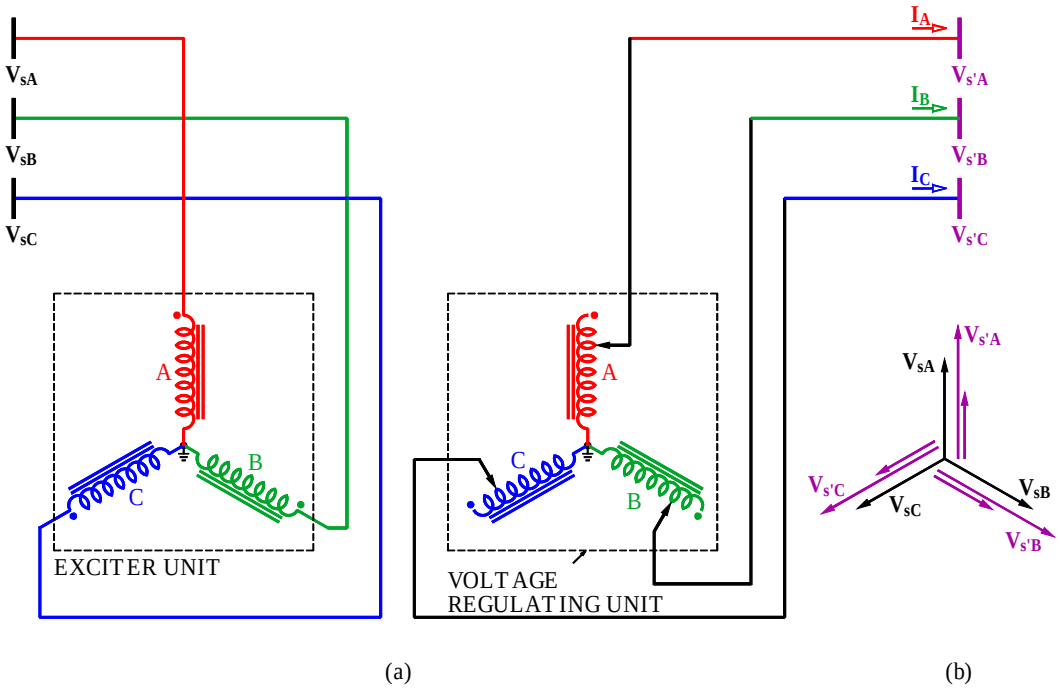


Figure 9-3. (a) Voltage regulating transformer (two-winding transformer). (b) Phasor diagram.

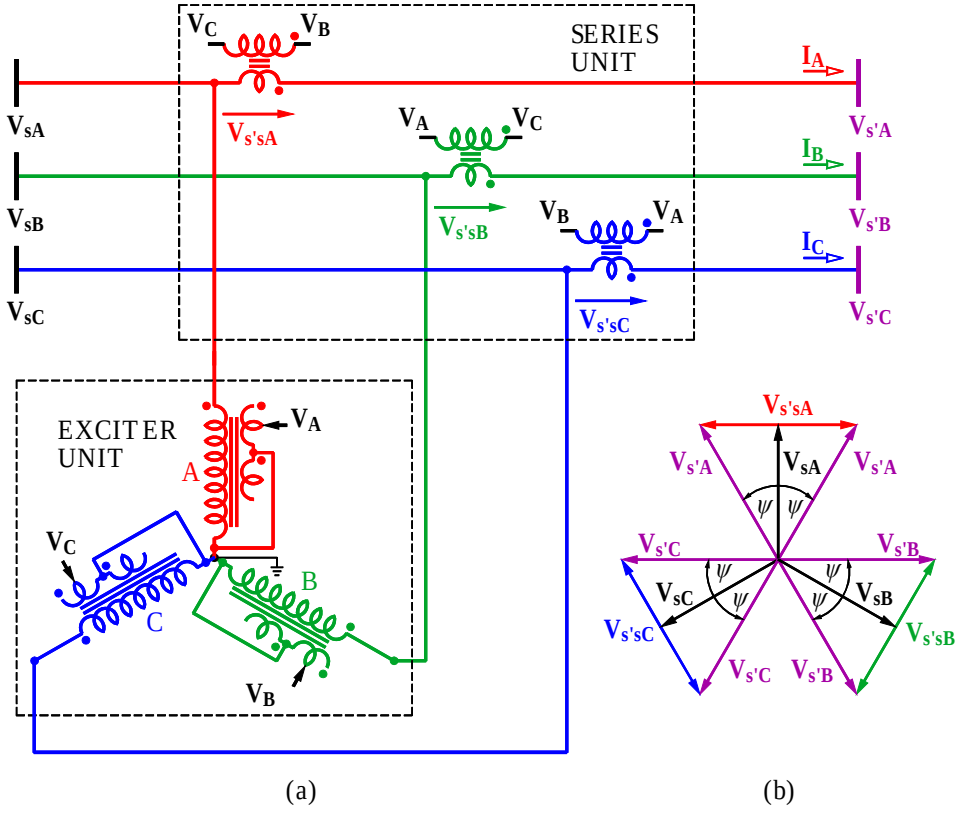


Figure 9-4. (a) Phase angle regulator. (b) Phasor diagram.

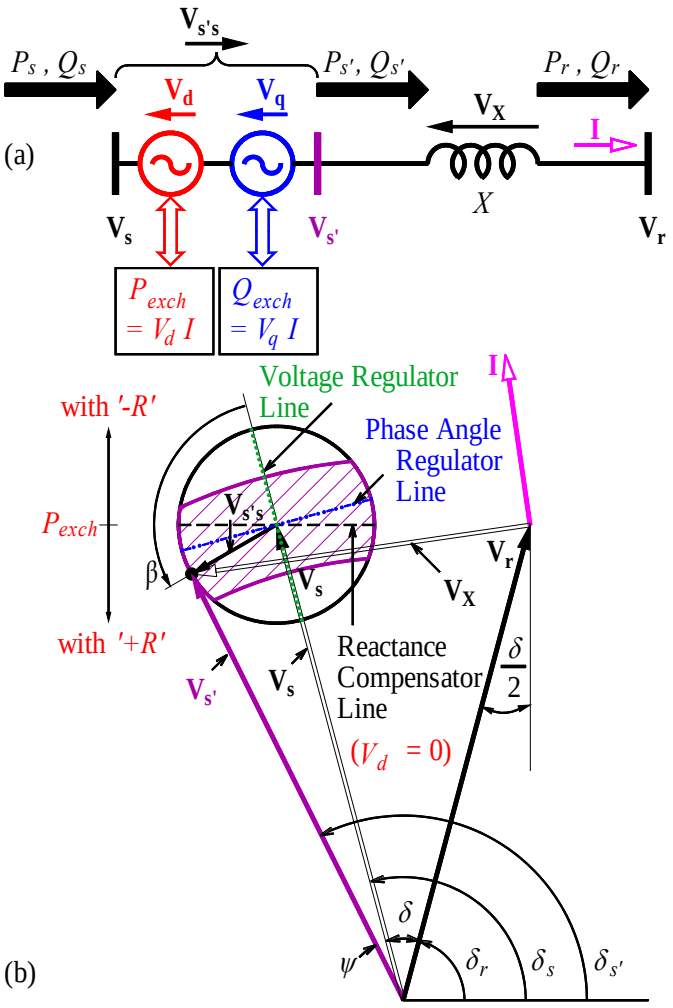


Figure 9-5(a, b). Effect of a series-connected compensating voltage on power flow in a transmission line. (a) Power transmission system with a series-connected compensating voltage ($\mathbf{V}_{s's}$). (b) Phasor diagram.

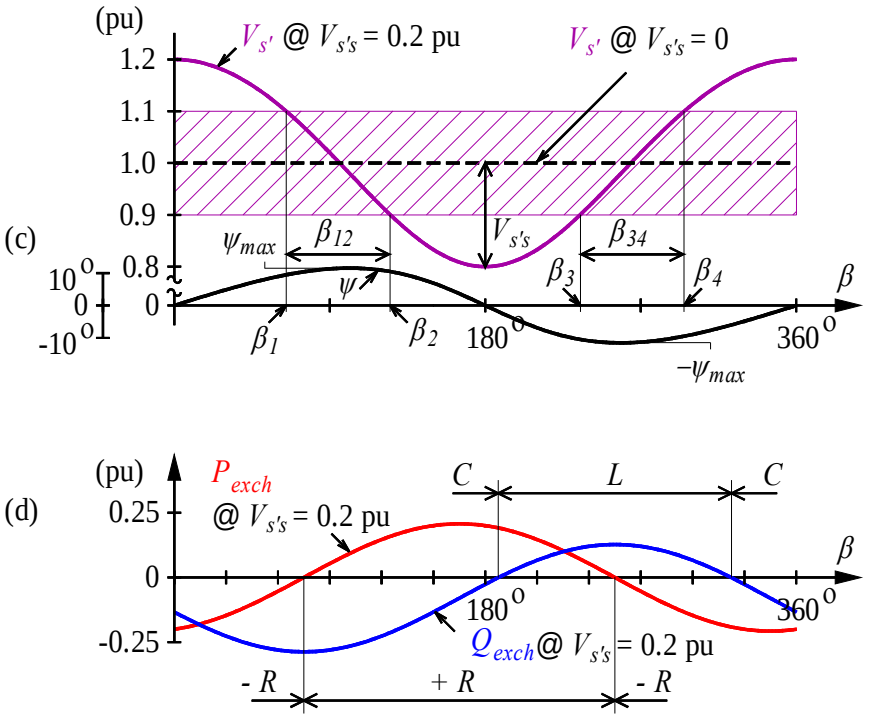


Figure 9-5(c, d). Effect of a series-connected compensating voltage on power flow in a transmission line. (c) Variations of the line voltage magnitude and relative phase angle (ψ). (d) Exchanged active and reactive powers as a function of relative phase angle (β).

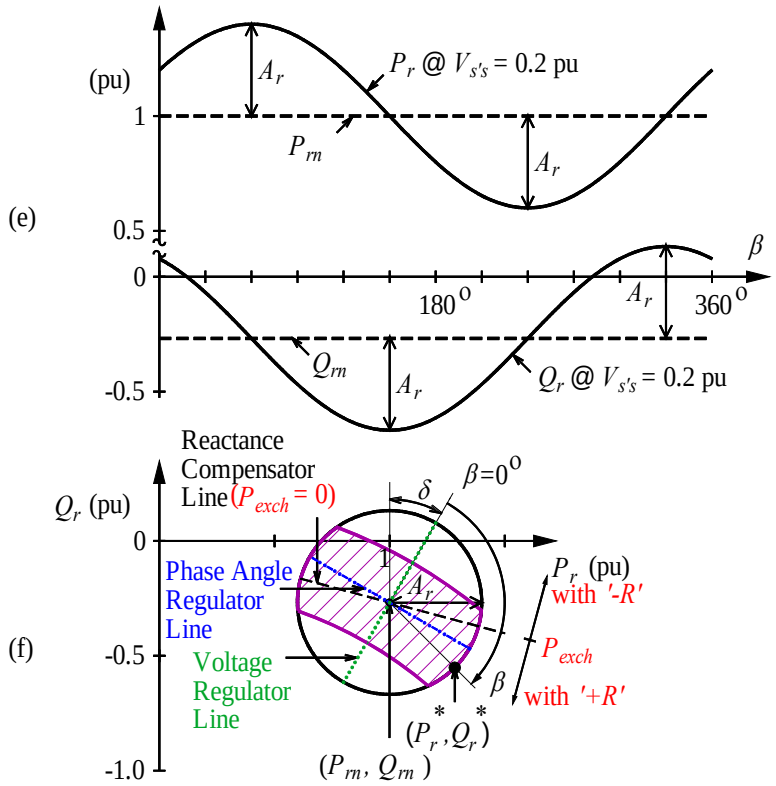


Figure 9-5(e, f). Effect of a series-connected compensating voltage on power flow in a transmission line. (e) Variation of the receiving-end active and reactive power flows (P_r and Q_r) as a function of the relative phase angle (β). (f) Receiving-end Q_r versus P_r.

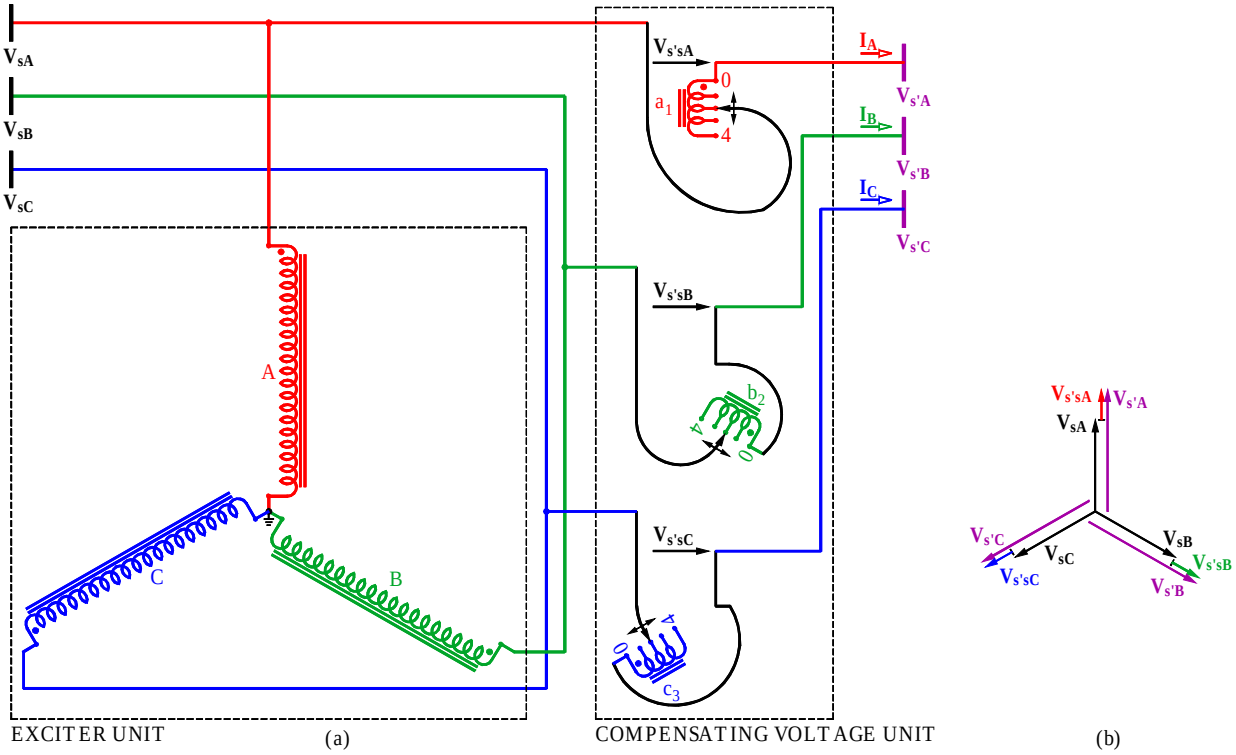


Figure 9-6. (a) Voltage regulating transformer for increasing line voltage. (b) Phasor diagram.

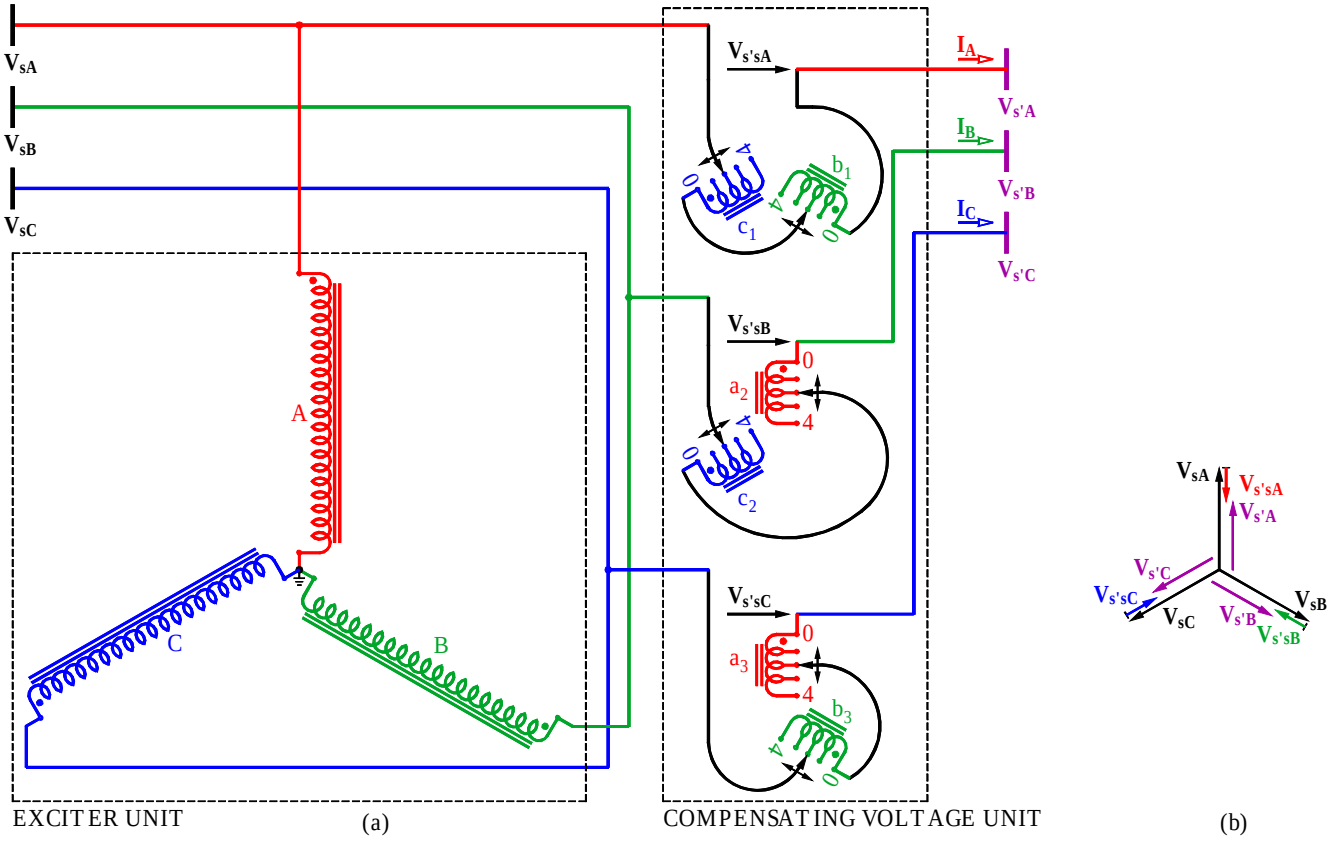


Figure 9-7. (a) Voltage regulating transformer for decreasing line voltage. (b) Phasor diagram.

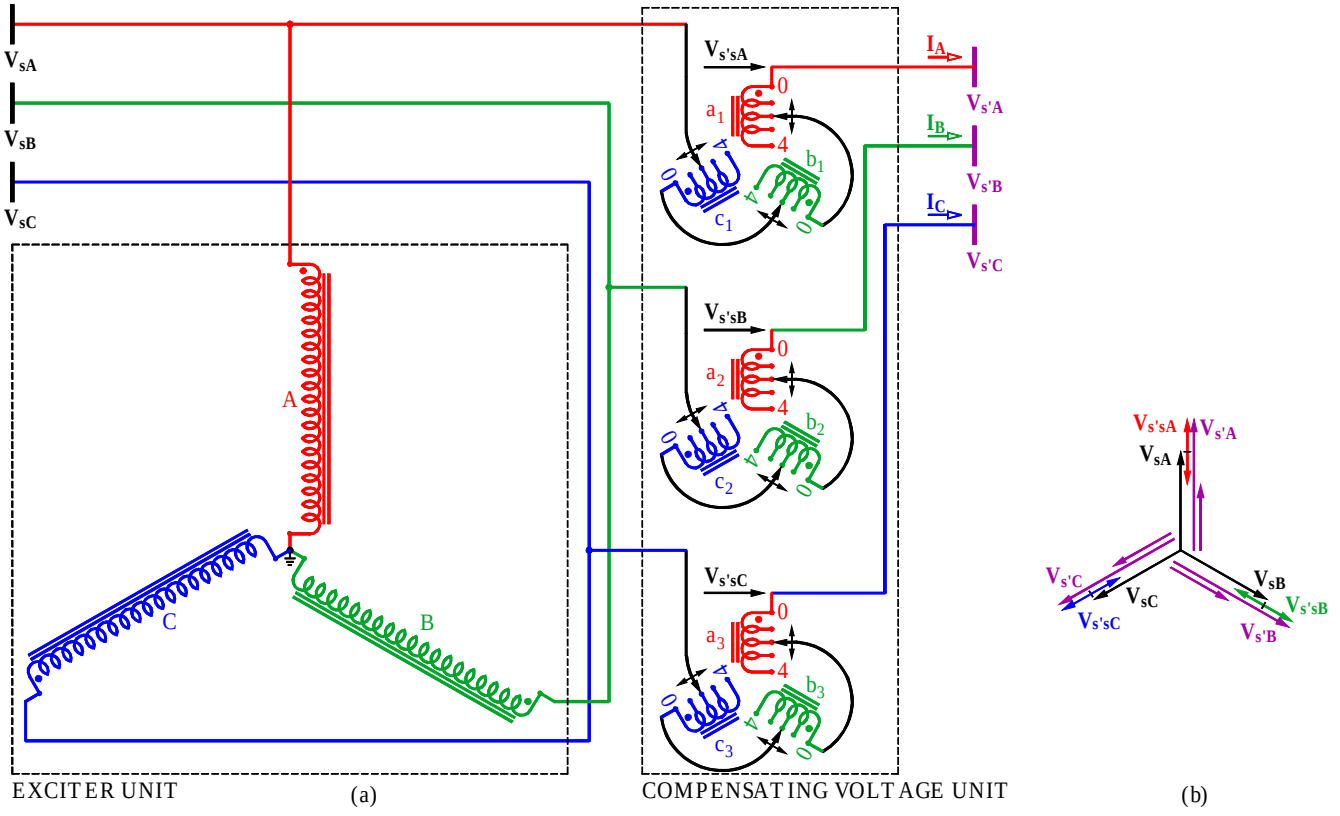


Figure 9-8. (a) ST for voltage regulation. (b) Phasor diagram.

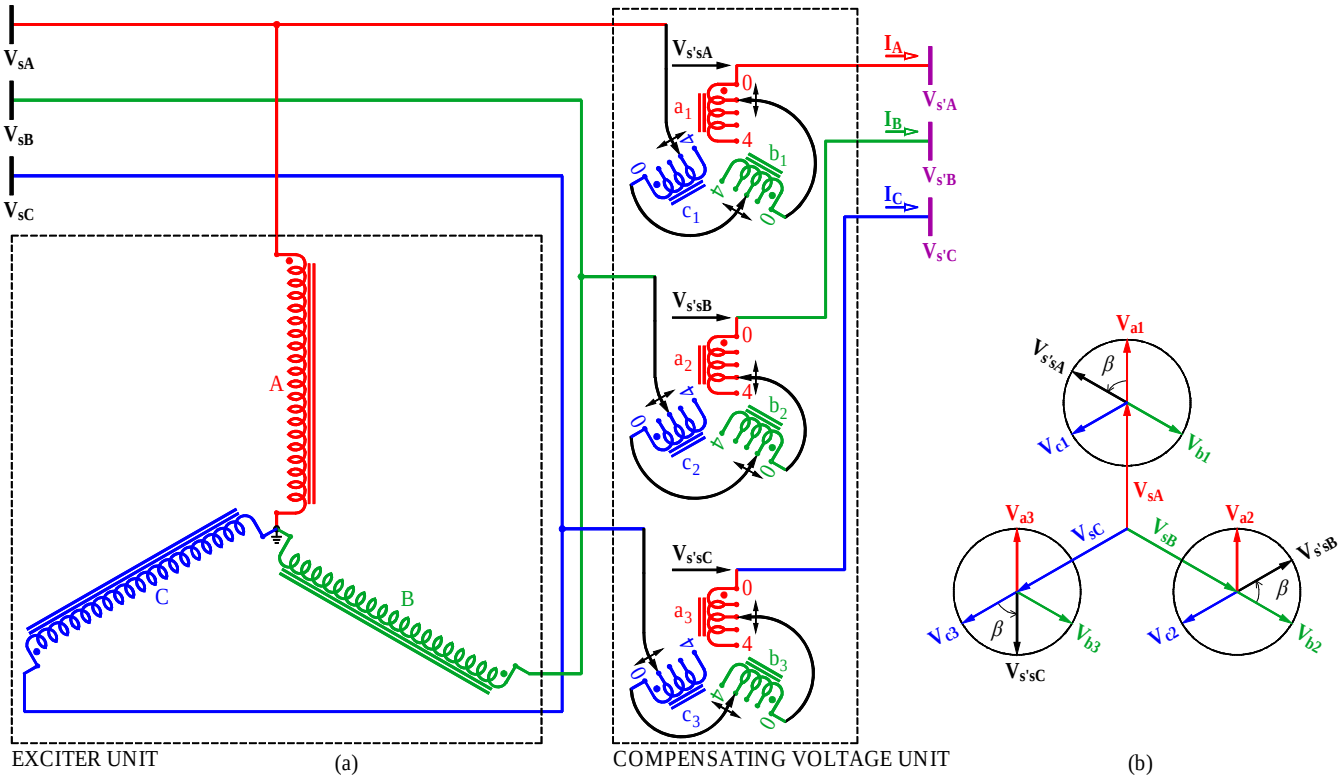


Figure 9-9. (a) ST for voltage compensation in the entire control range of 0^{o} through 360^{o}. (b) Phasor diagram.

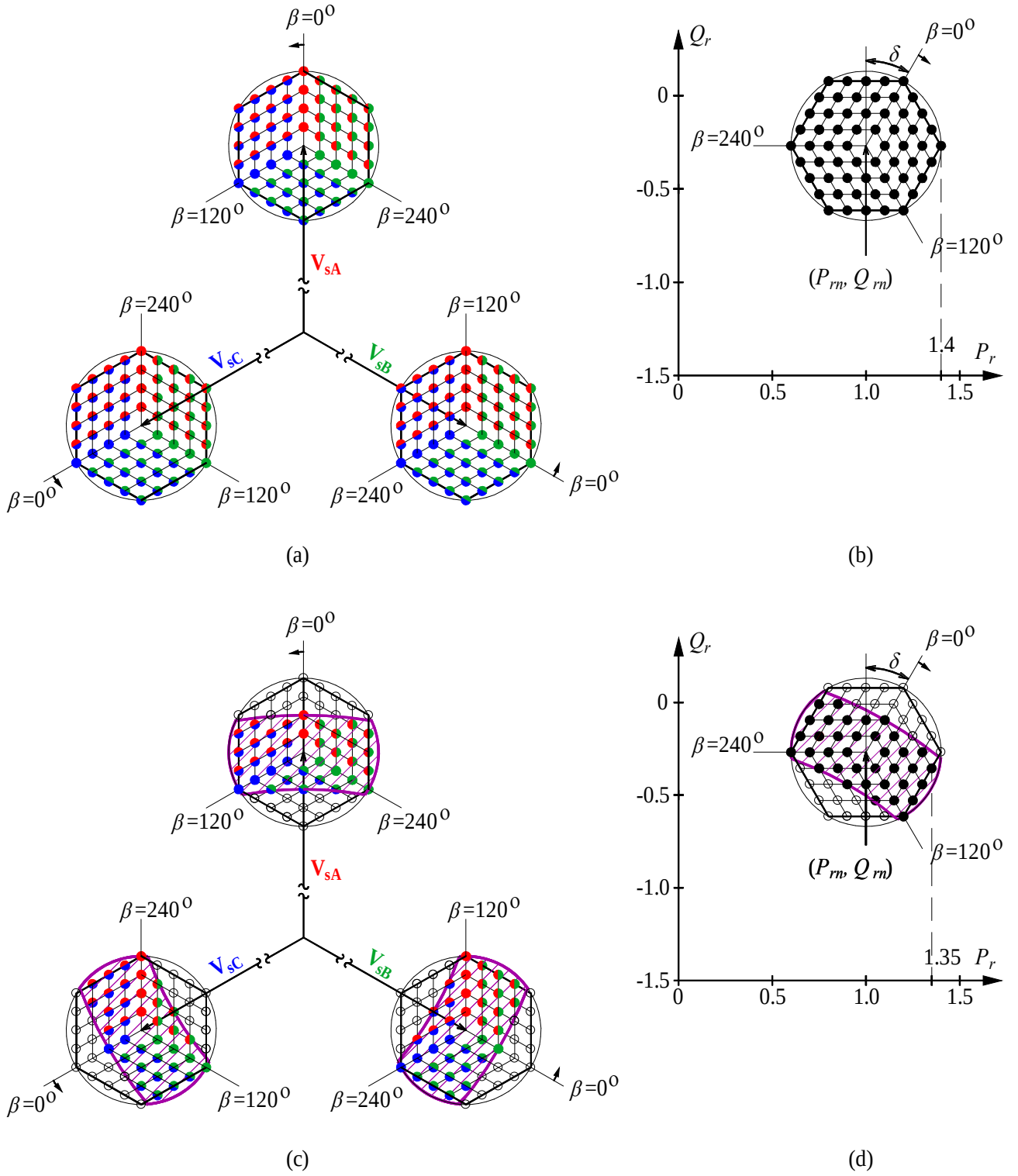


Figure 9-10. Compensating points with the use of the Sen transformer within the entire control range of 0° and 360°. Theoretically possible (a) modified sending-end voltage and (b) active and reactive power flows at the receiving end. Practically possible (c) modified sending-end voltage and (d) active and reactive power flows at the receiving end.

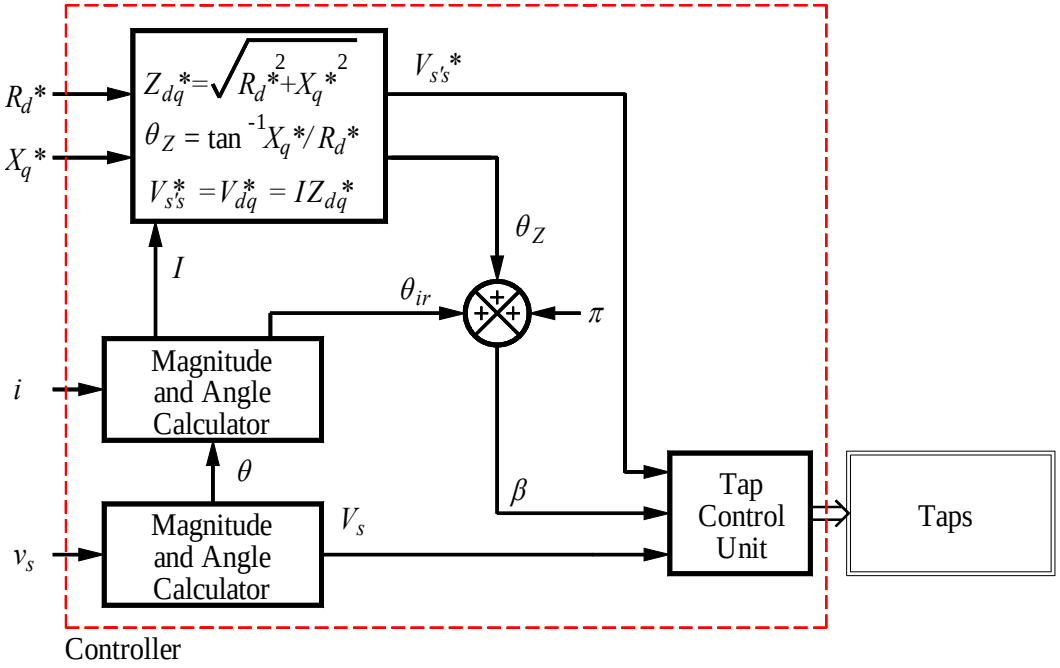


Figure 9-11. Series impedance emulation control block diagram of the ST.

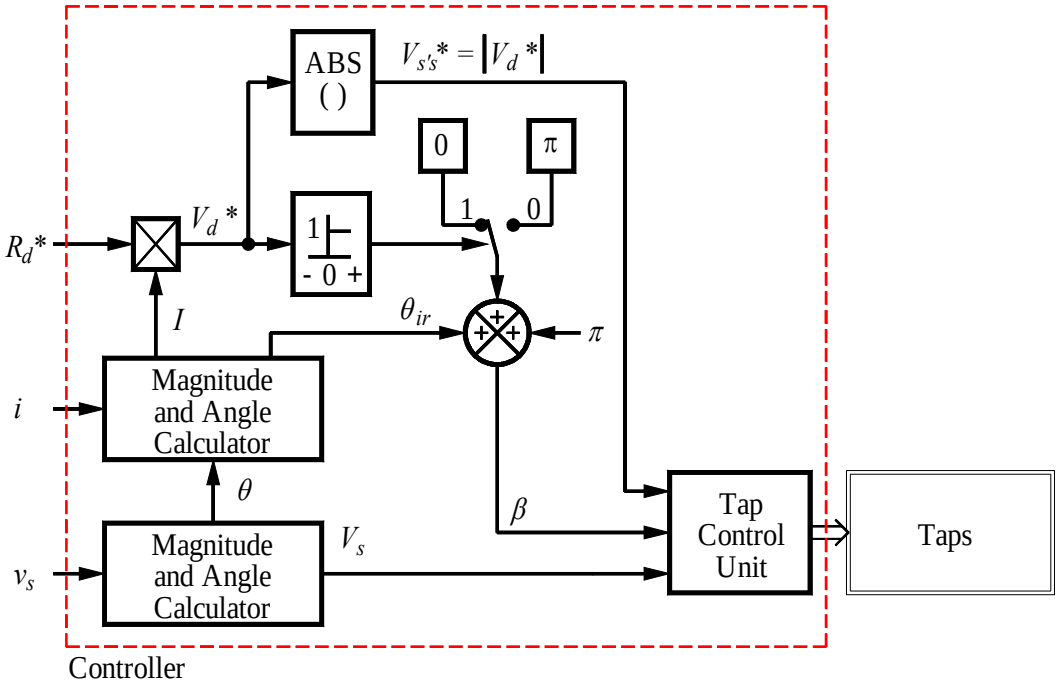


Figure 9-12. Series resistance emulation control block diagram of the ST.

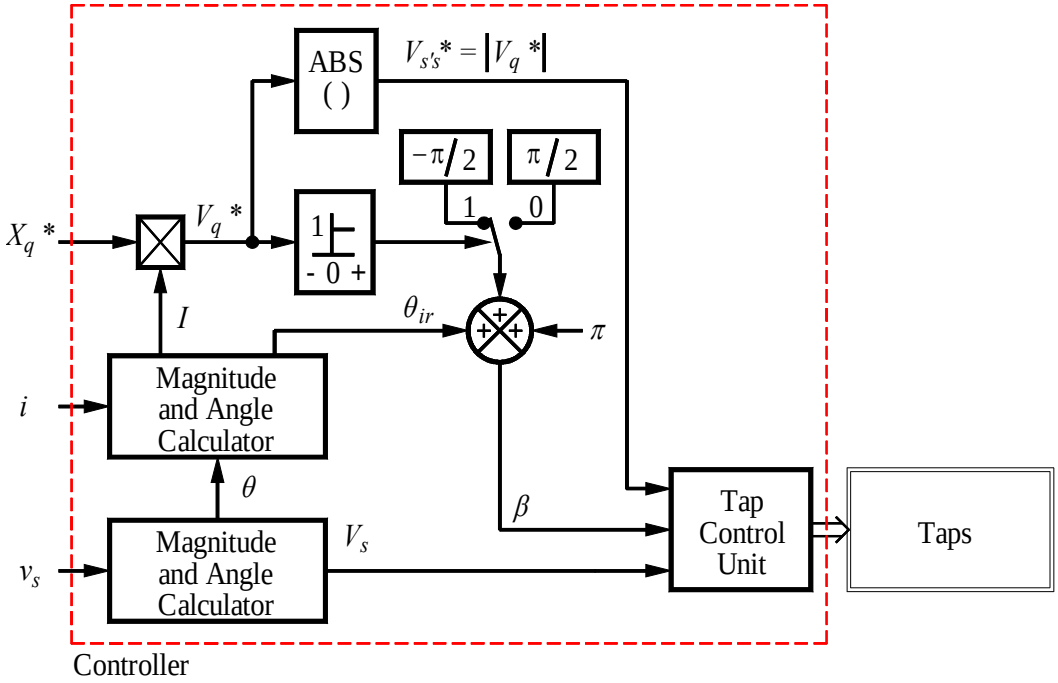


Figure 9-13. Series reactance emulation control block diagram of the ST.

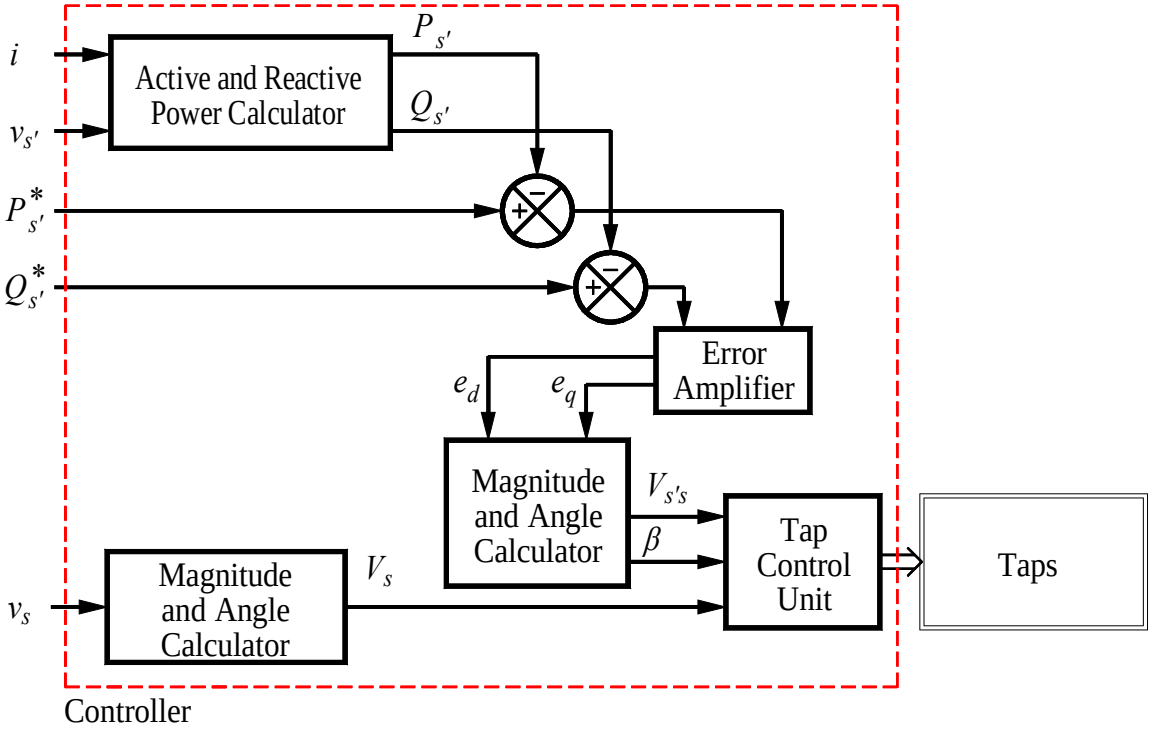


Figure 9-14. Closed loop automatic power flow control block diagram of the ST.

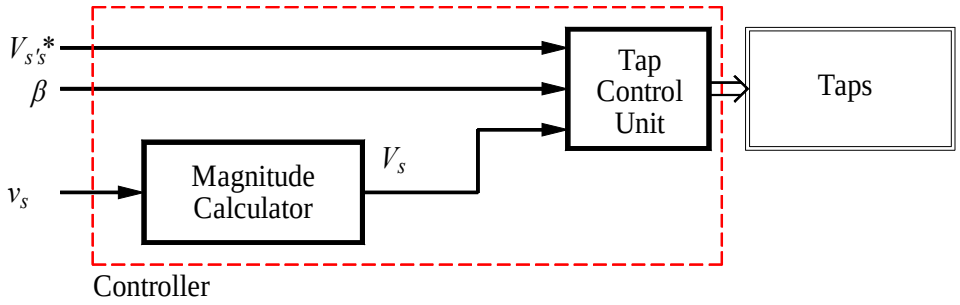


Figure 9-15. Open loop compensating voltage unit control block diagram of the ST.

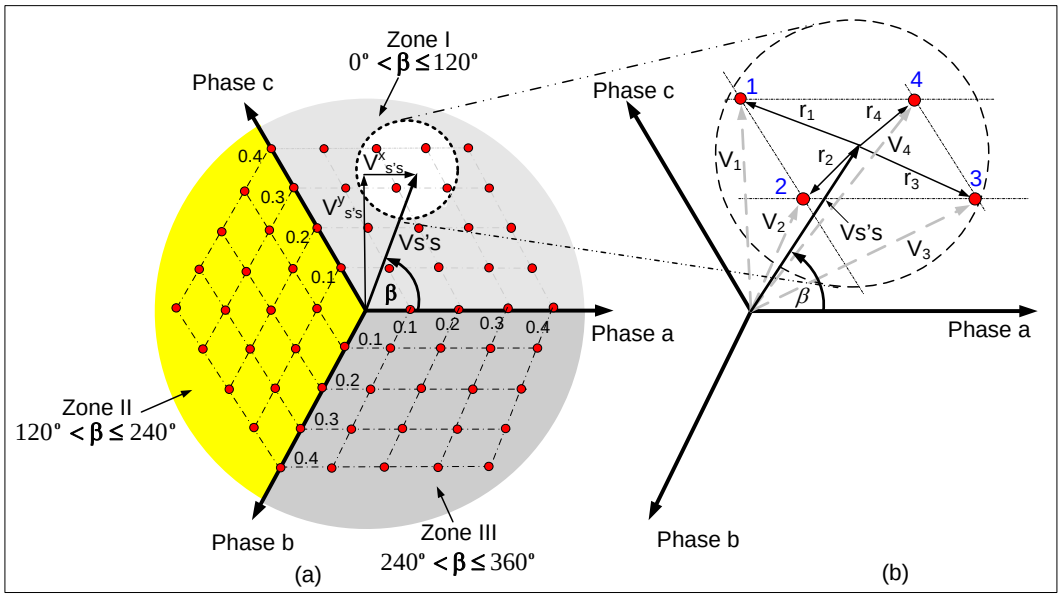


Figure 9-16. Selection of tap positions (Faruque & Dinavahi-2007).

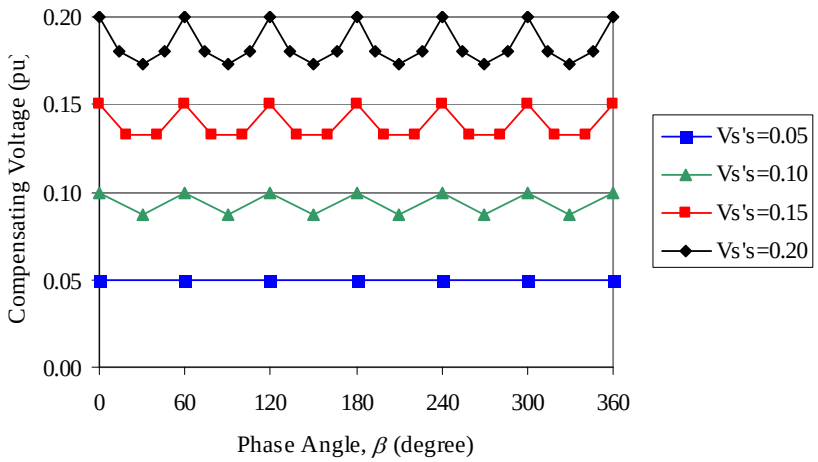
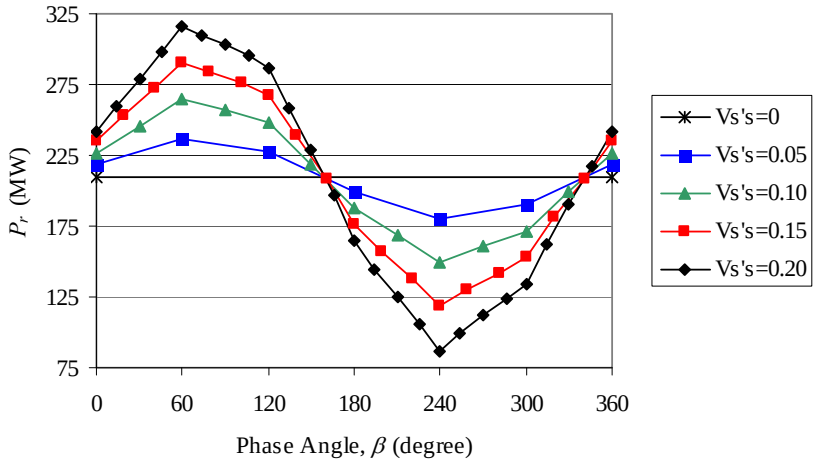
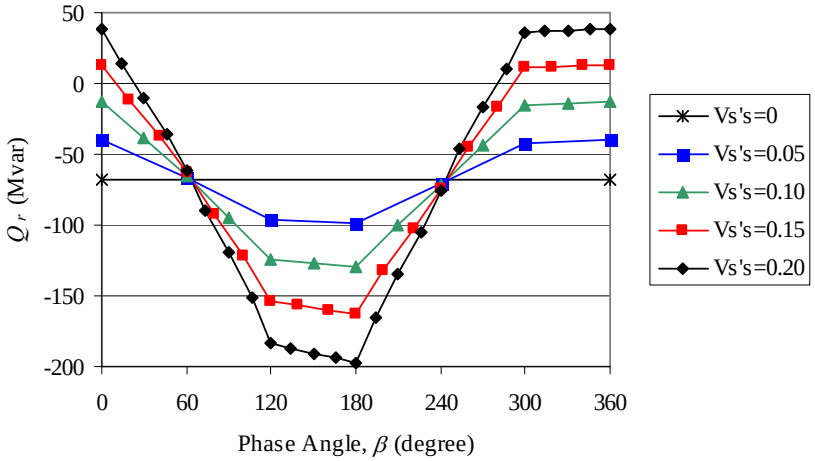


Figure 9-17. Magnitude of the series-connected compensating voltage ($V_{s's}$) in pu during the entire control range of its relative phase angle (β) from 0° and 360°.



(a)



(b)

Figure 9-18. (a) Active power (P_r) and (b) reactive power (Q_r) flows at the receiving end during the entire control range of the relative phase angle (β) from 0^o and 360^o.

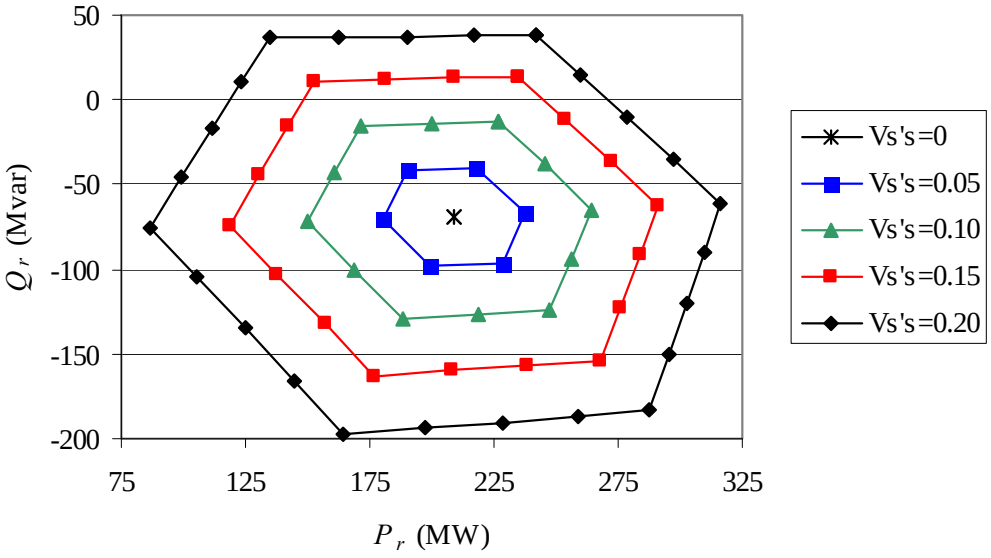


Figure 9-19. Active power (P_r) versus reactive power (Q_r) flows at the receiving end during the entire control range of the relative phase angle (β) from 0° and 360°.

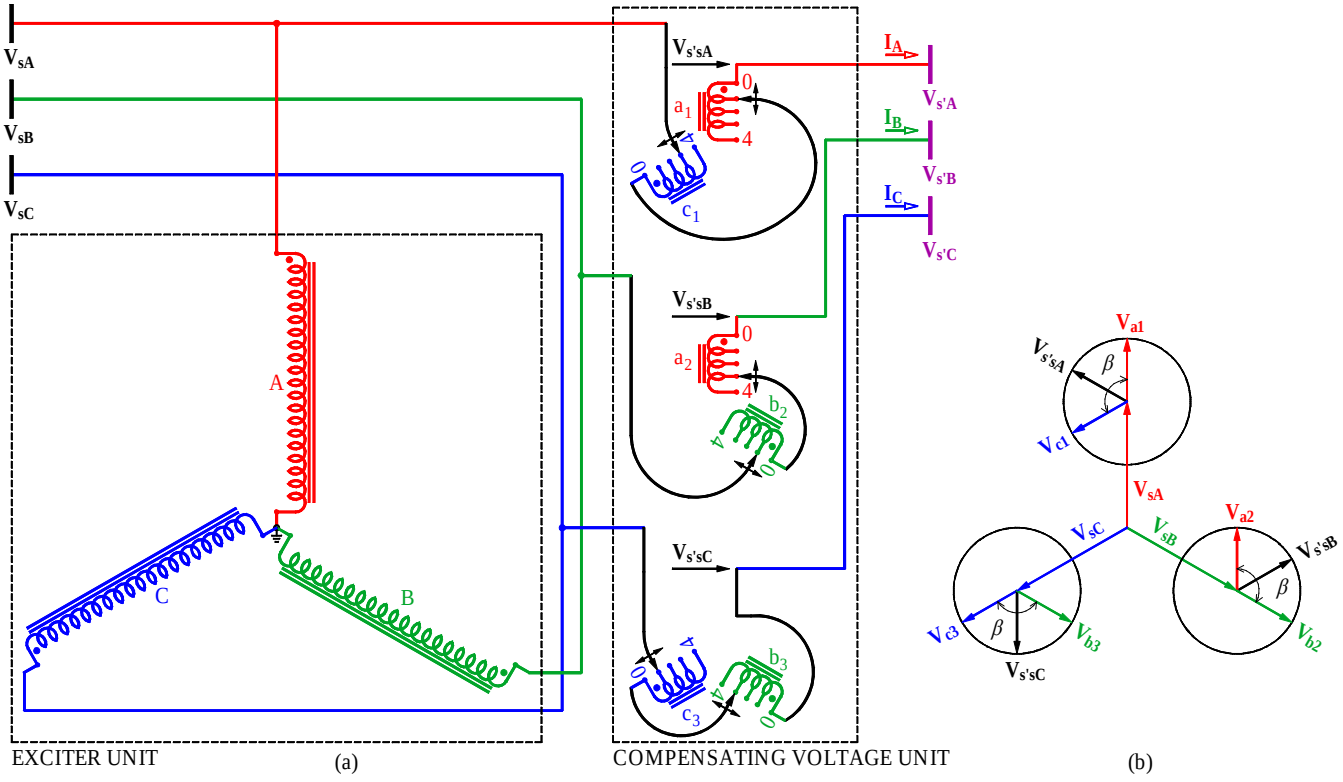
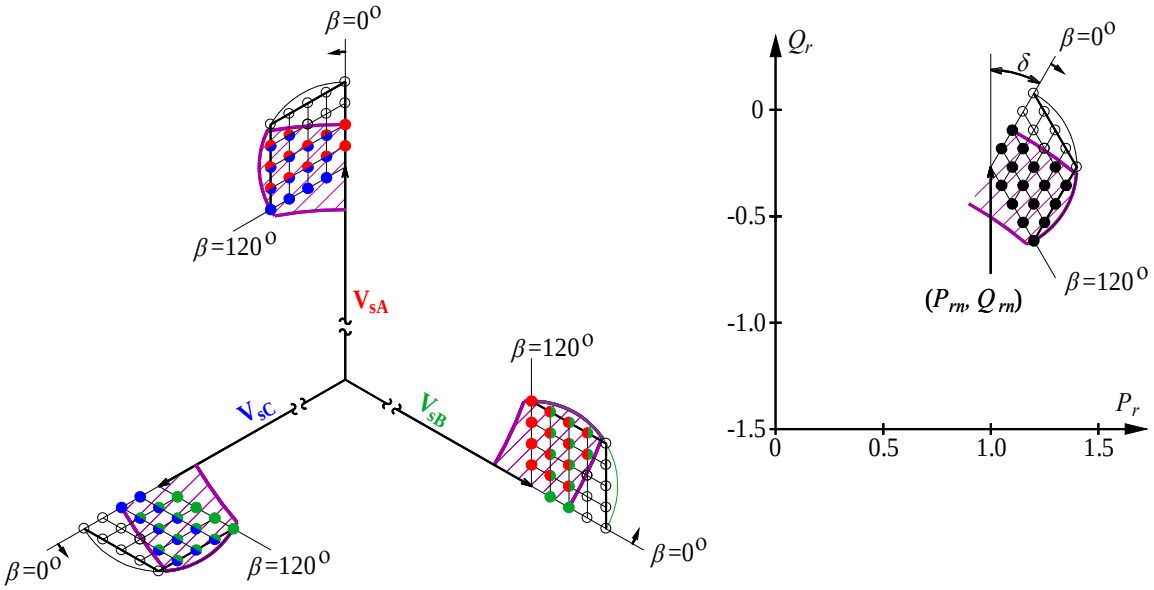


Figure 9-20(a, b). (a) ST for voltage compensation in the range of 0° through 120°. (b) Phasor diagram.



(c) (d)

Figure 9-20(c, d). (c) Modified sending-end voltage points. (d) Corresponding receiving-end active and reactive power points for operation within the control range of 0° and 120°.

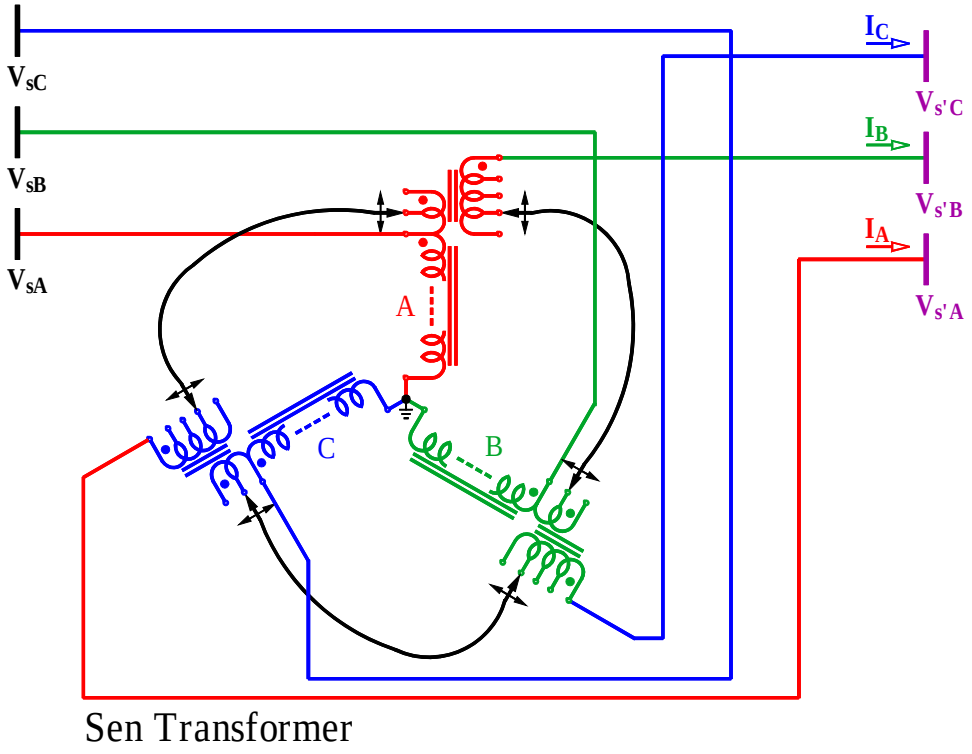


Figure 9-20(e). Most simplified configuration of the ST for operation in the range of 0° through 120°.

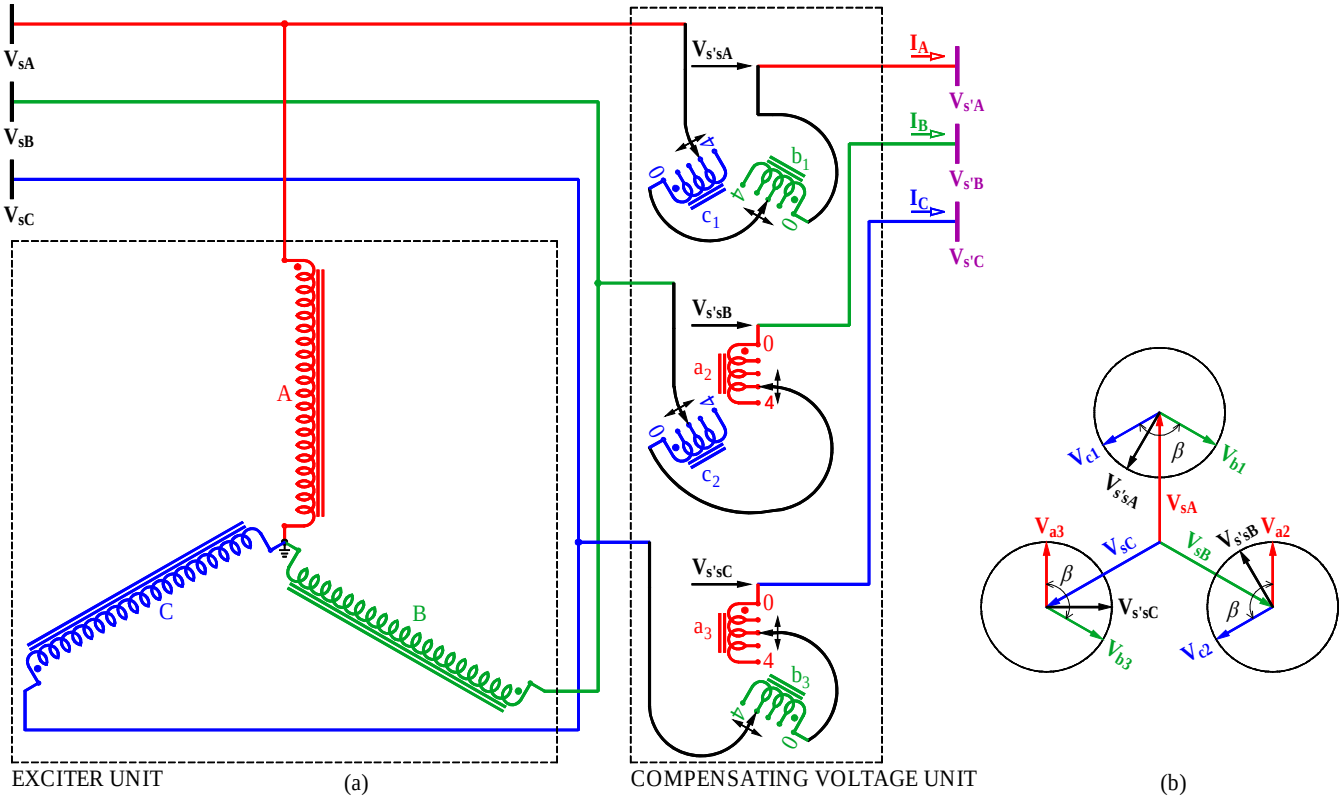


Figure 9-21(a, b). (a) ST for compensating voltage in the range of 120° through 240°. (b) Phasor diagram.

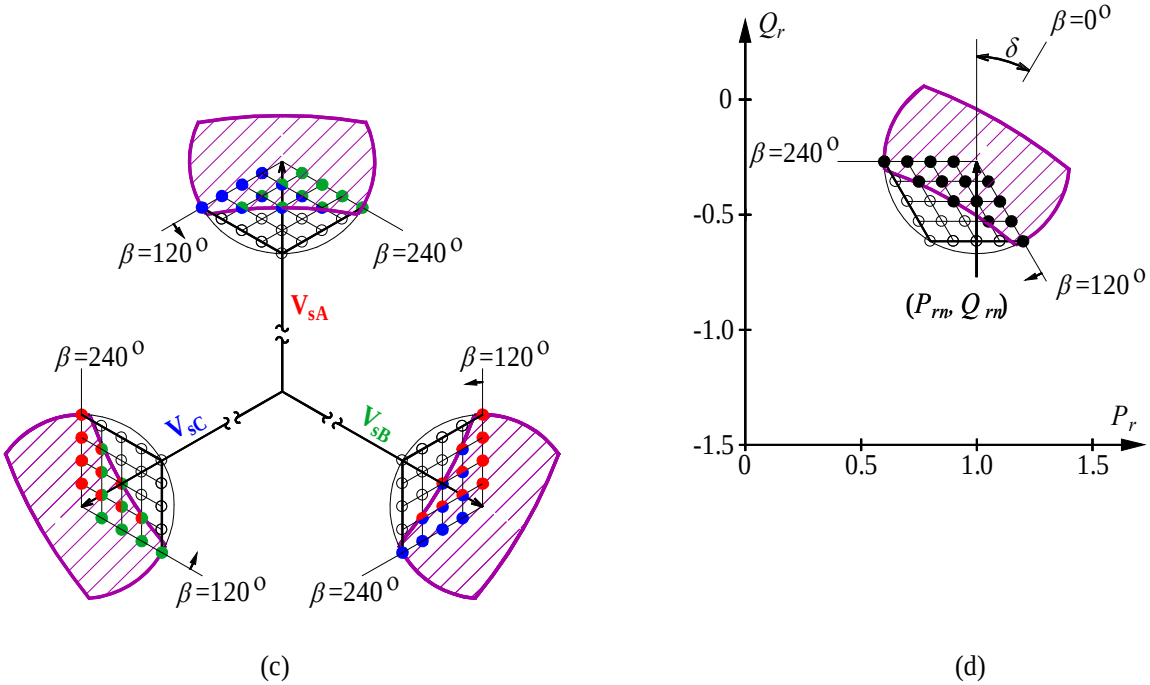


Figure 9-21(c, d). (c) Modified sending-end voltage points. (d) Corresponding receiving-end active and reactive power points for operation within the control range of 120° and 240°.

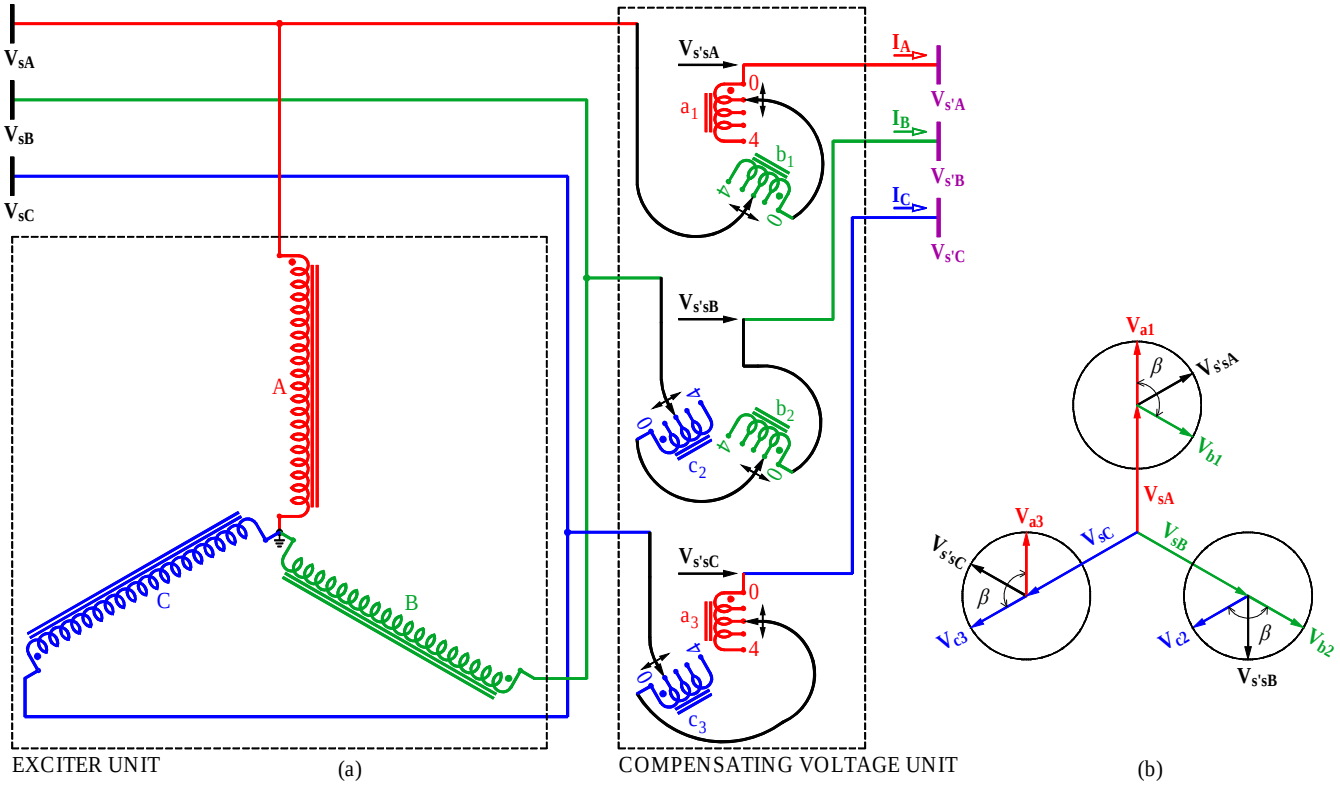


Figure 9-22(a, b). (a) ST for compensating voltage in the range of 240° through 360°. (b) Phasor diagram.

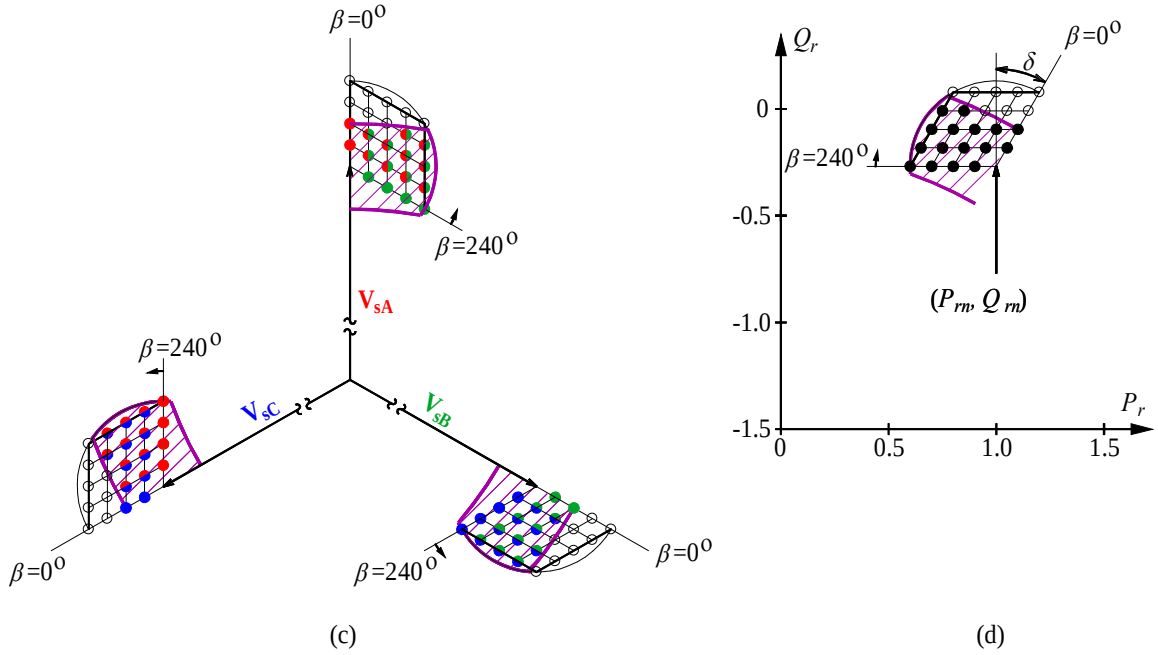


Figure 9-22(c, d). (c) Modified sending-end voltage points. (d) Corresponding receiving-end active and reactive power points for operation within the control range of 240° and 360°.

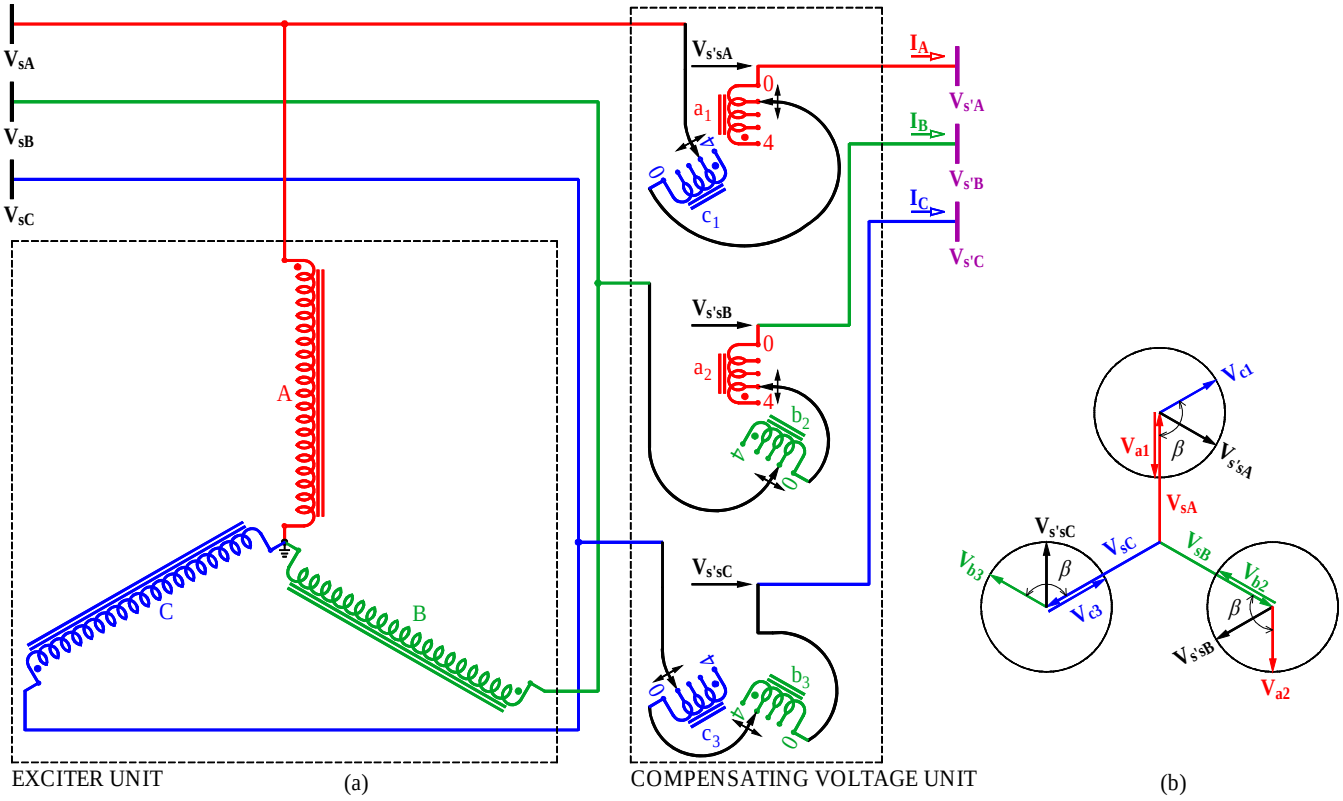


Figure 9-23. (a) ST for compensating voltage in the range of 180° through 300°. (b) Phasor diagram.

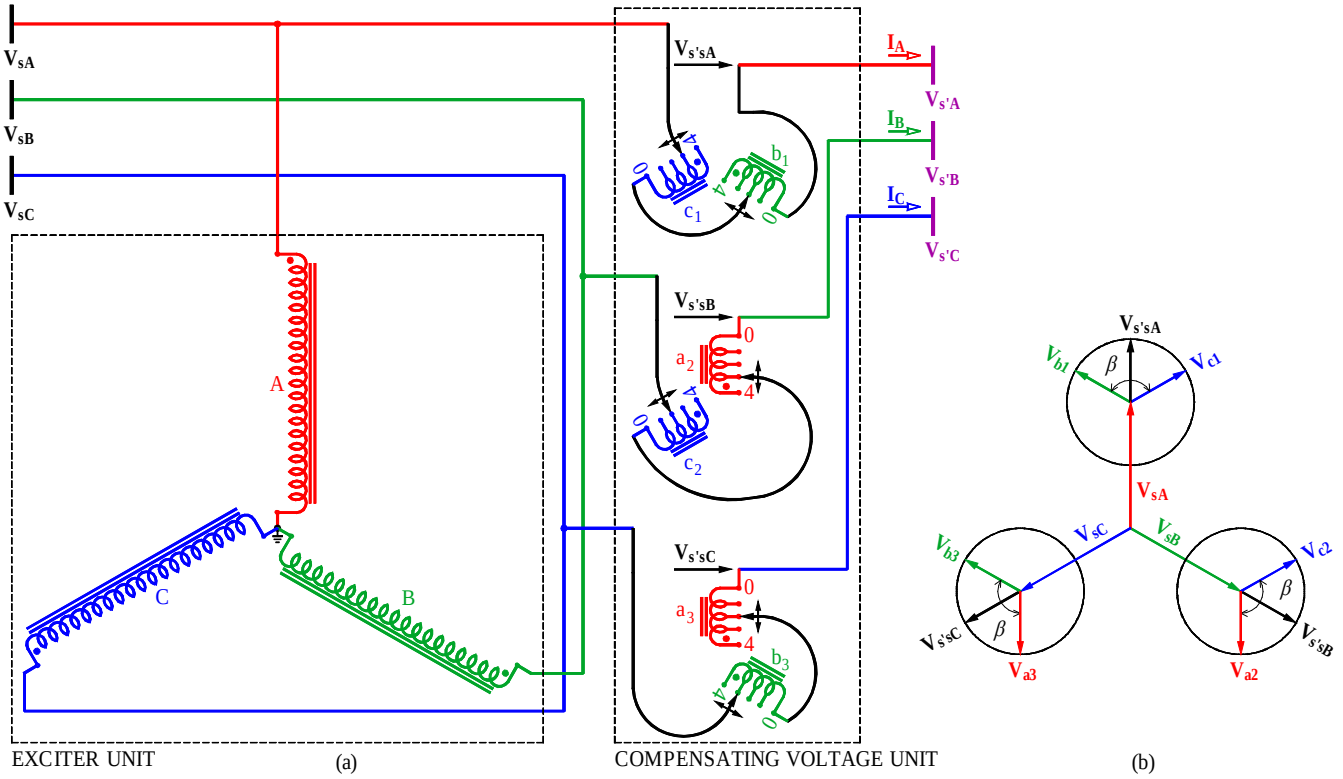


Figure 9-24. (a) ST for compensating voltage in the range of 300° through 60°. (b) Phasor diagram.

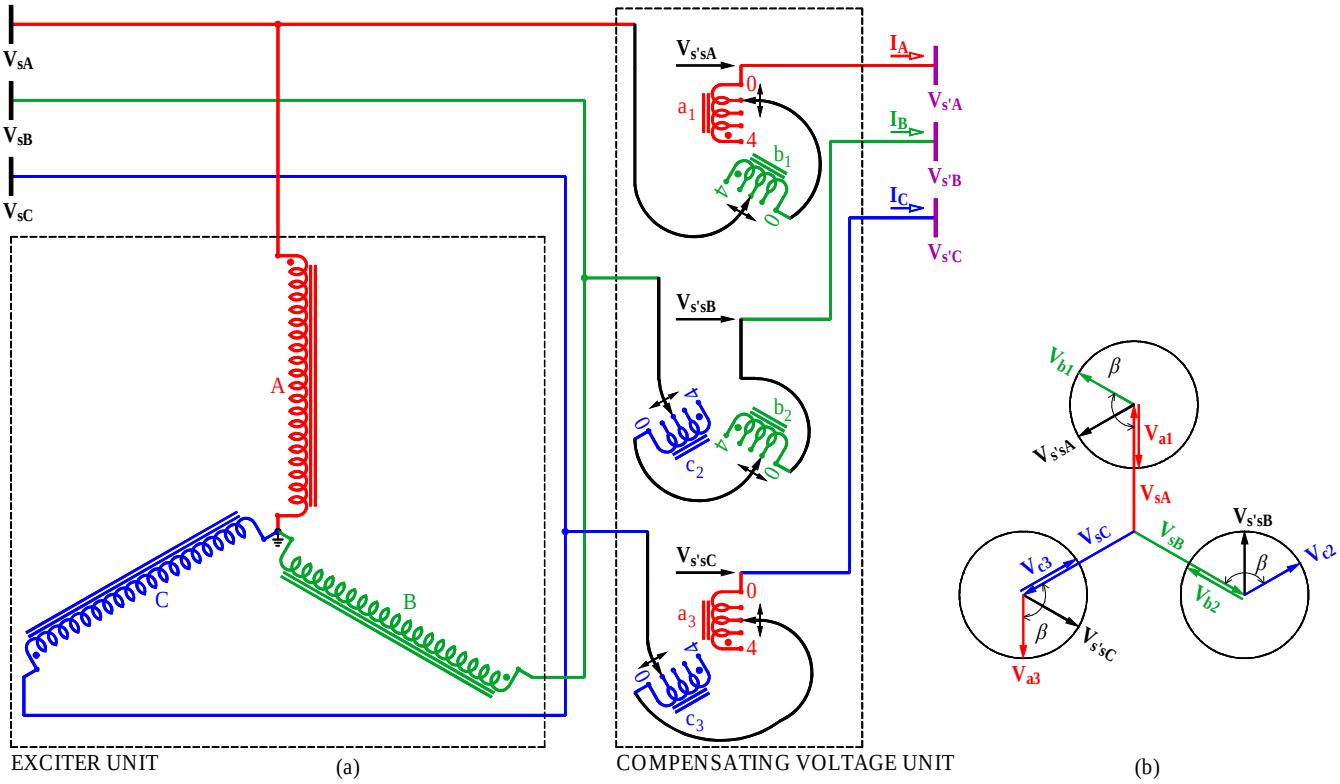


Figure 9-25. (a) ST for compensating voltage in the range of 60° through 180°. (b) Phasor diagram.

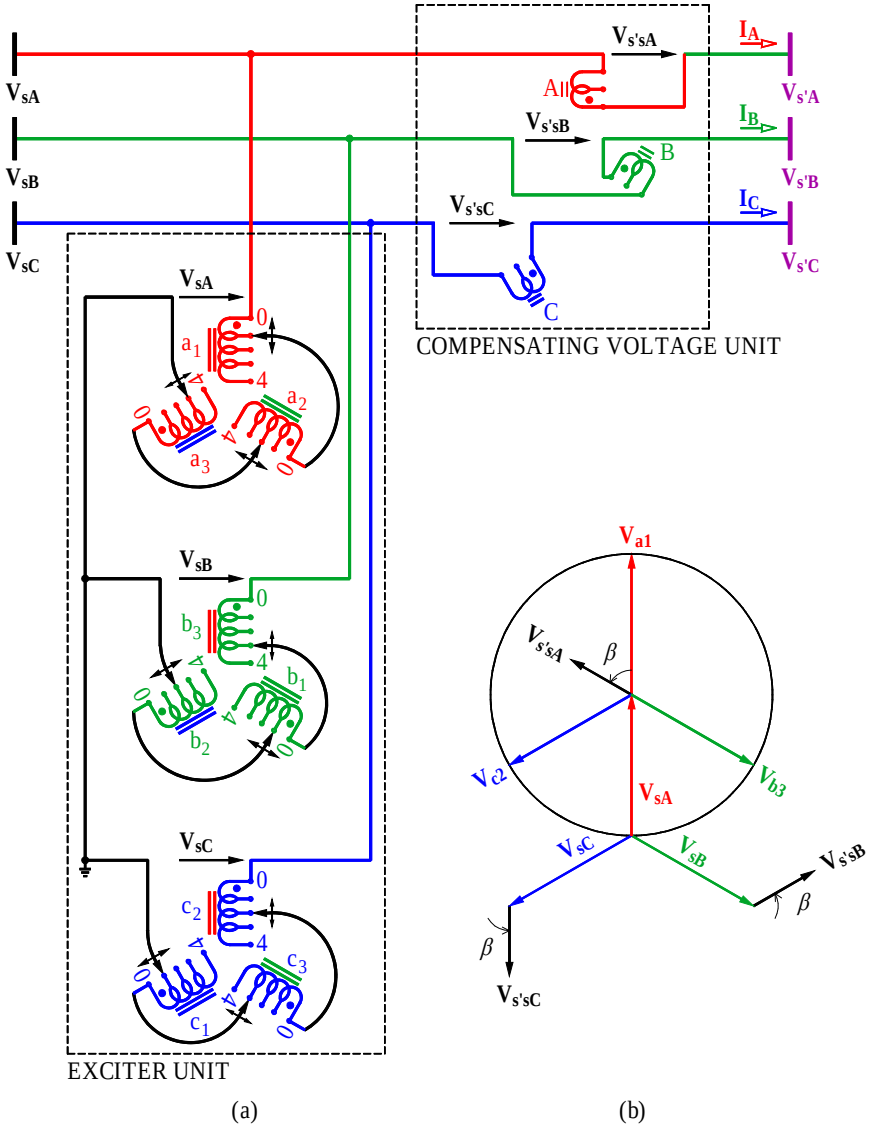


Figure 9-26(a, b). (a) ST configuration using LTCs with lower current rating. (b) Phasor diagram for compensating voltage with variable magnitude and phase angle.

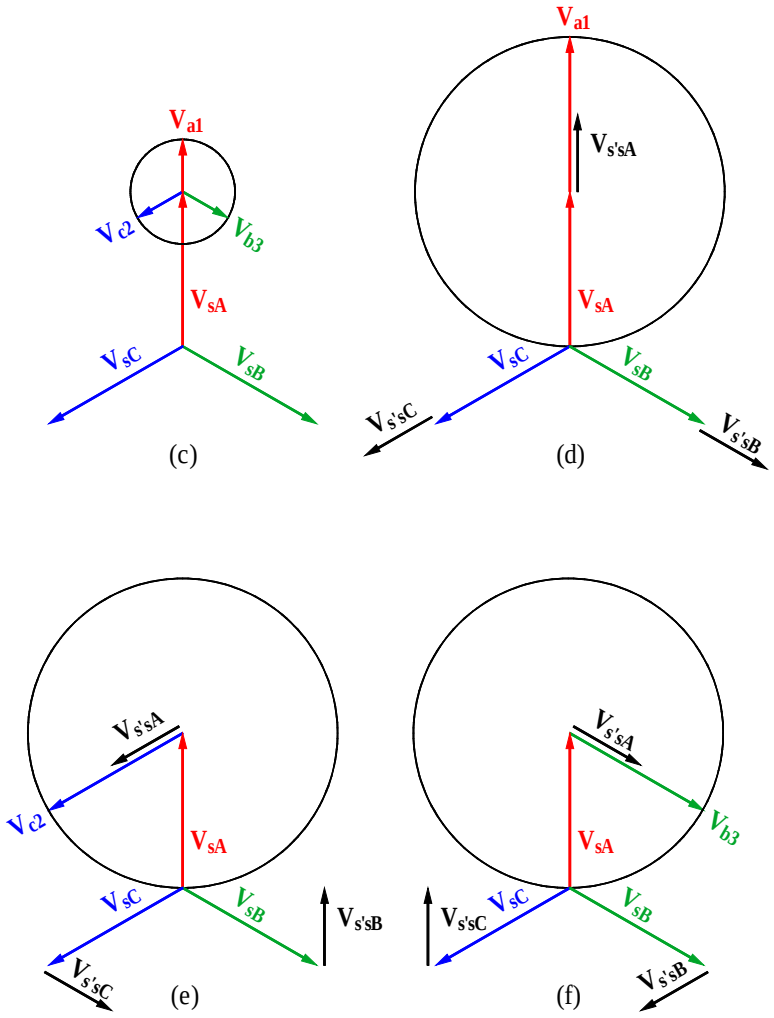


Figure 9-26(c, d, e, f). Phasor diagrams for (c) zero compensating voltage, (d) in-phase compensating voltage with variable magnitude, (e) 120^{o} leading compensating voltage with variable magnitude, and (f) 120^{o} lagging compensating voltage with variable magnitude.

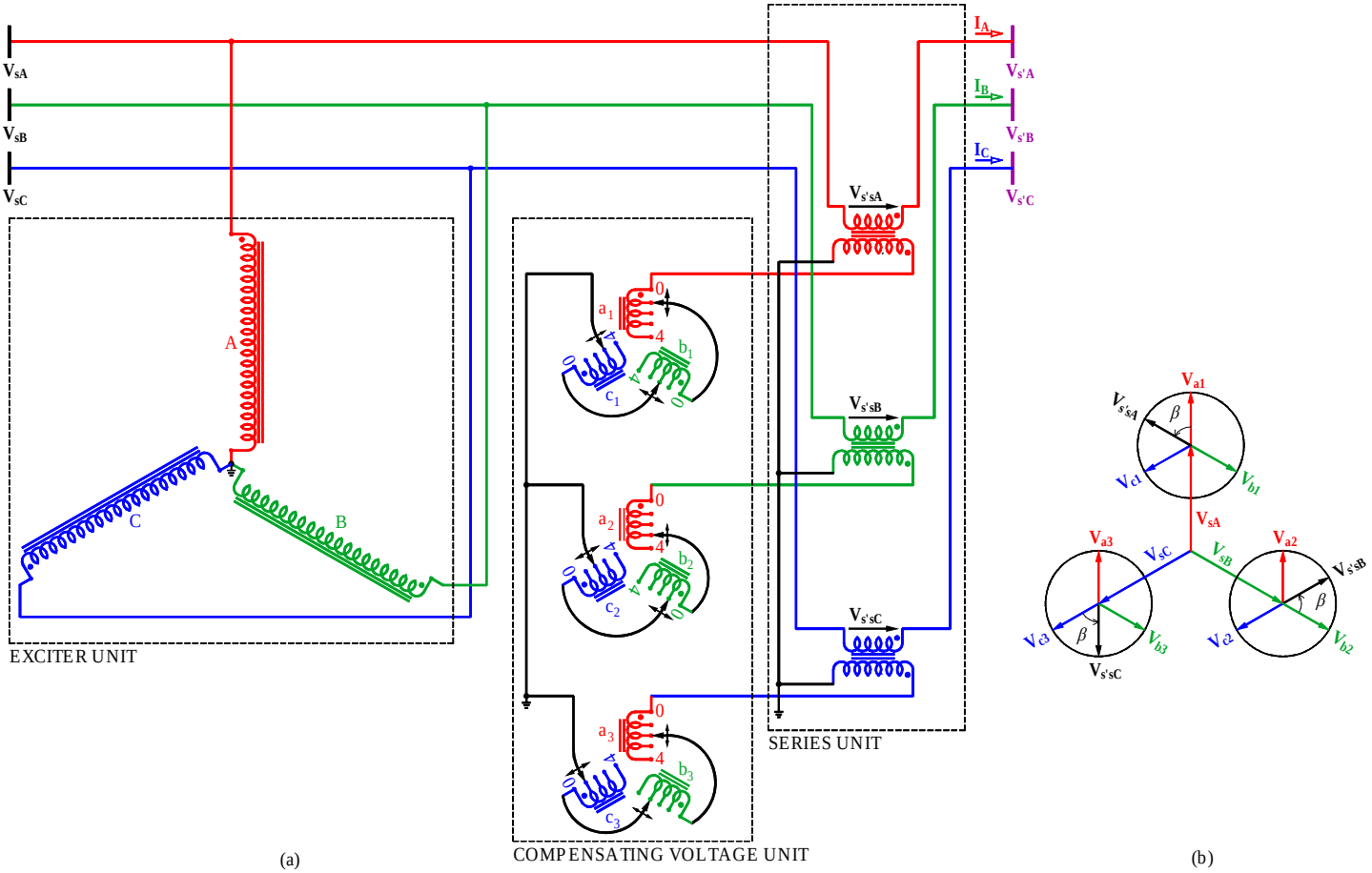
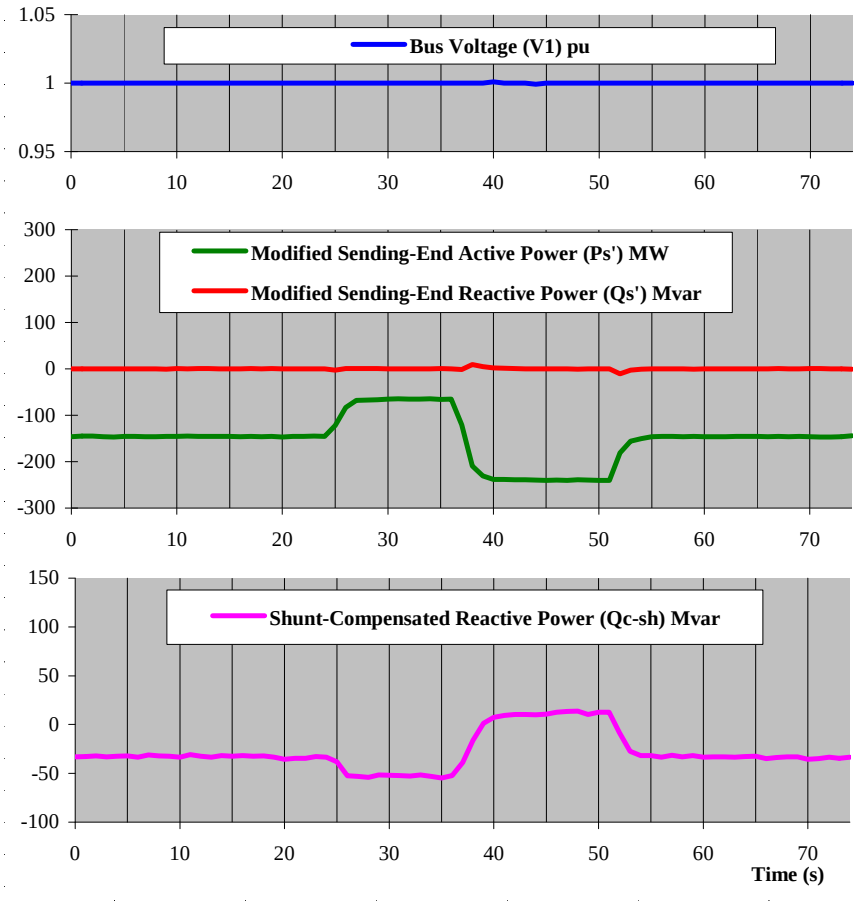
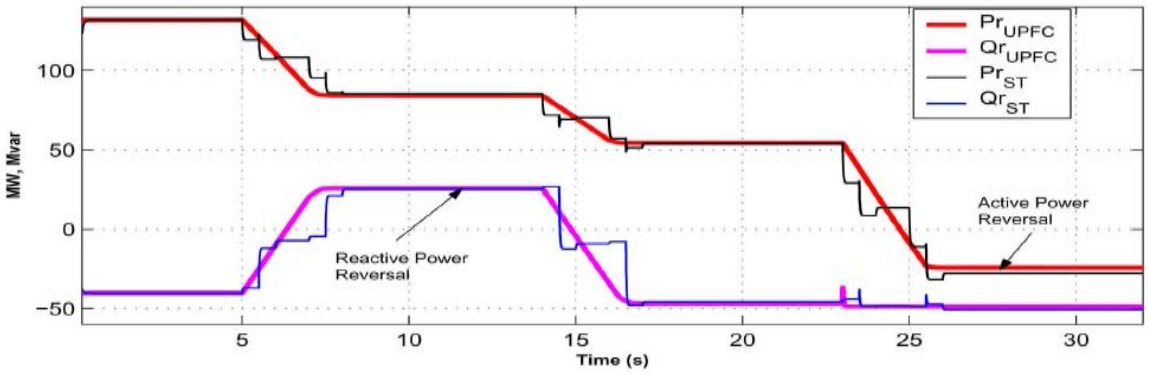


Figure 9-27. (a) ST configuration using taps with lower voltage and current ratings. (b) Phasor diagram.



(a)



(b)

Figure 9-28. (a) UPFC test results for automatic power flow control mode of operation with maintaining unity power factor and one pu bus voltage while regulating the line power (Sen & Keri-2002). (b) ST simulation results for open loop power flow control mode of operation (Faruque & Dinavahi-2007).

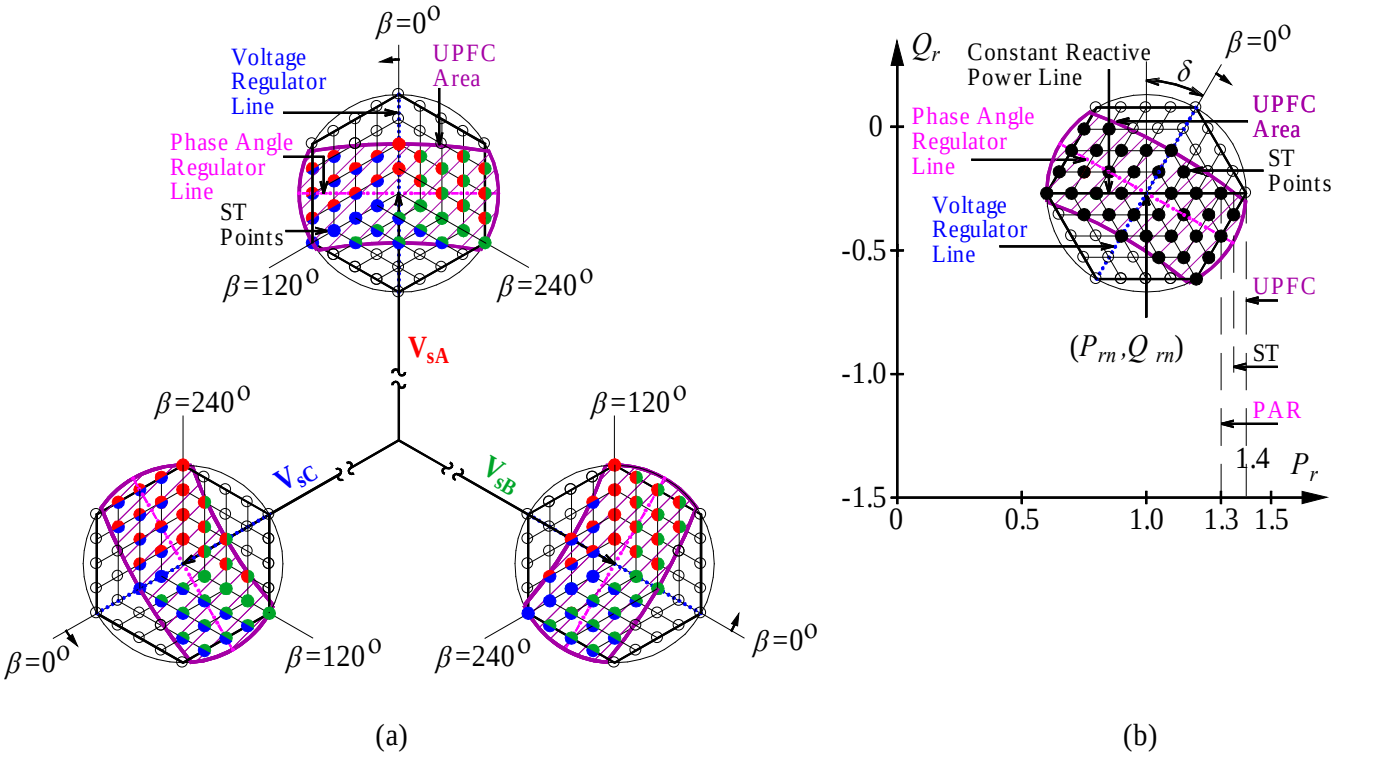


Figure 9-29. Practical voltage compensation range with the use of the VRT, PAR, UPFC, and ST within the control range of relative phase angle (β) from 0° and 360°: (a) modified sending-end voltage and (b) active and reactive power flows at the receiving end.

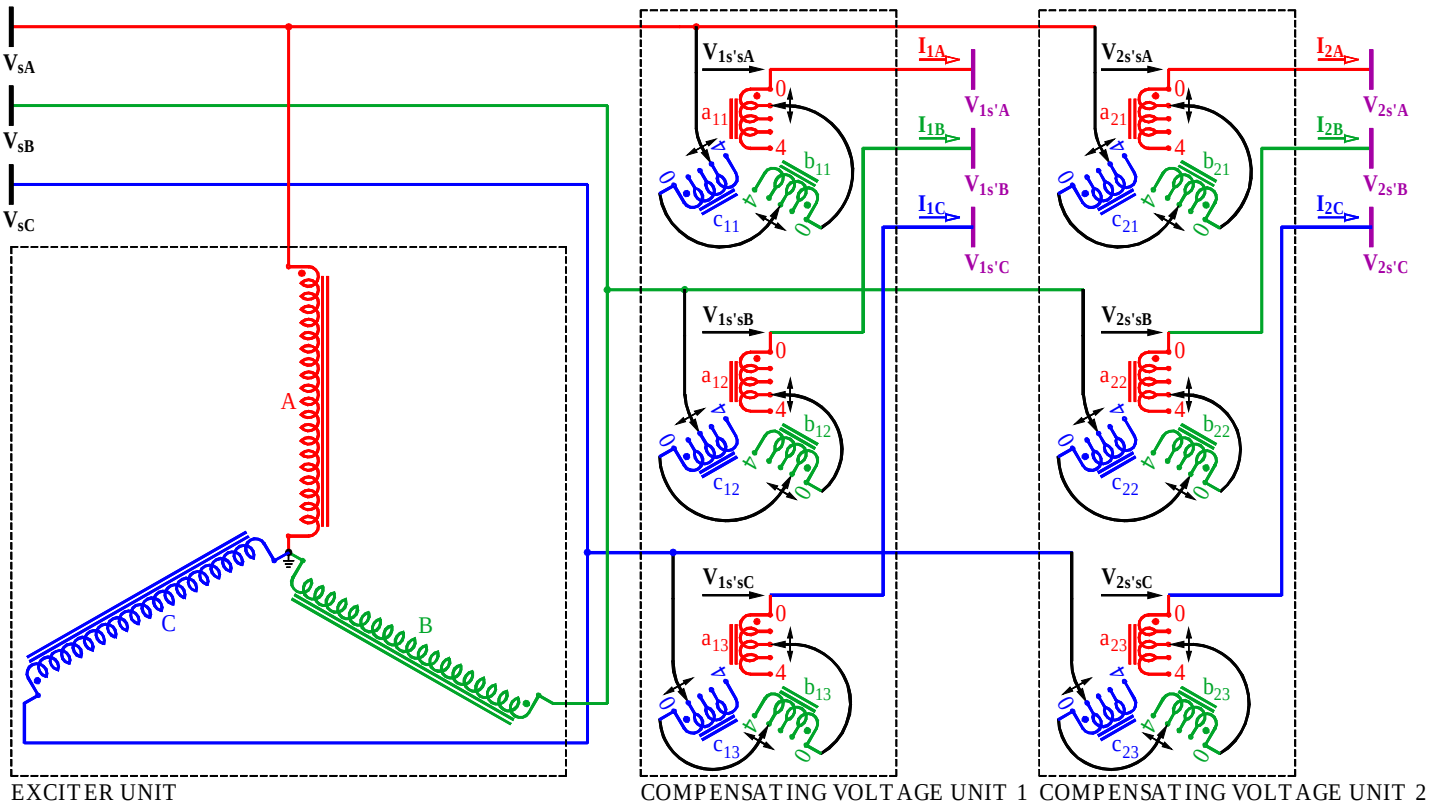


Figure 9-30. Multiline Sen transformer.

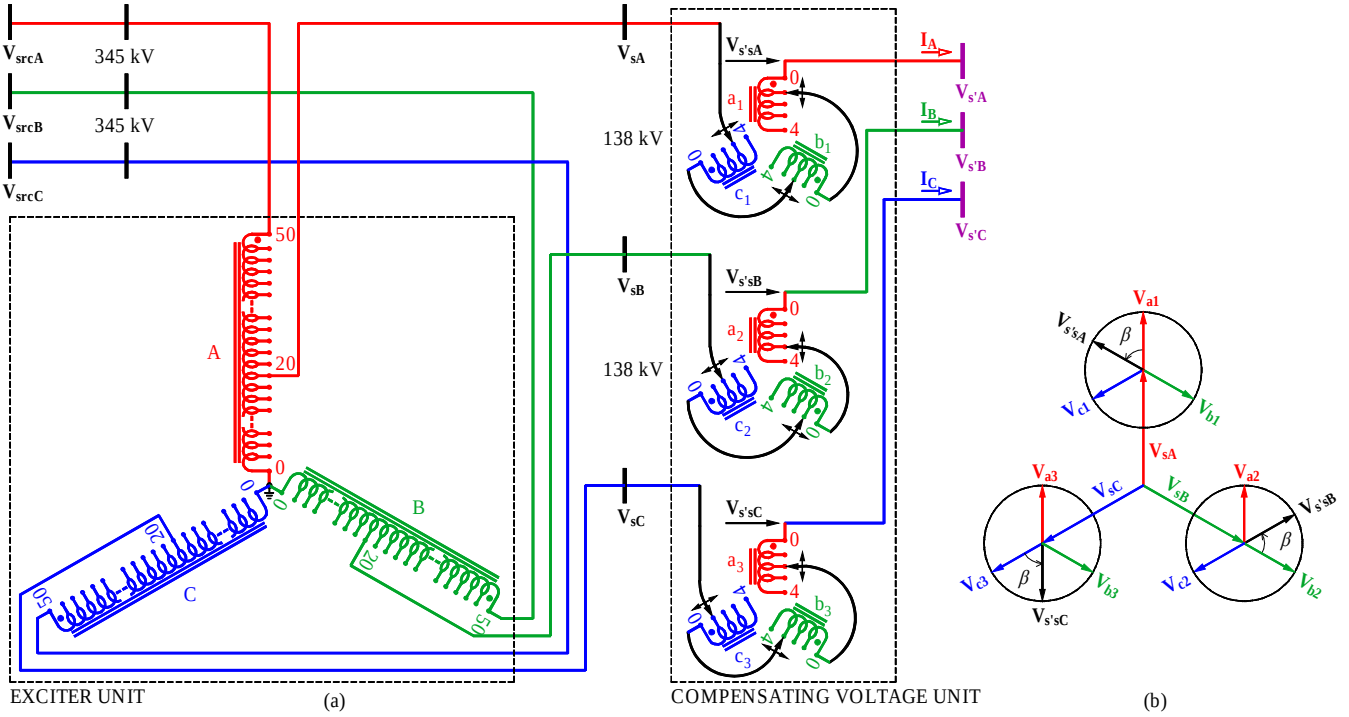


Figure 9-31. (a) ST's compensating voltage unit is connected to the stepped down voltage of a transmission line. (b) Phasor diagram.

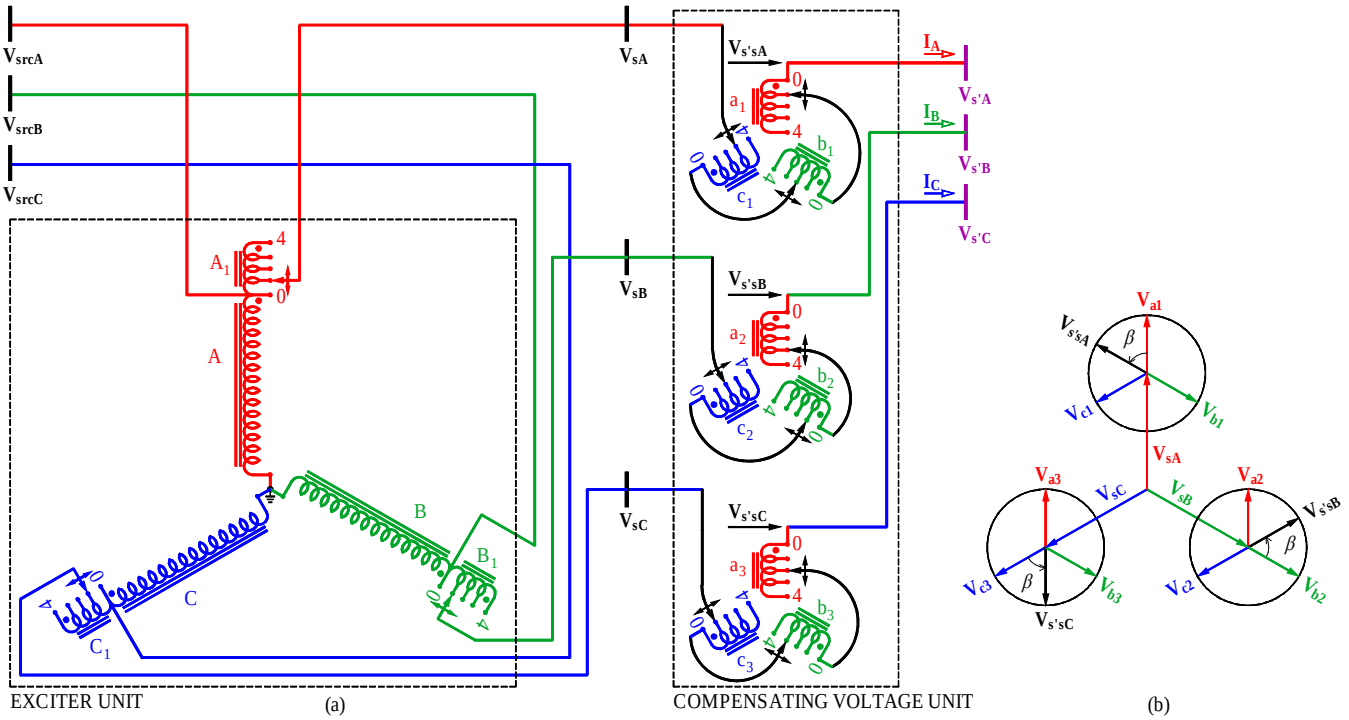


Figure 9-32. (a) ST's compensating voltage unit is connected to the stepped up voltage of a transmission line. (b) Phasor diagram.

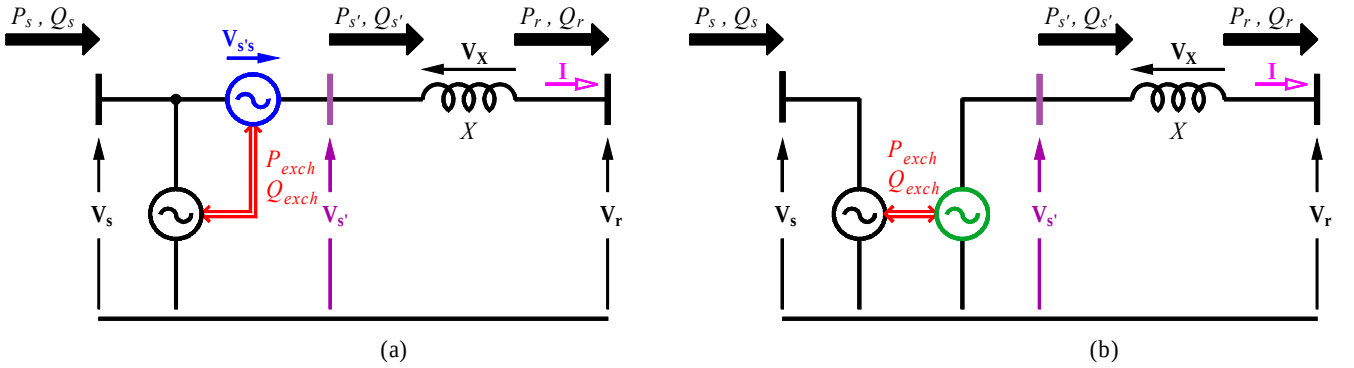


Figure 9-33. Two methods of modifying a transmission line voltage: (a) with a series-connected compensating voltage, (b) with a shunt-connected compensating voltage.

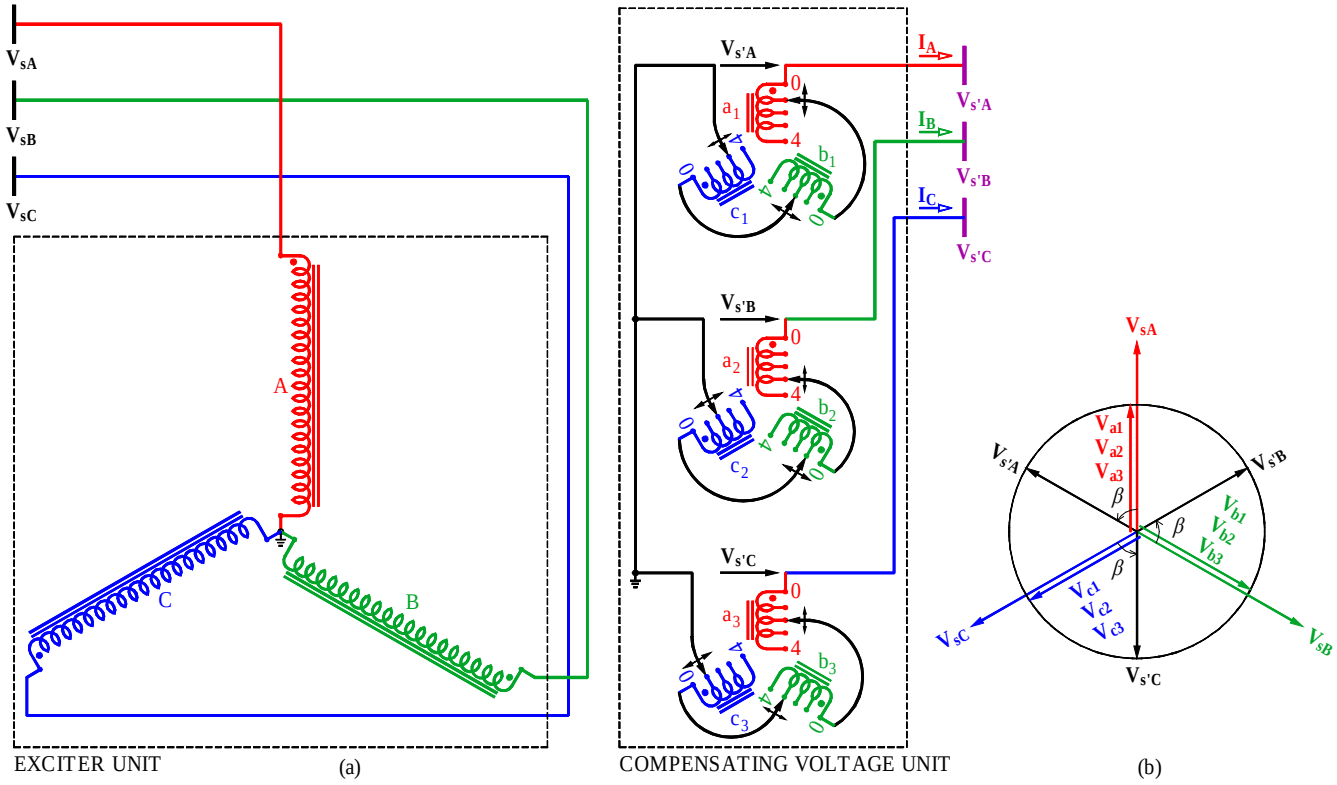


Figure 9-34. (a) Shunt-connected compensating voltage in the ST. (b) Phasor diagram.

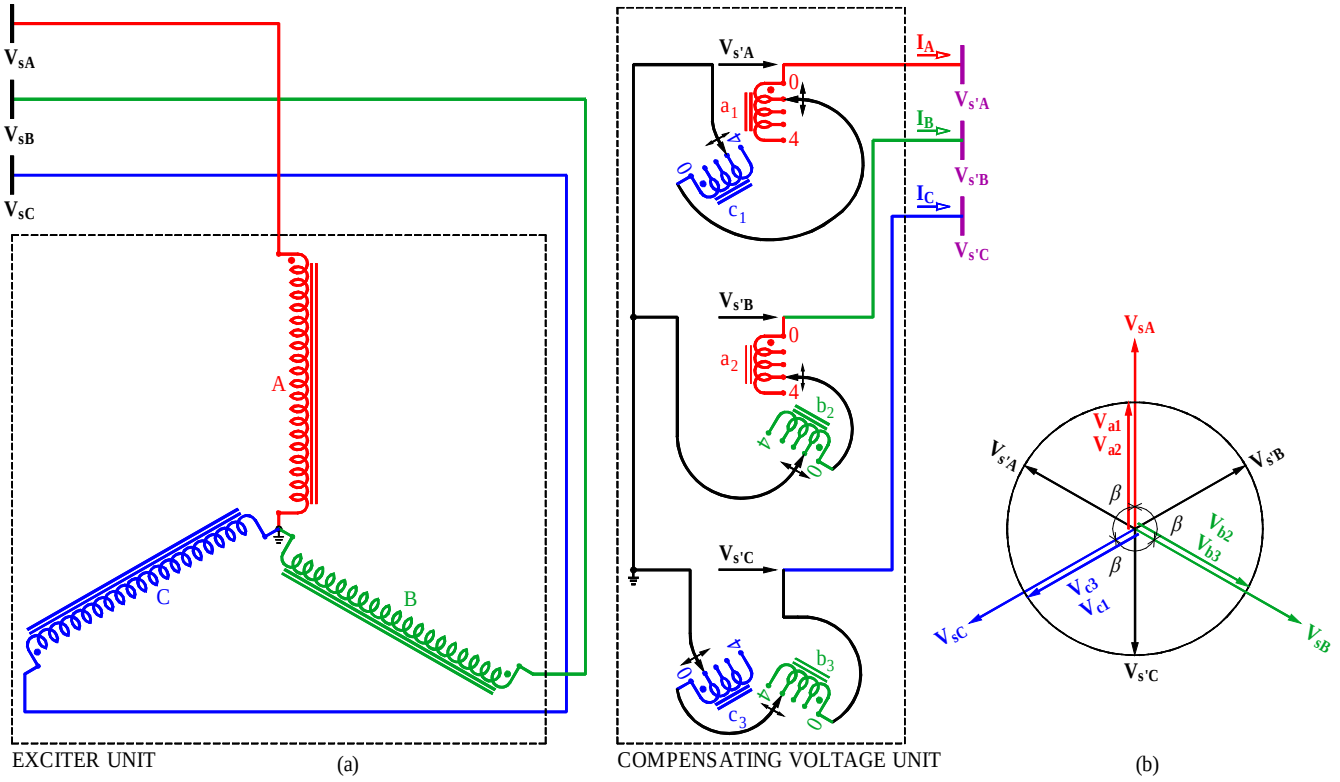


Figure 9-35. (a) ST with shunt-connected compensating voltage unit operating in the range of 0° through 120°. (b) Phasor diagram.

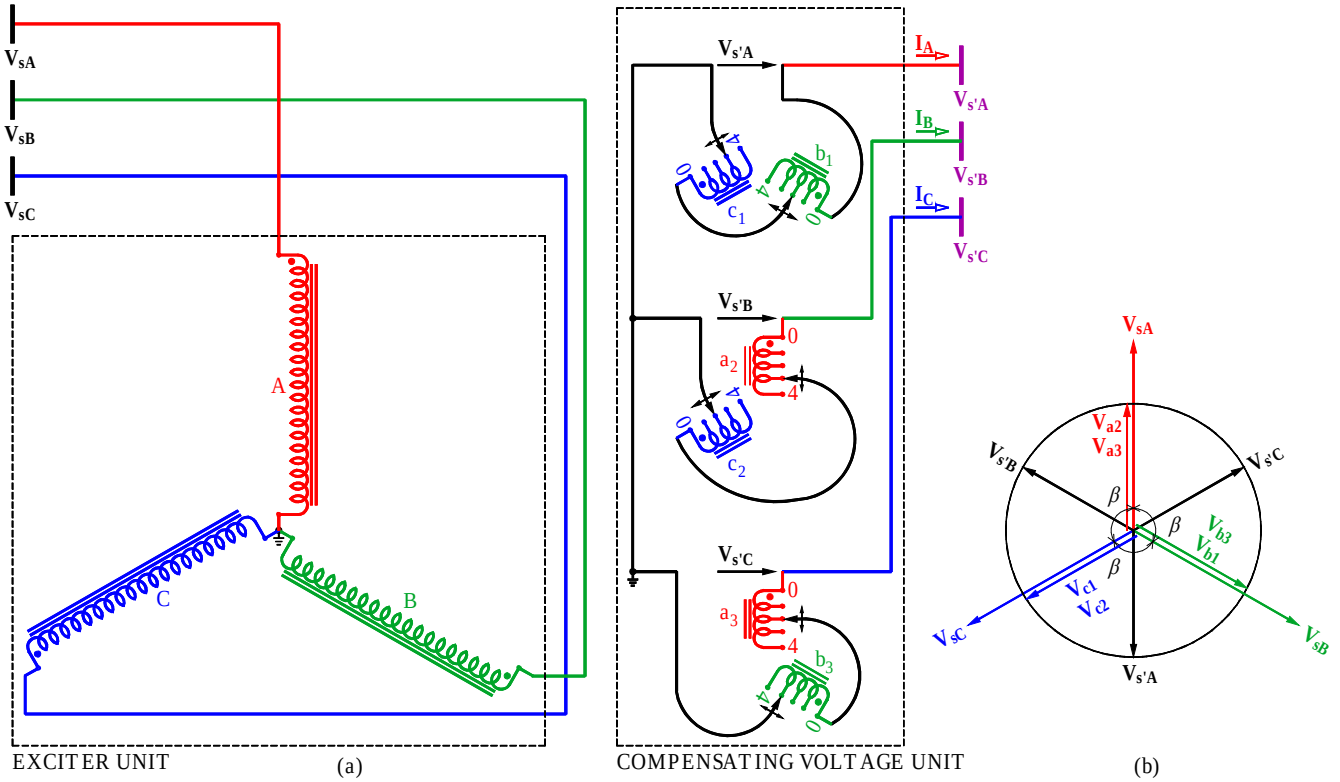


Figure 9-36. (a) ST with shunt-connected compensating voltage unit operating in the range of 120° through 240°. (b) Phasor diagram.

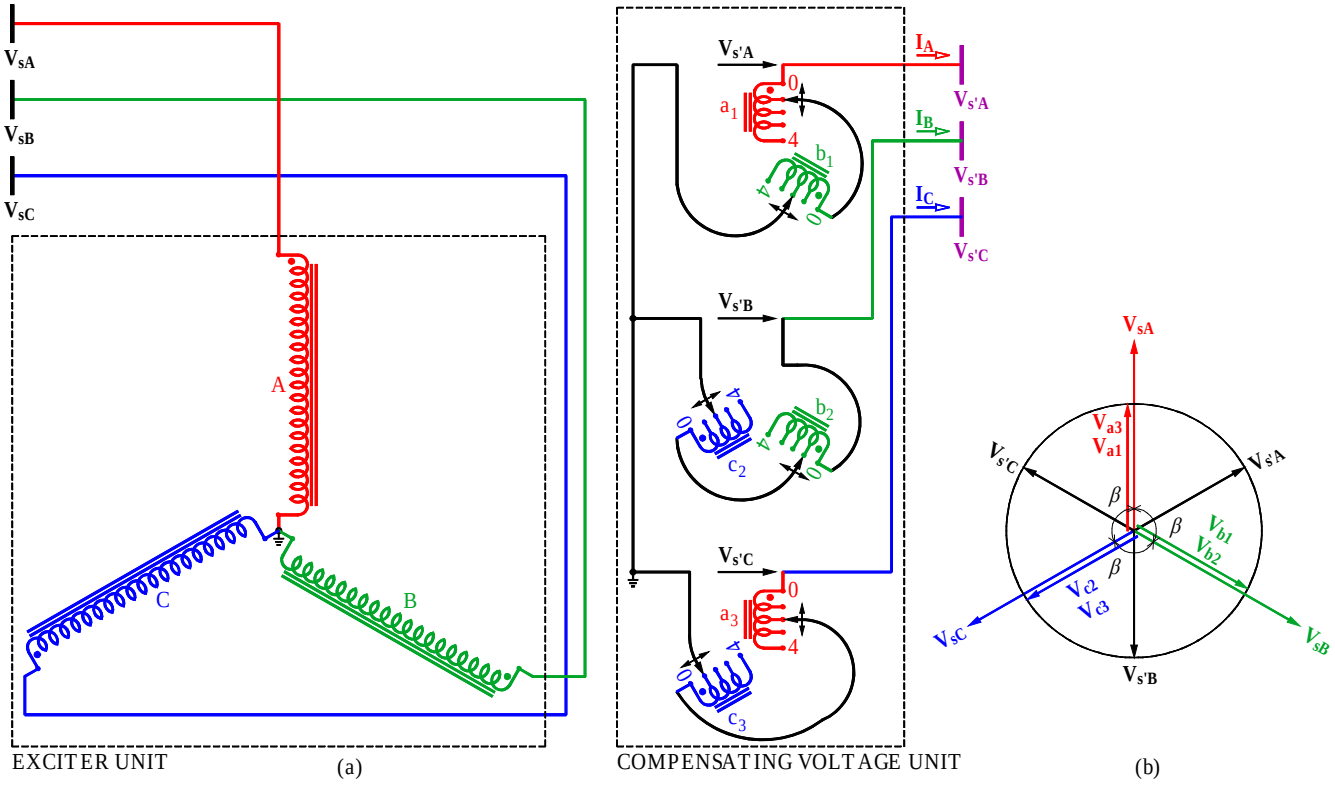


Figure 9-37. (a) ST with shunt-connected compensating voltage unit operating in the range of 240° through 360°. (b) Phasor diagram.

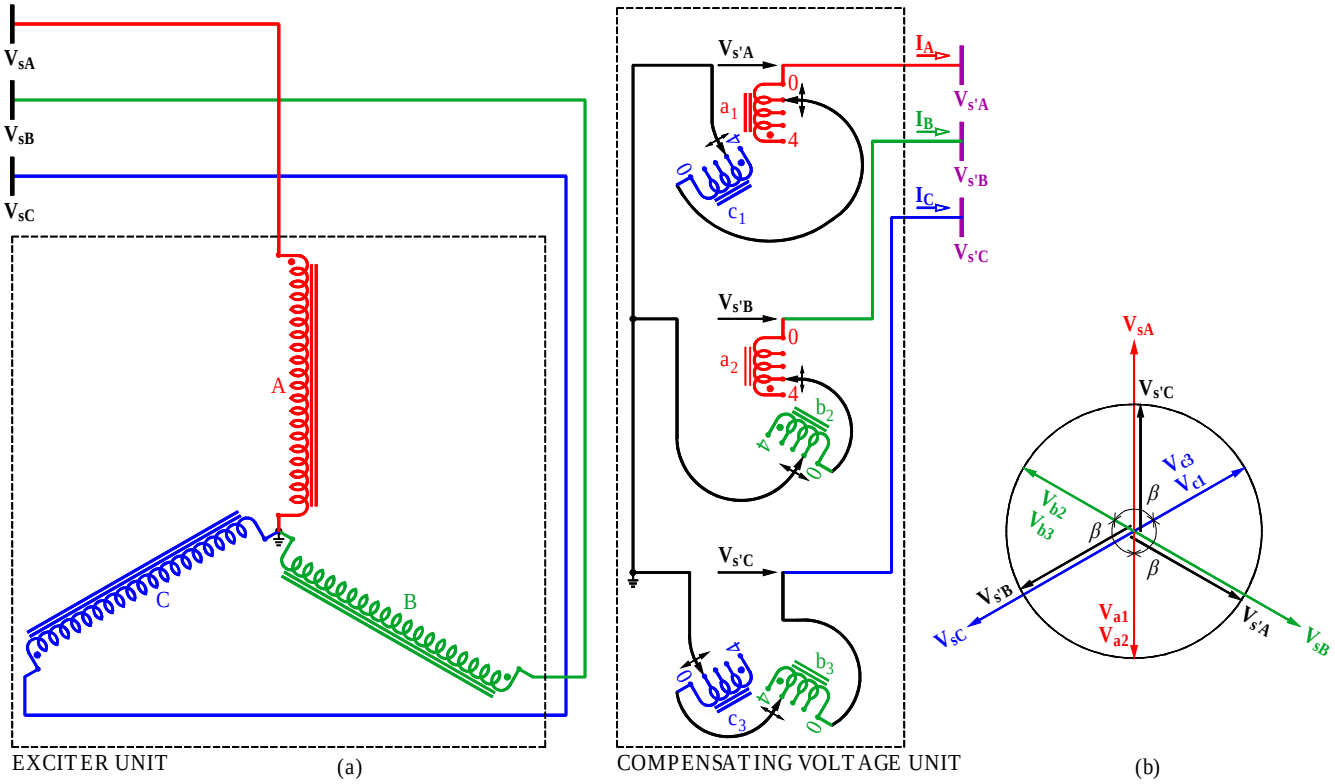


Figure 9-38. (a) ST with shunt-connected compensating voltage unit operating in the range of 180° through 300°. (b) Phasor diagram.

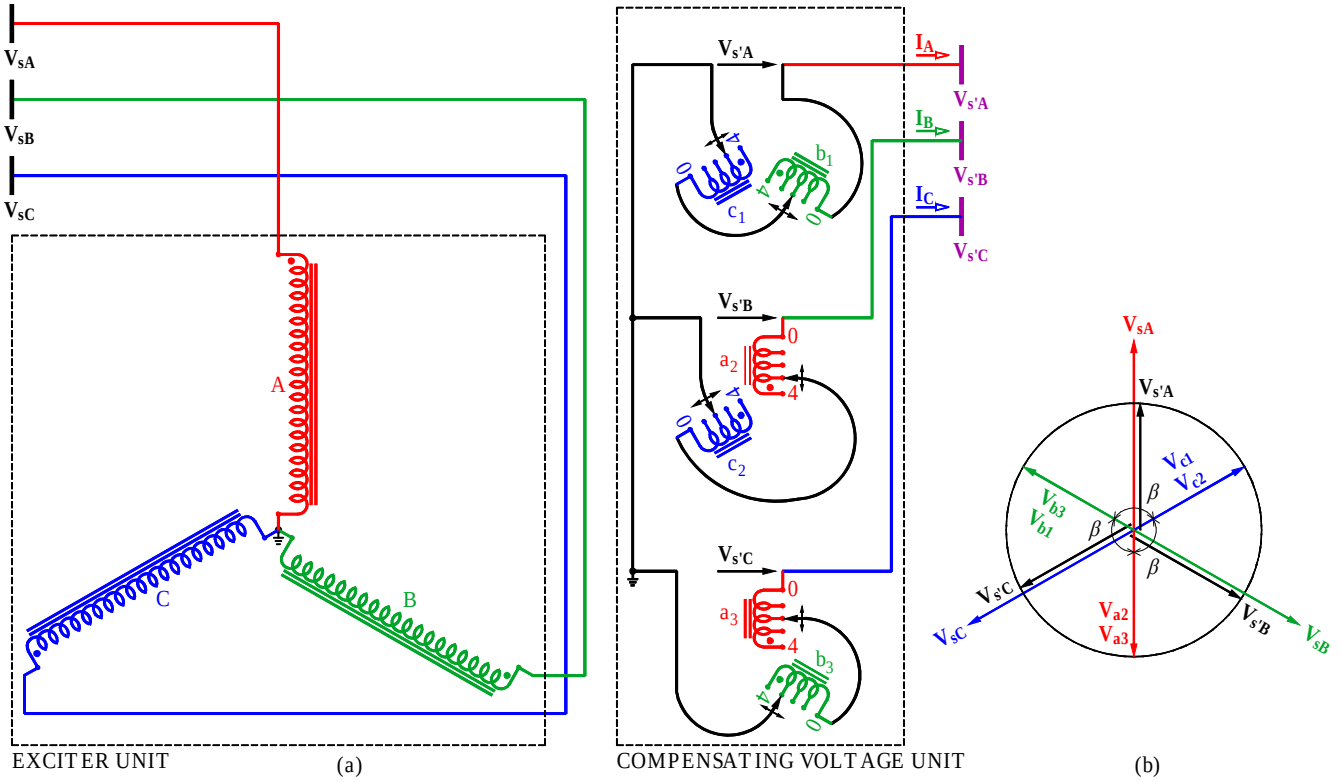


Figure 9-39. (a) ST with shunt-connected compensating voltage unit operating in the range of 300° through 60°. (b) Phasor diagram.

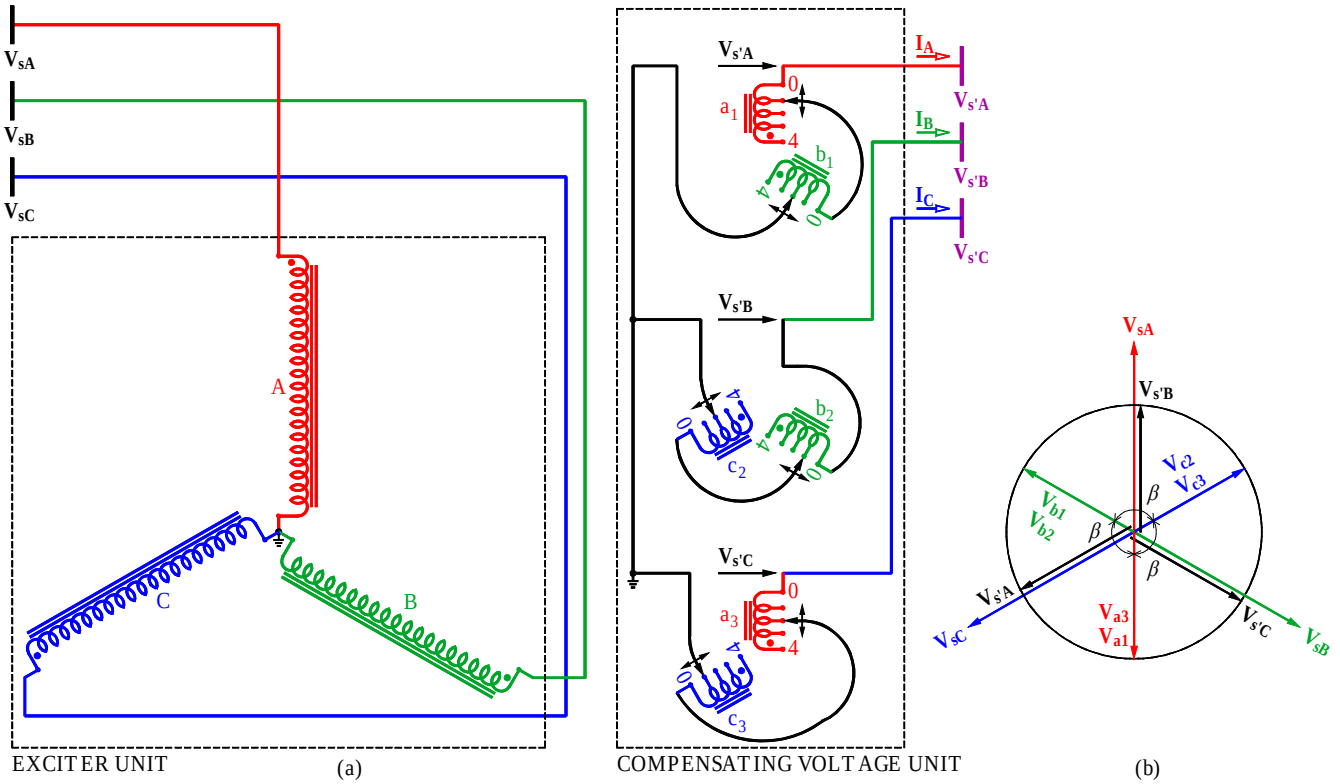


Figure 9-40. (a) ST with shunt-connected compensating voltage unit operating in the range of 60° through 180°. (b) Phasor diagram.

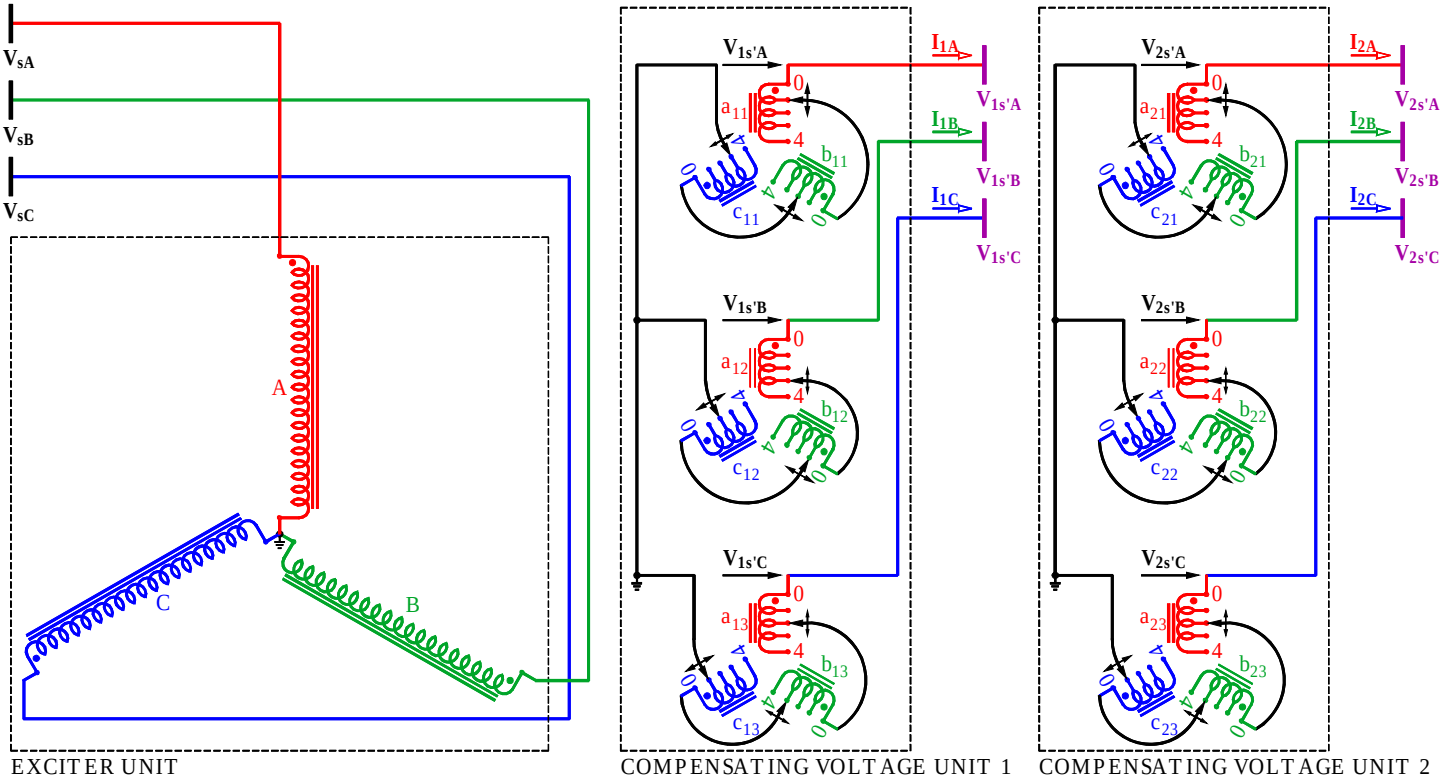


Figure 9-41. MST with shunt-connected compensating voltage units.

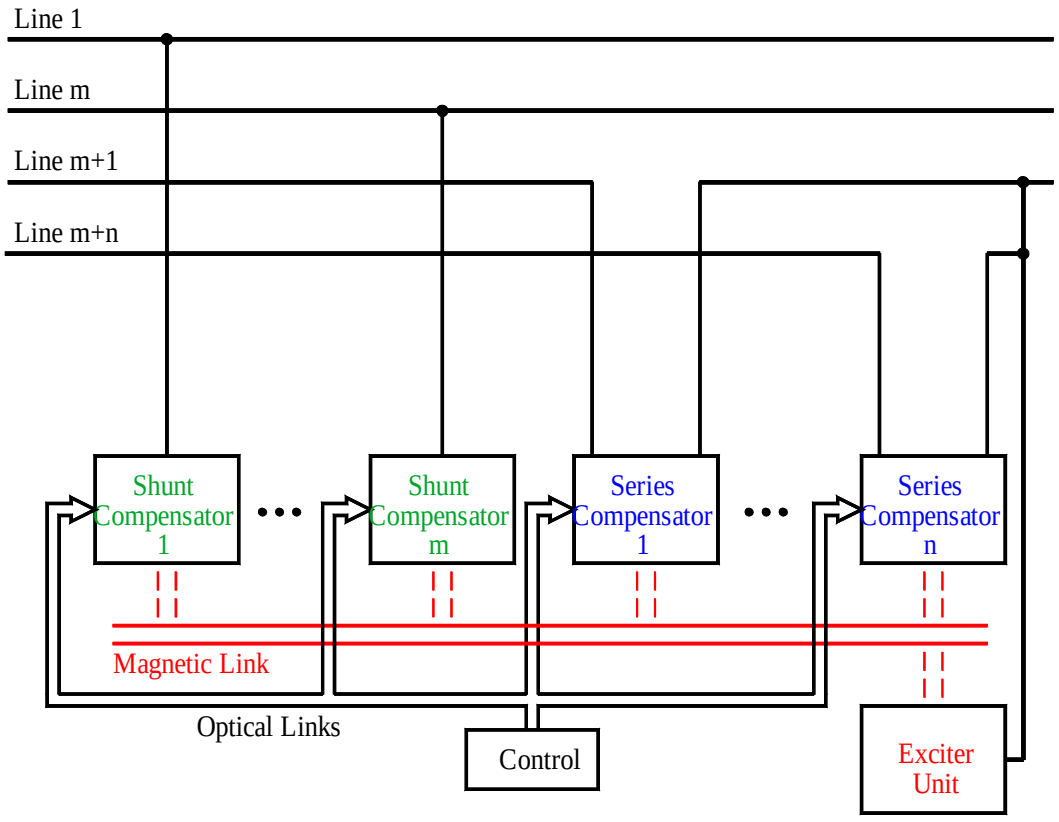


Figure 9-42. Generalized Sen transformer.

APPENDIX A

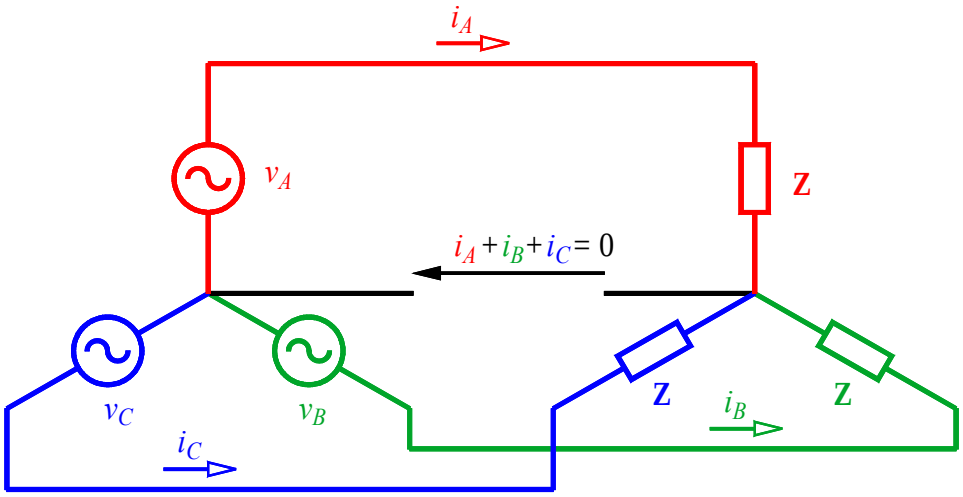


Figure A-1. Three-phase voltage source supplying currents to a three-phase load.

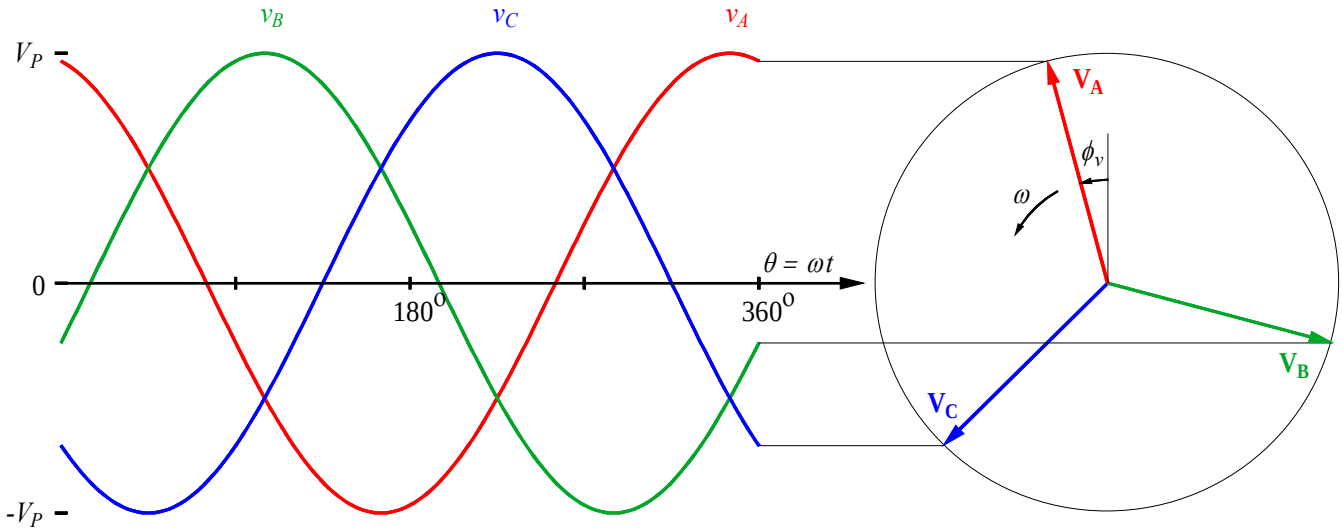


Figure A-2. Balanced three-phase voltages in a timing diagram and the corresponding phasor diagram at the end of the cycle.

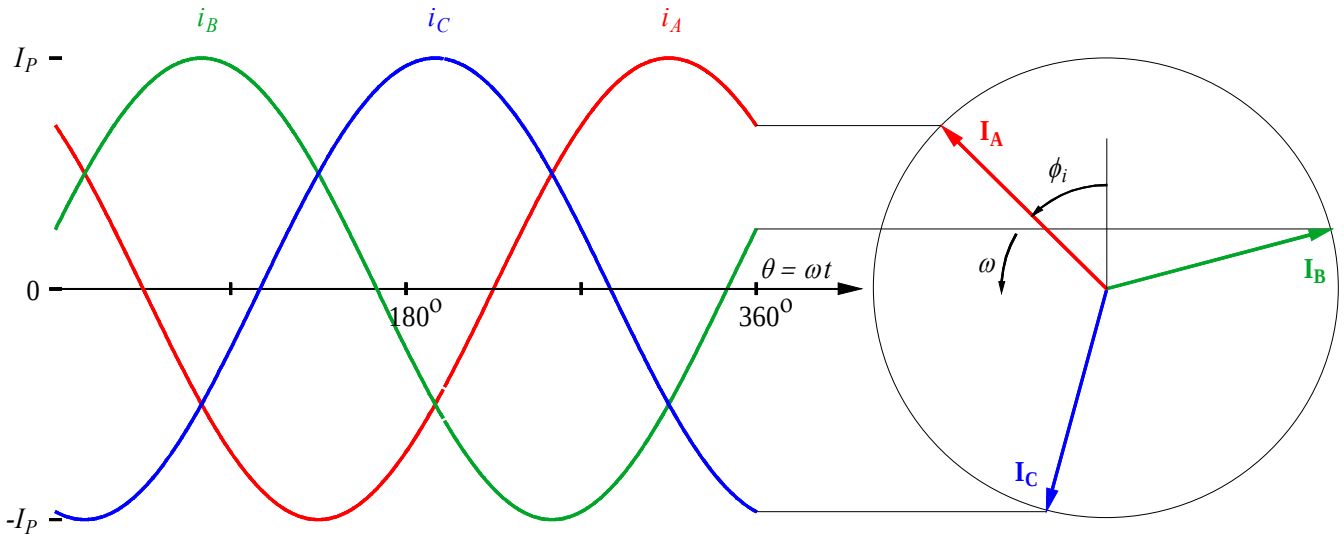


Figure A-3. Balanced three-phase currents in a timing diagram and the corresponding phasor diagram at the end of the cycle.

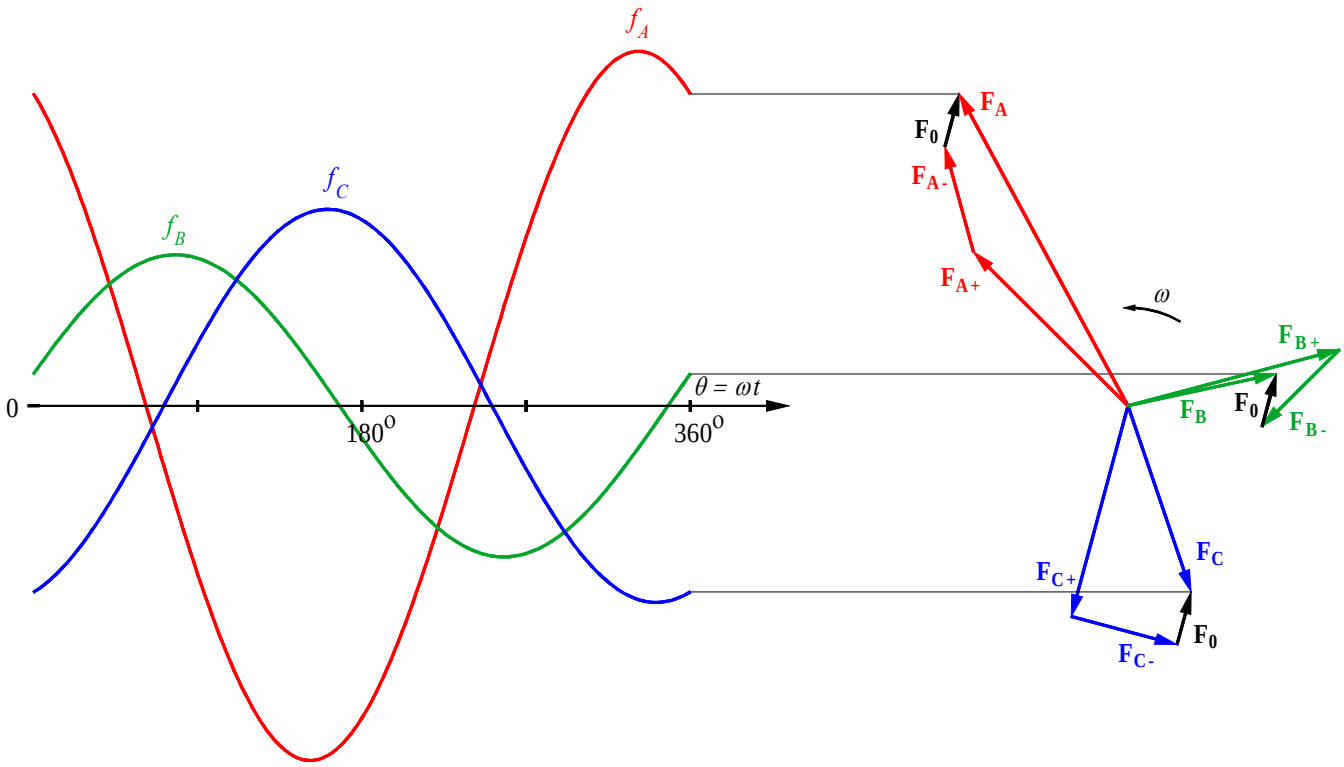


Figure A-4. Unbalanced three-phase variables in a timing diagram and the corresponding phasor diagram at the end of the cycle.

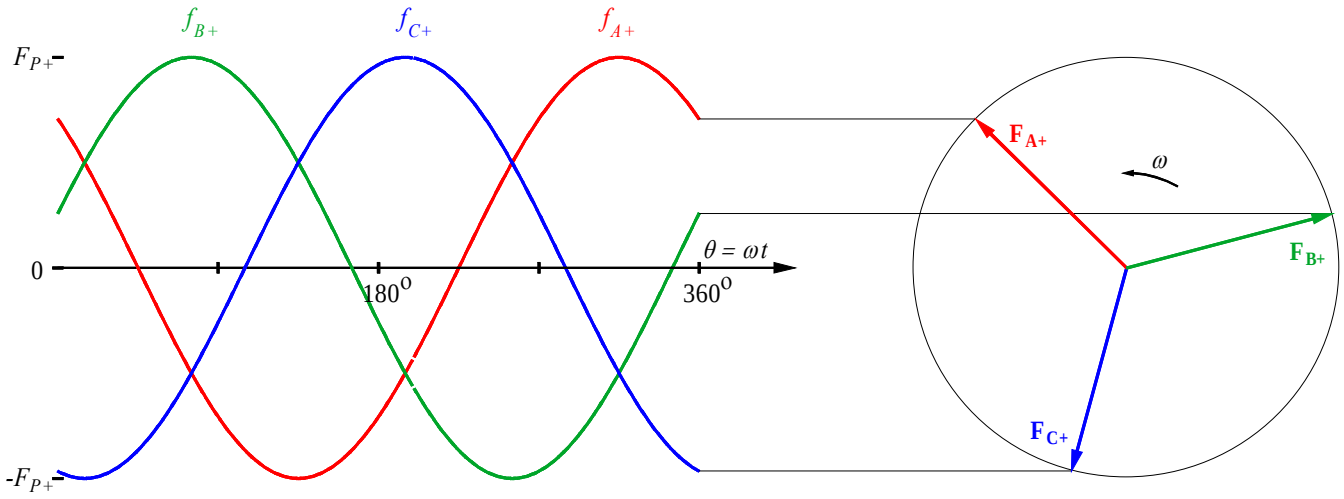
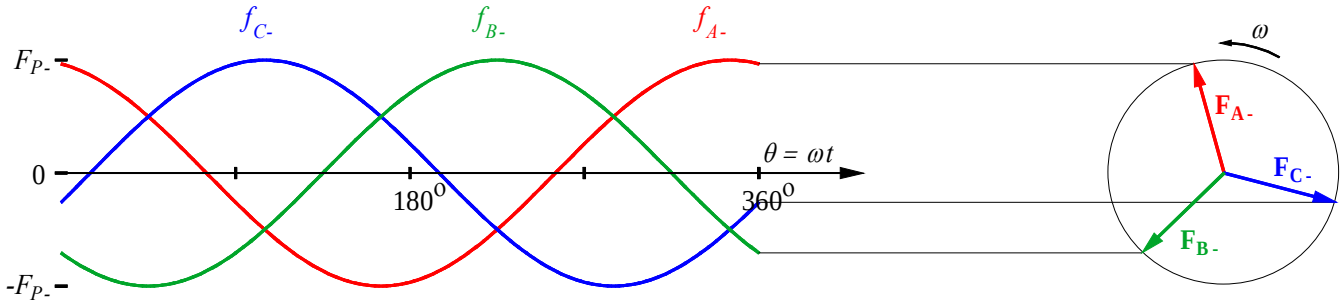


Figure A-5. Balanced three-phase positive sequence components in a timing diagram and the corresponding phasor diagram at the end of the cycle.



FigureA-6. Balanced three-phase negative sequence components in a timing diagram and the corresponding phasor diagram at the end of the cycle.

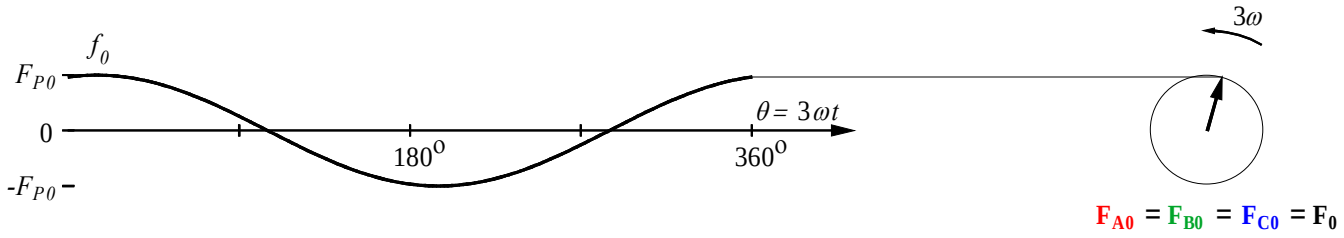


Figure A-7. Zero sequence component in a timing diagram and the corresponding phasor diagram at the end of the cycle.

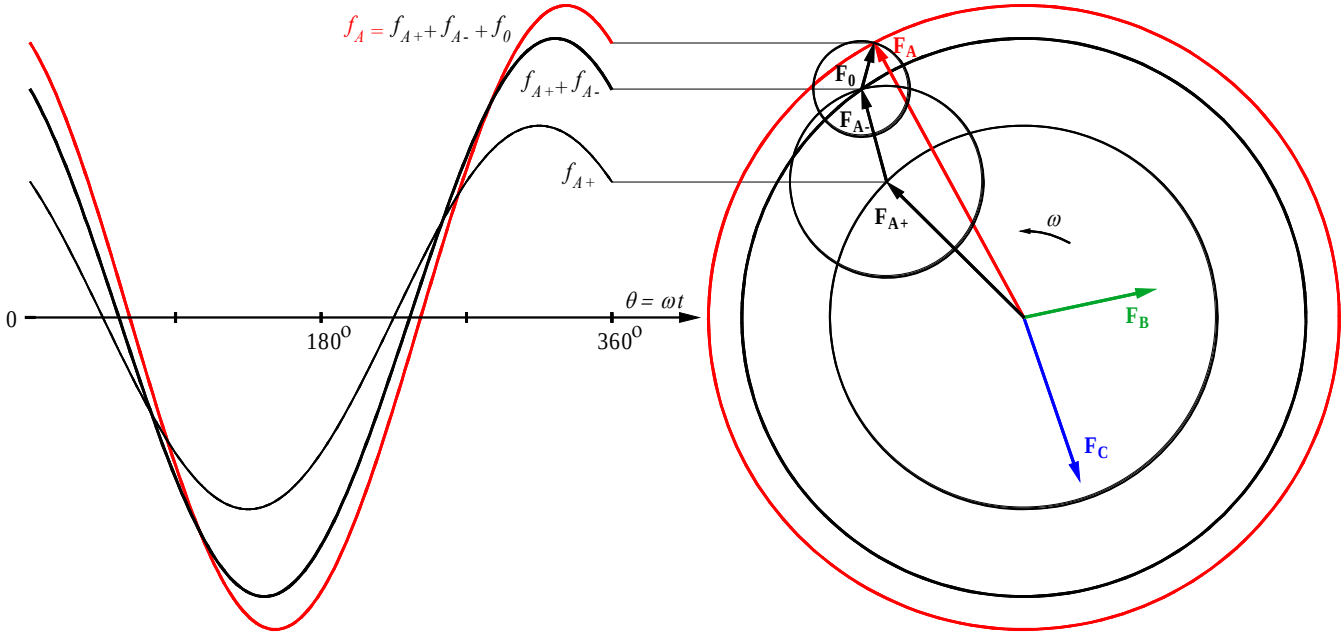


Figure A-8. A phase positive, negative, and zero sequence components in a timing diagram and the corresponding phasor diagram at the end of the cycle.

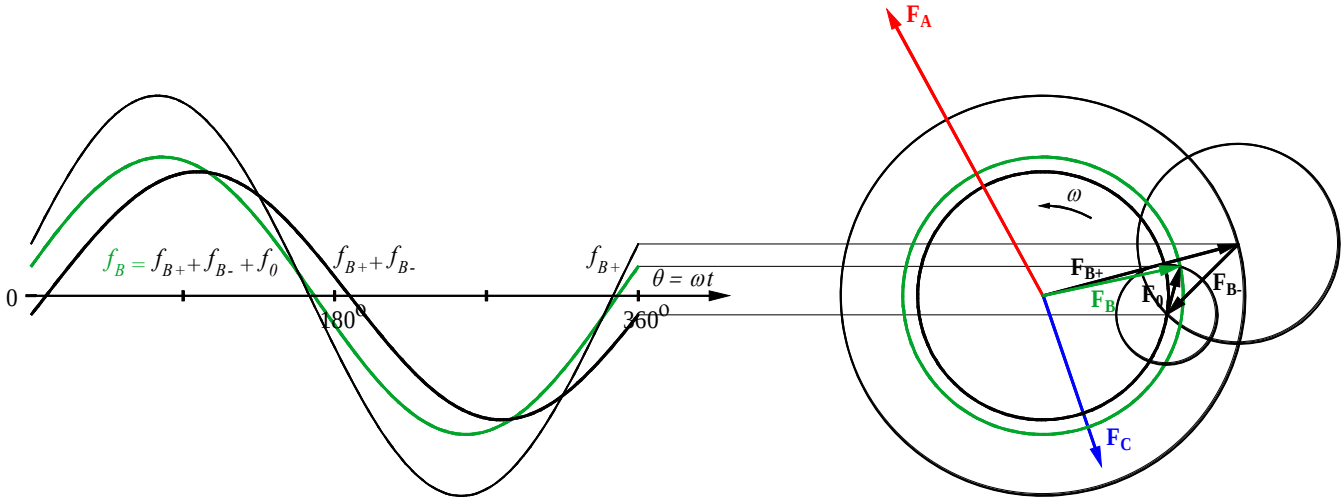


Figure A-9. B phase positive, negative, and zero sequence components in a timing diagram and the corresponding phasor diagram at the end of the cycle.

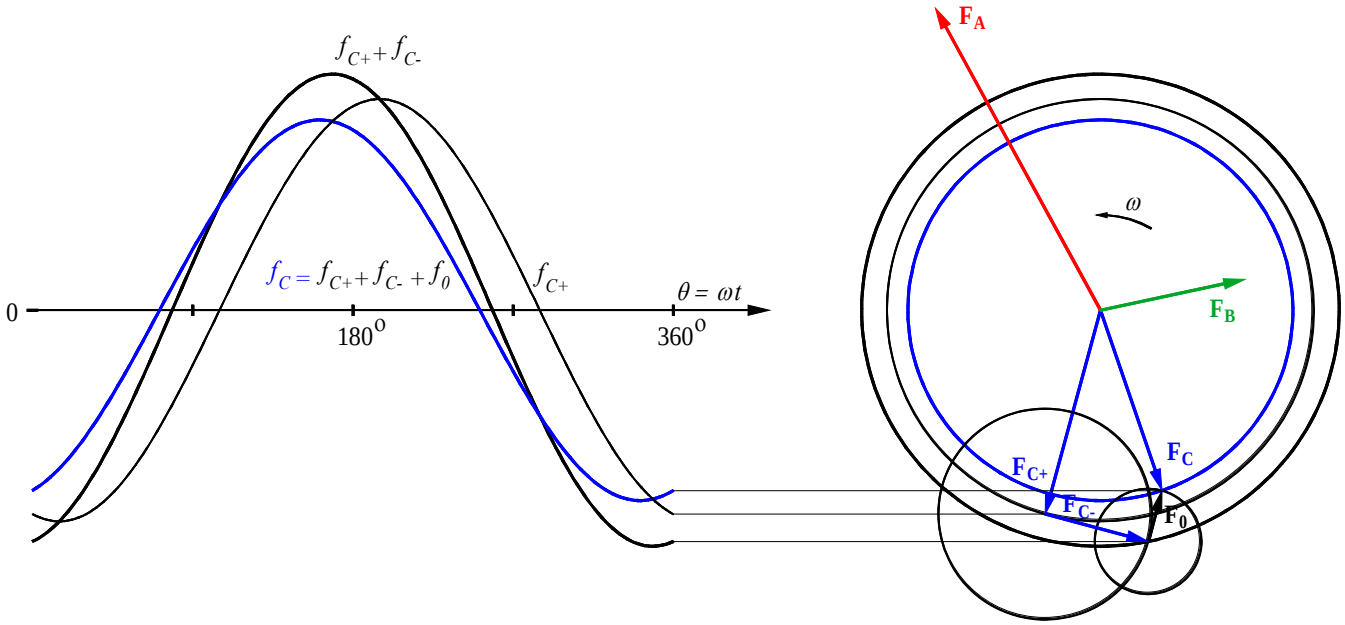


Figure A-10. C phase positive, negative, and zero sequence components in a timing diagram and the corresponding phasor diagram at the end of the cycle.

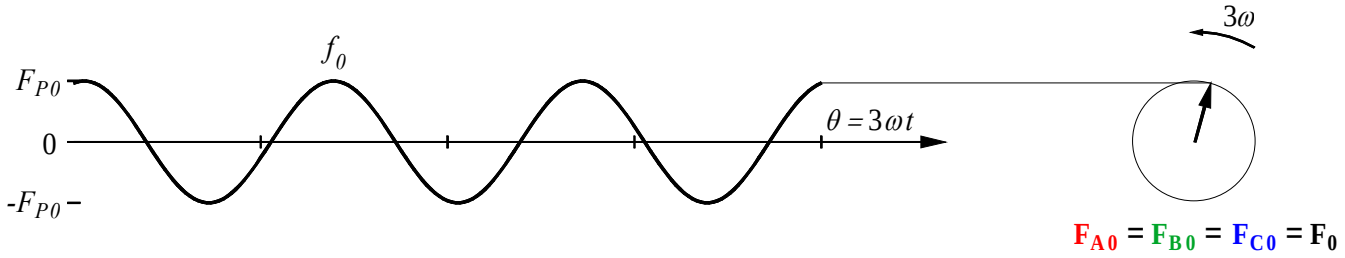


Figure A-11. Triple frequency zero sequence component in a timing diagram and the corresponding phasor diagram at the end of the cycle.

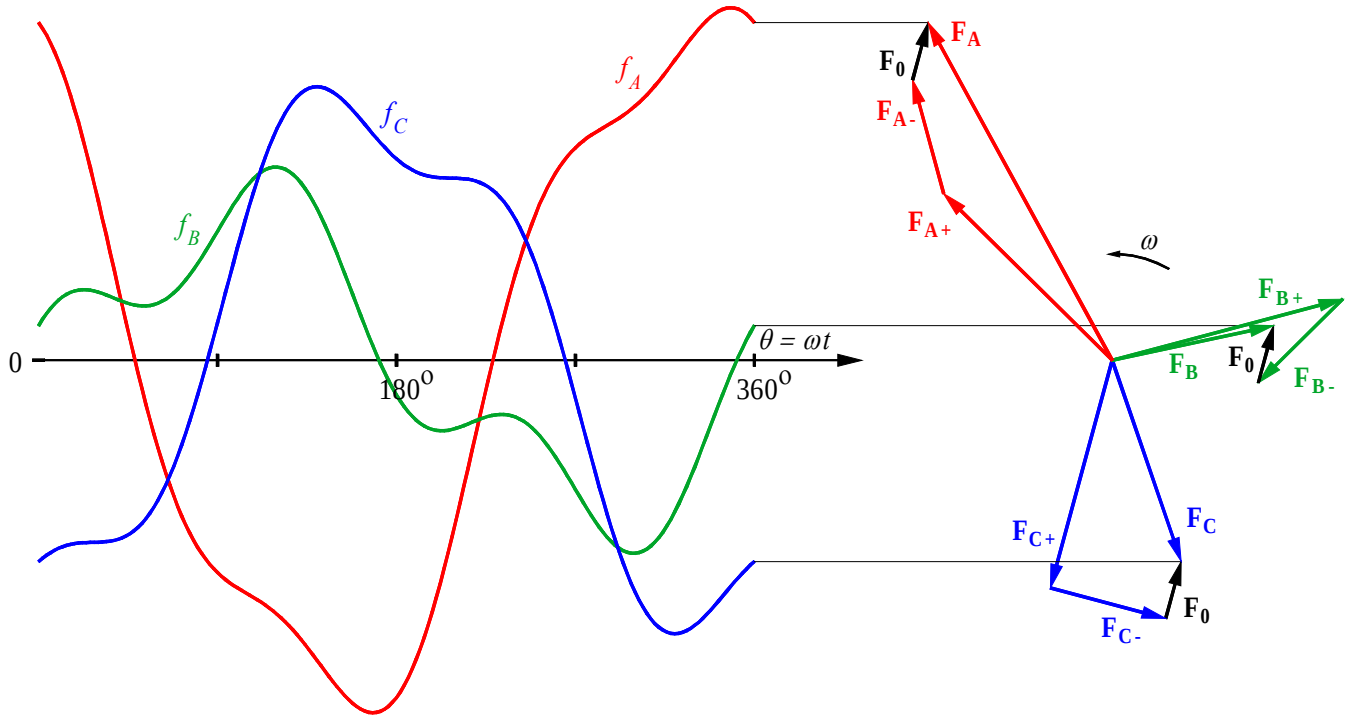


Figure A-12. Unbalanced three-phase variables in a timing diagram and the corresponding phasor diagram at the end of the cycle.

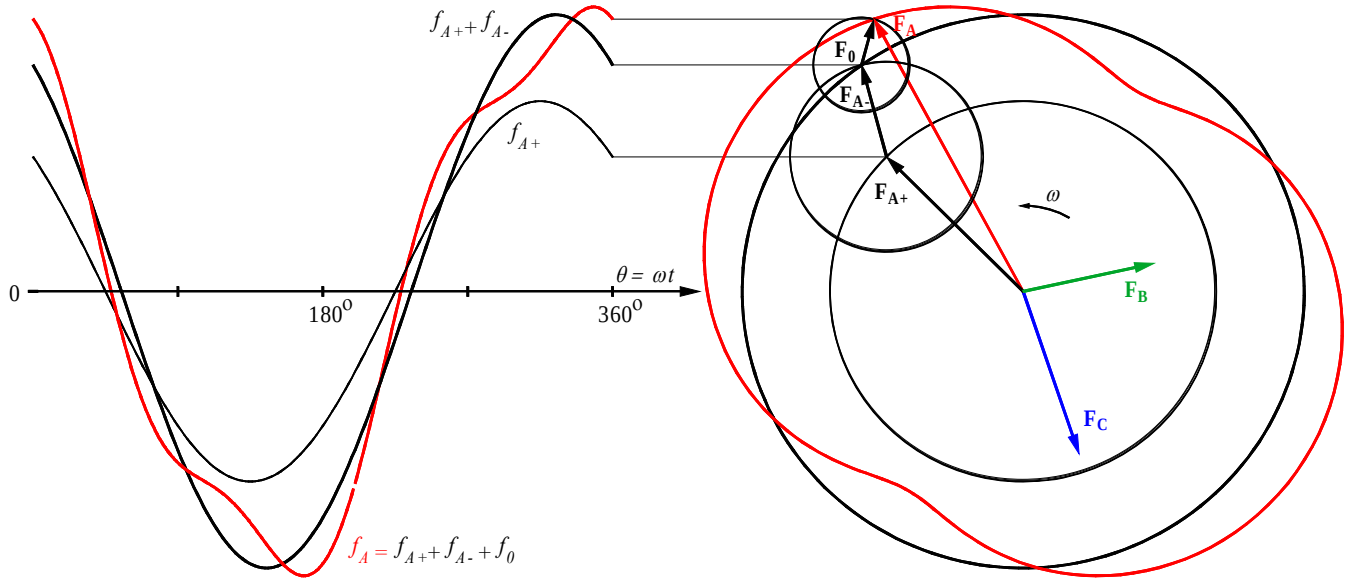


Figure A-13. A phase positive, negative, and zero sequence components in a timing diagram and the corresponding phasor diagram at the end of the cycle.

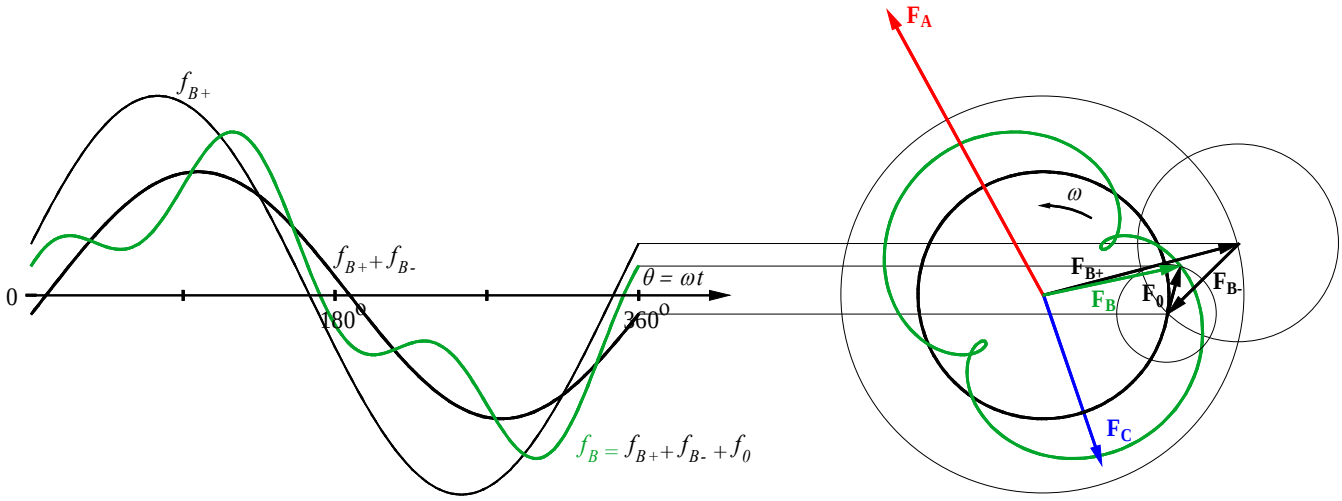


Figure A-14. B phase positive, negative, and zero sequence components in a timing diagram and the corresponding phasor diagram at the end of the cycle.

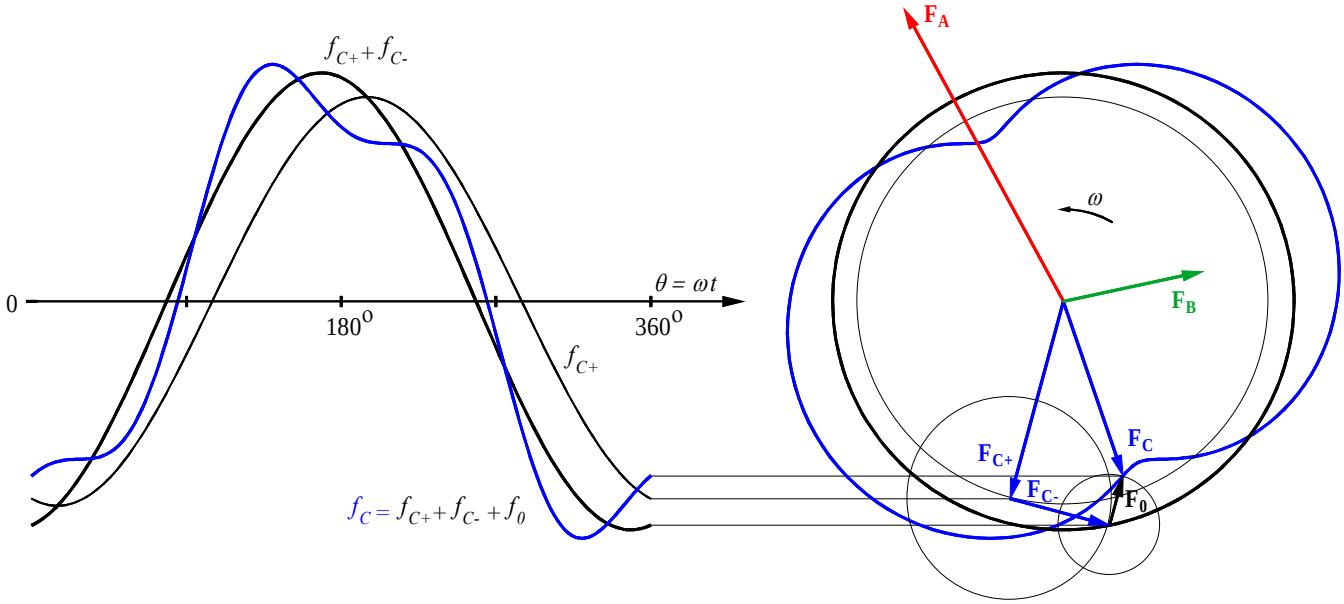


Figure A-15. C phase positive, negative, and zero sequence components in a timing diagram and the corresponding phasor diagram at the end of the cycle.

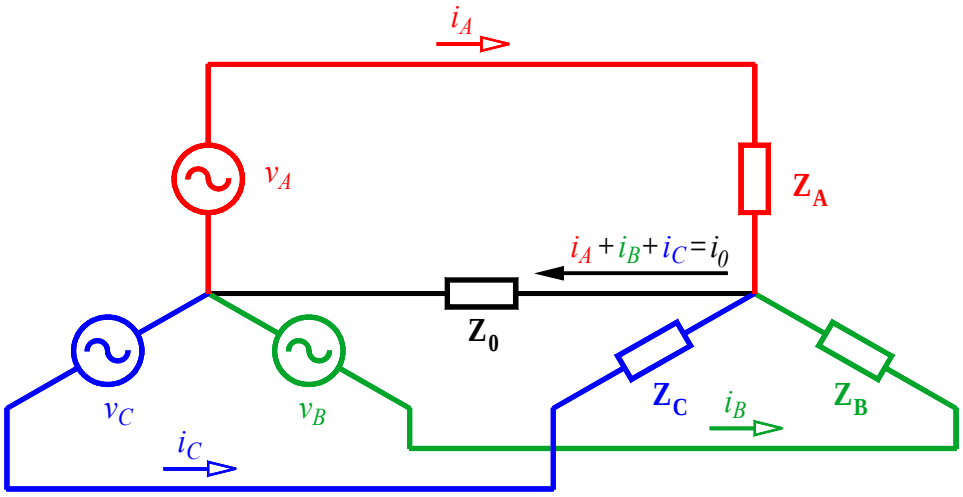


Figure A-16. Three-phase voltage source supplying three-phase unbalanced load.

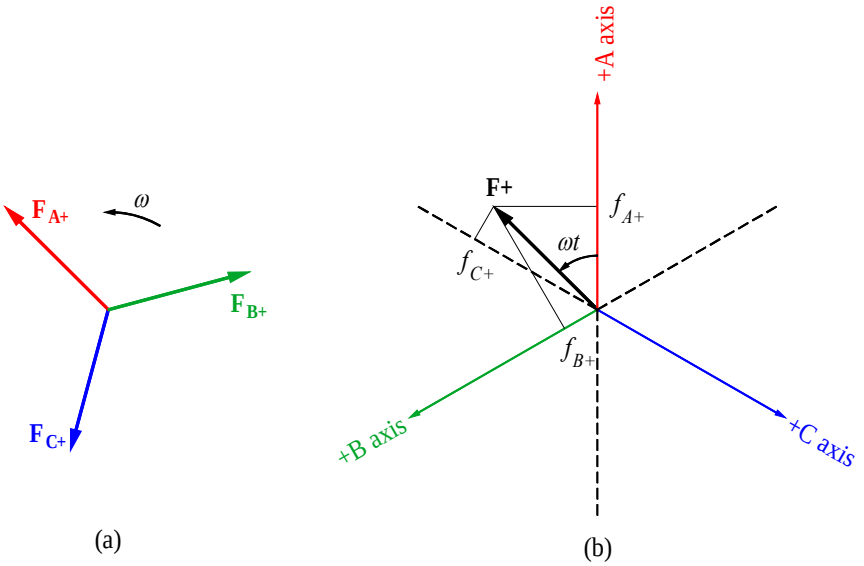


Figure A-17. Representation of three-phase positive sequence variables in (a) a phasor diagram and (b) a vector diagram.

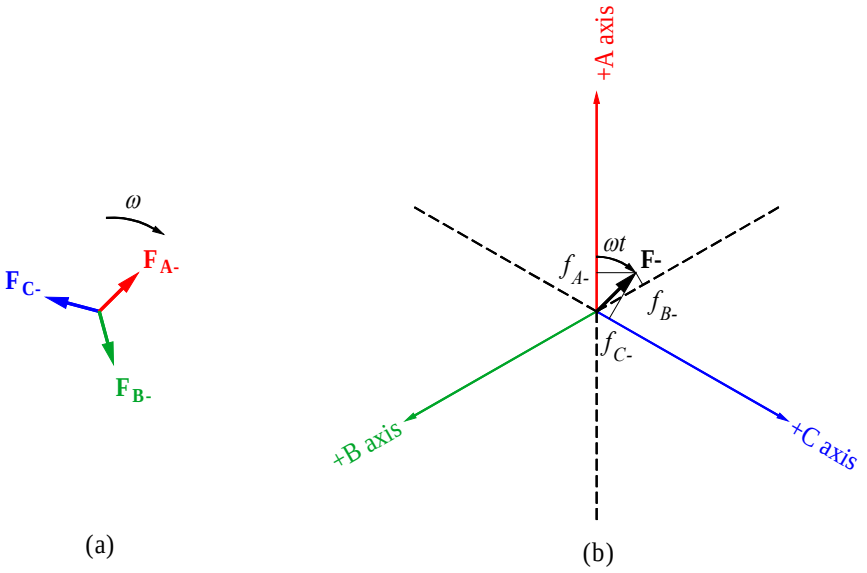


Figure A-18. Representation of three-phase negative sequence variables in (a) a phasor diagram and (b) a vector diagram.

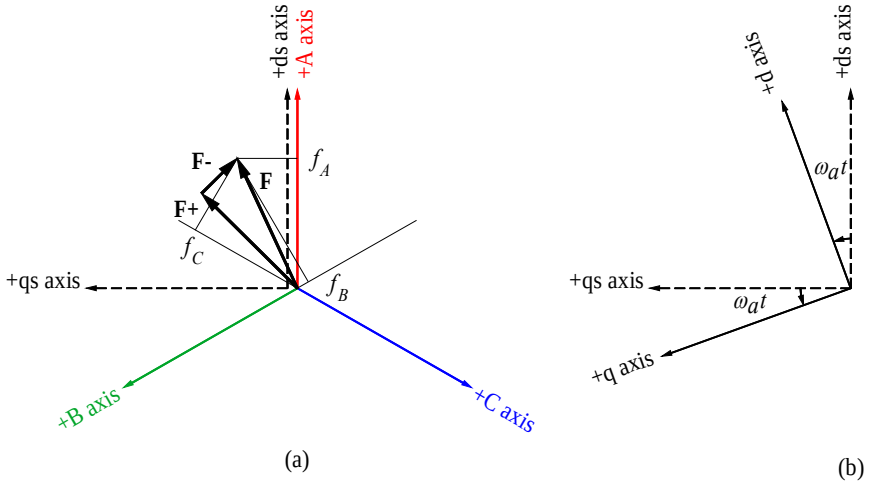


Figure A-19. Conversion of A, B, and C stationary variables into (a) d-q stationary and (b) d-q rotating frames.

APPENDIX B

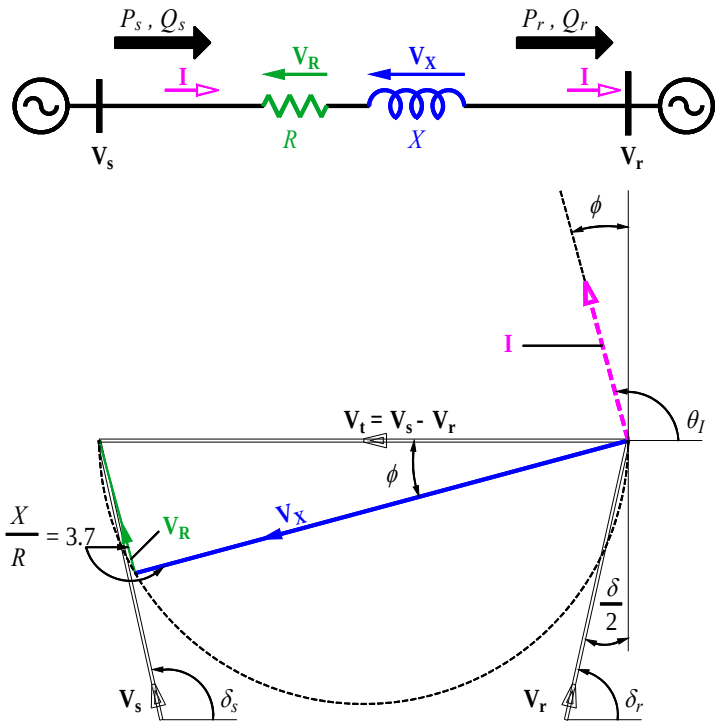


Figure B-1. Single line power transmission system and its phasor diagram.

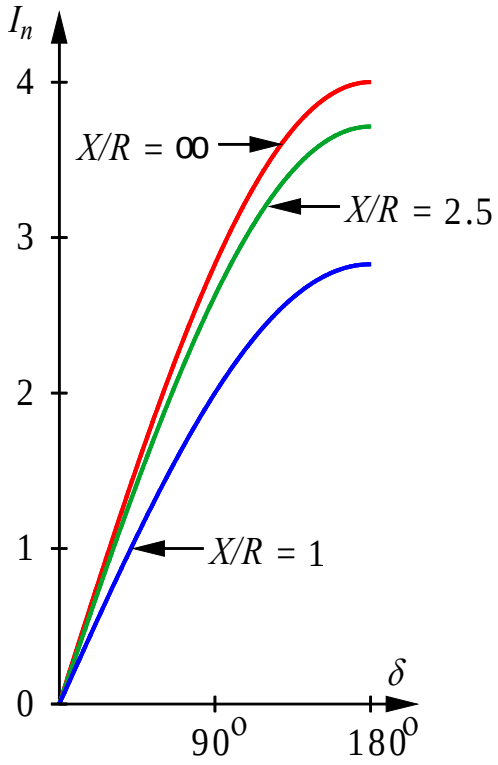


Figure B-2. (a) Natural current (I_n) as a function of power angle δ (*i.e.*, δ_s–δ_r).

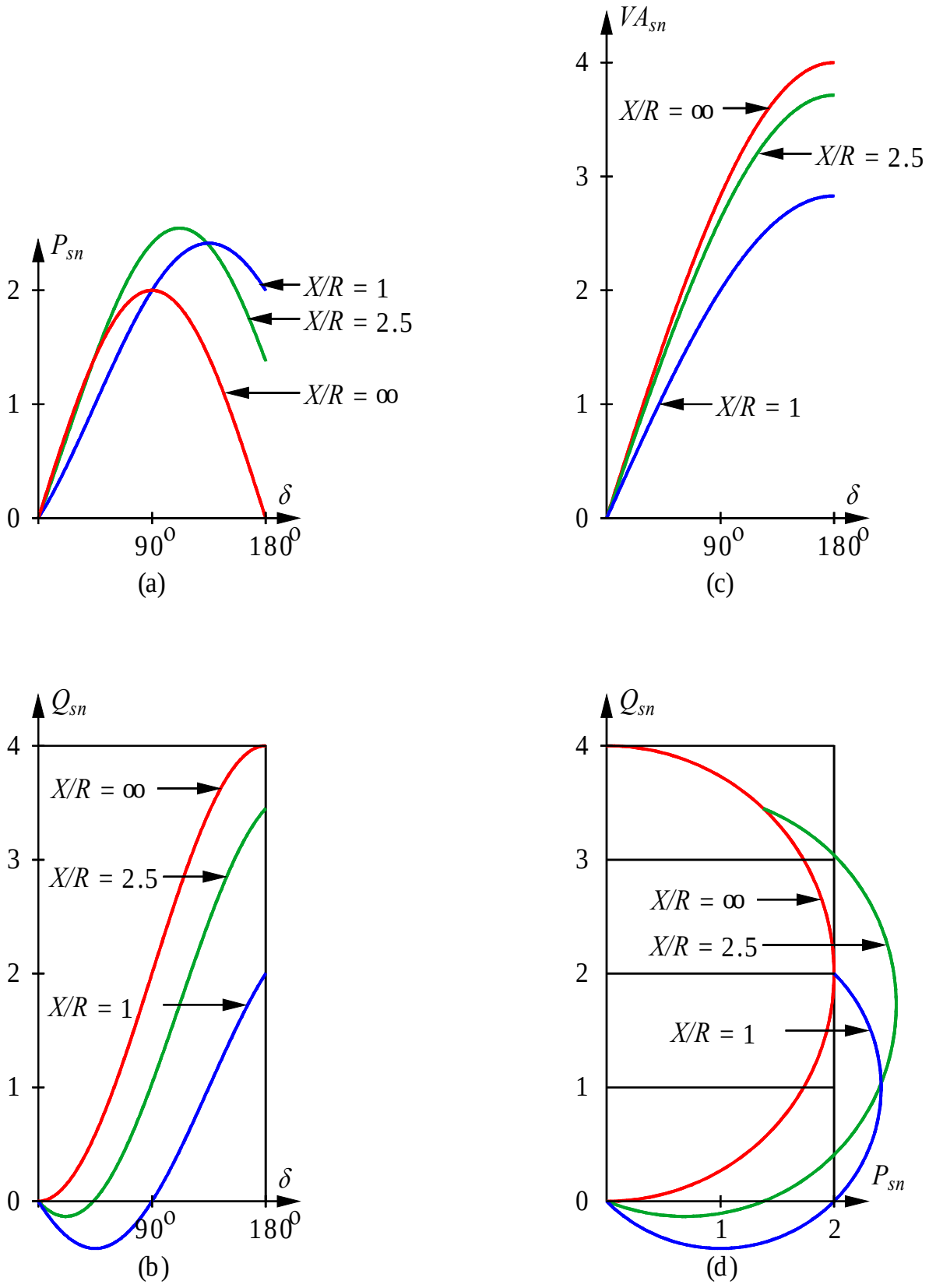


Figure B-3. (a) Natural active power (P_{sn}), (b) natural reactive power (Q_{sn}), and (c) natural apparent power (VA_{sn}) as a function of power angle (δ), and (d) Q_{sn} vs P_{sn} at the sending end of the transmission line.

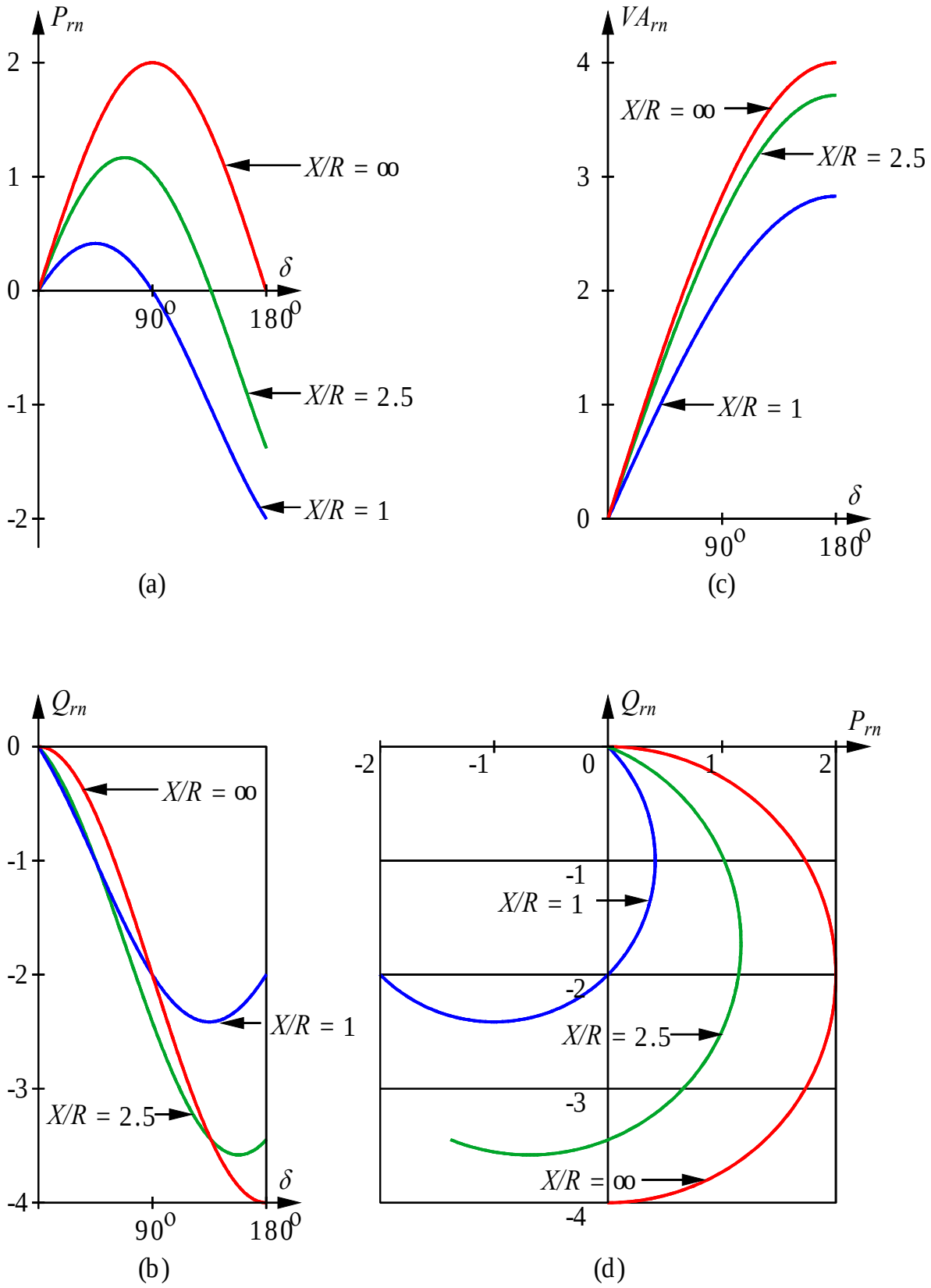


Figure B-4. (a) Natural active power (P_{rn}), (b) natural reactive power (Q_{rn}), and (c) natural apparent power (VA_{rn}) as a function of power angle (δ), and (d) Q_{rn} vs P_{rn} at the receiving end of the transmission line.

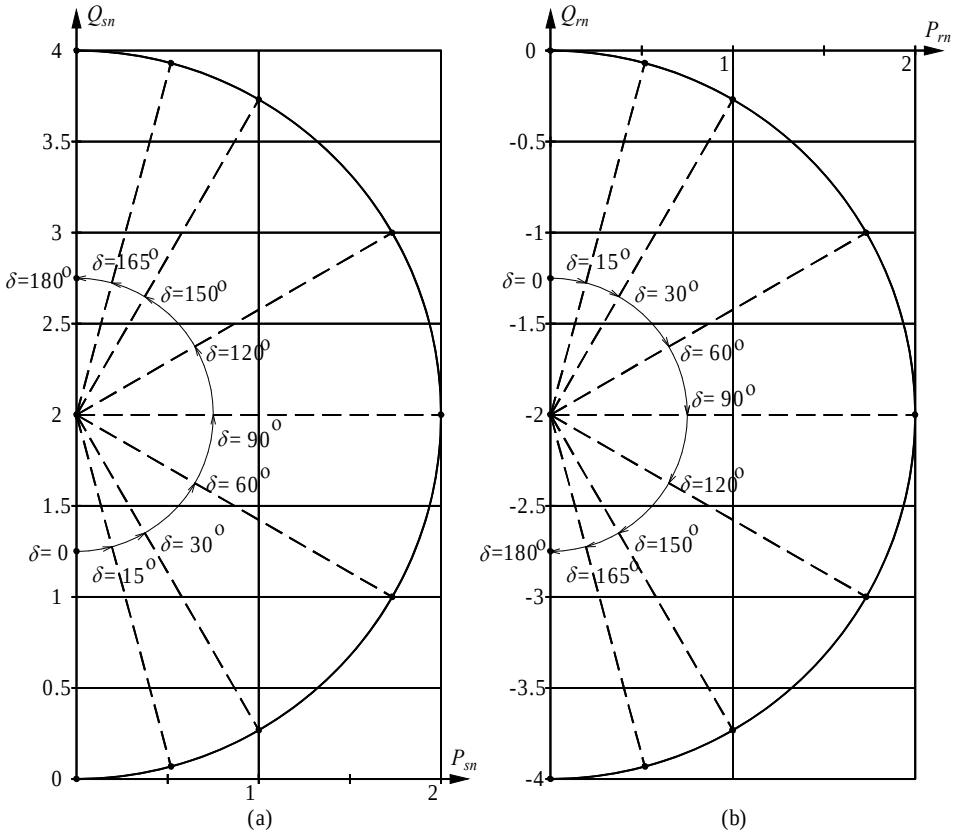


Figure B-5. (a) Q_{sn} vs P_{sn} at the sending end and (b) Q_{rn} vs P_{rn} at the receiving end of the transmission line for the range of power angle δ (*i.e.*, δ_s–δ_r) from 0 to 180° when $V_s = V_r = 1$, and $X = 0.5$, and $R = 0$ (X/R=∞).

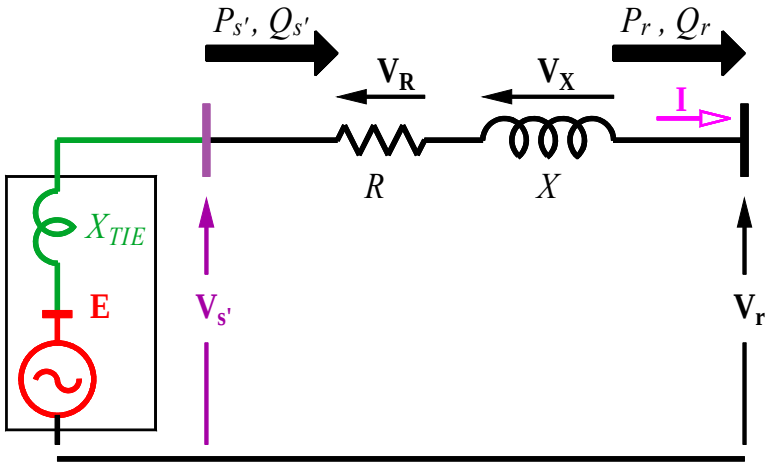


Figure B-6. Modified sending-end voltage ($\mathbf{V_{s'}}$) with a shunt-connected compensating voltage.

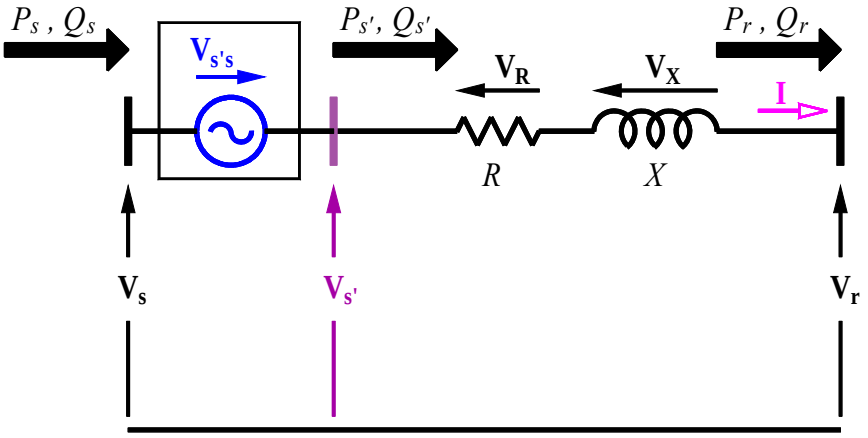


Figure B-7. Modified sending-end voltage ($\mathbf{V_{s'}}$) with a series-connected compensating voltage.