Broadband Circuits for Optical Fiber Communication

Slides for a short course based on the book:

E. Sackinger, "Broadband Circuits for Optical Fiber Communication," John Wiley, 2005.

ISBN: 0−471−71233−7

Overview

- **Introduction**
- **Optical Fiber**
- **Photodetectors**
- **Receiver Fundamentals**
- **Transimpedance Amplifiers (TIA)**
- **Main Amplifiers:**

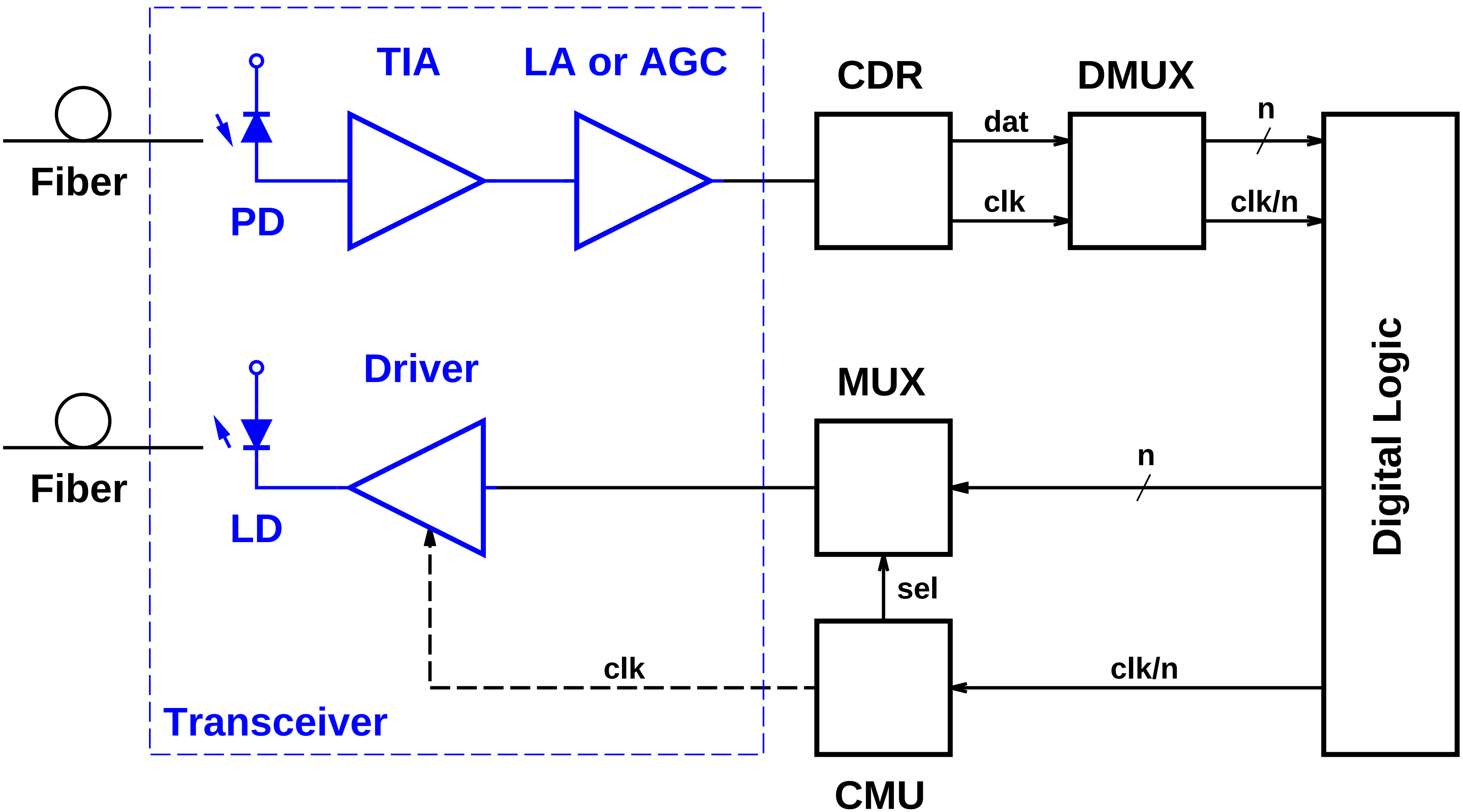
  Limiting Amplifiers (LA)

  Automatic Gain Control (AGC) Amplifiers
- **Lasers and Modulators**
- **Drivers:**

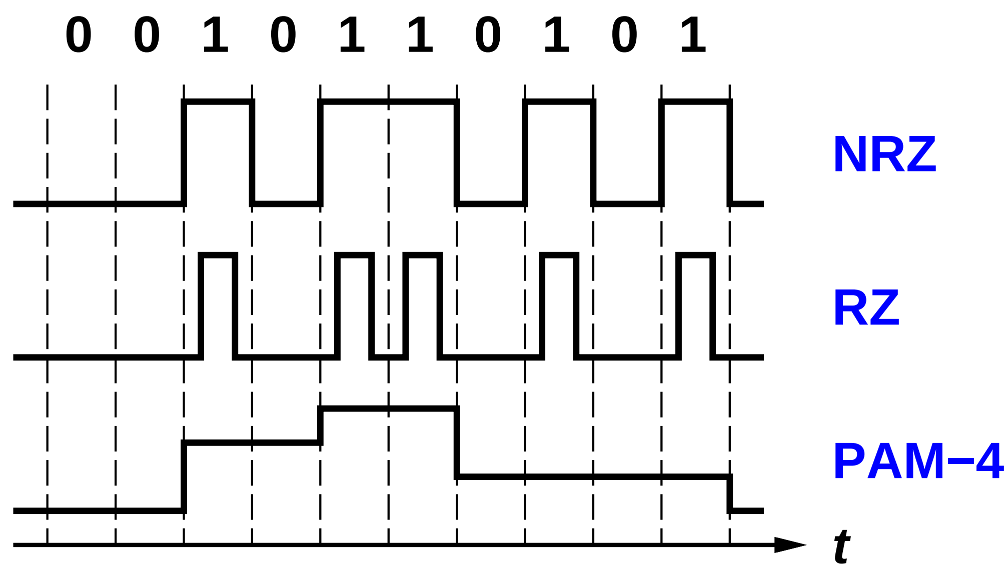
  Laser Drivers

  Modulator Drivers

Optical Transceiver



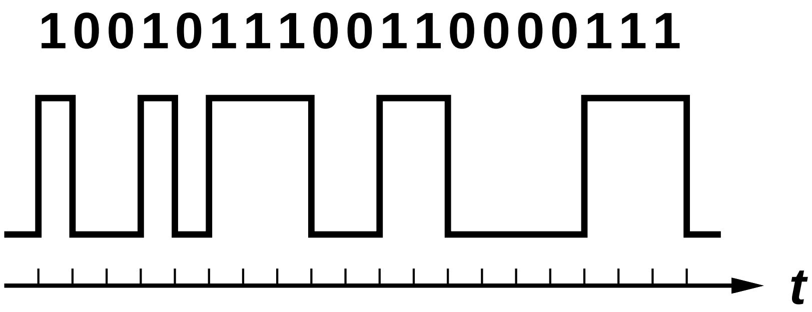
Modulation Schemes



- **NRZ: Most commonly used**
- **RZ: Less SNR, but more bandwidth required**
  Used in high−speed long−distance transmission
- **PAM, QAM, AM−VSB, etc.**
  Less bandwidth, but more SNR required
  Used in CATV/HFC systems, etc.

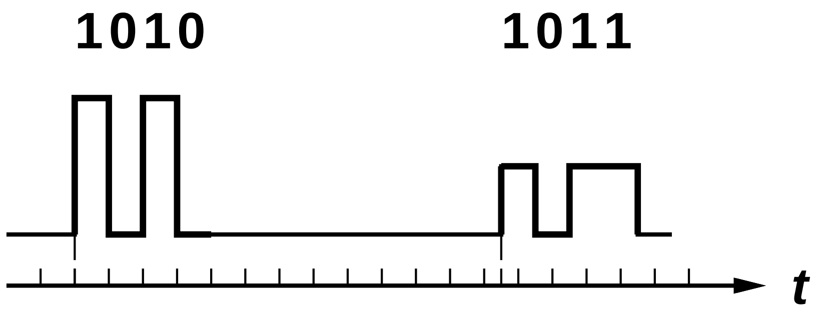
Continuous Mode vs. Burst Mode

Continuous mode:



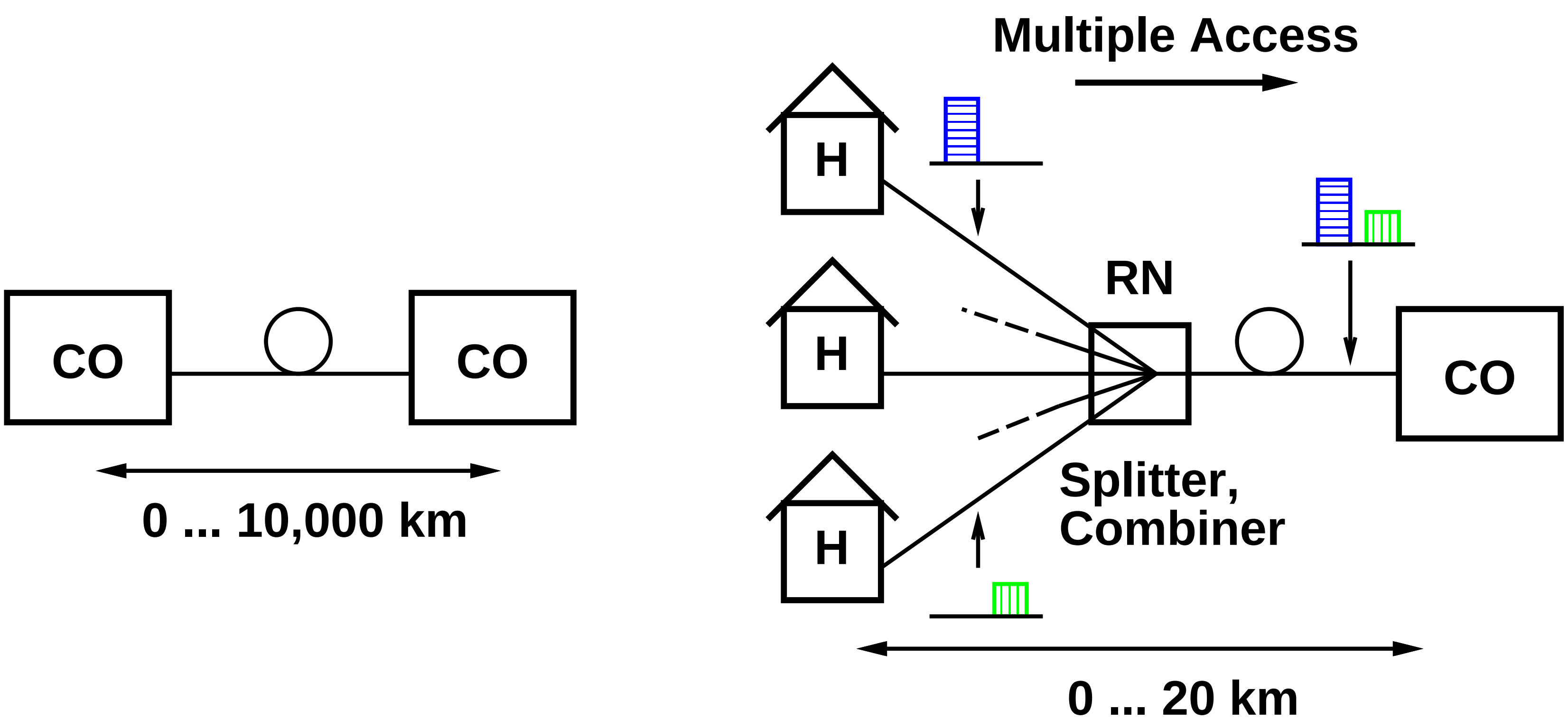
- DC balanced
  - Scrambling
  - 8B10B encoding
- Synchronous
- Used in
  SONET, SDH, GbE, 10−GbE, ...

Burst mode:



- Not DC balanced
  - Bursty
  - Large amplitude variations
- Asynchronous bursts
- Used in
  BPON, EPON, ...

Backbone vs. Access Networks



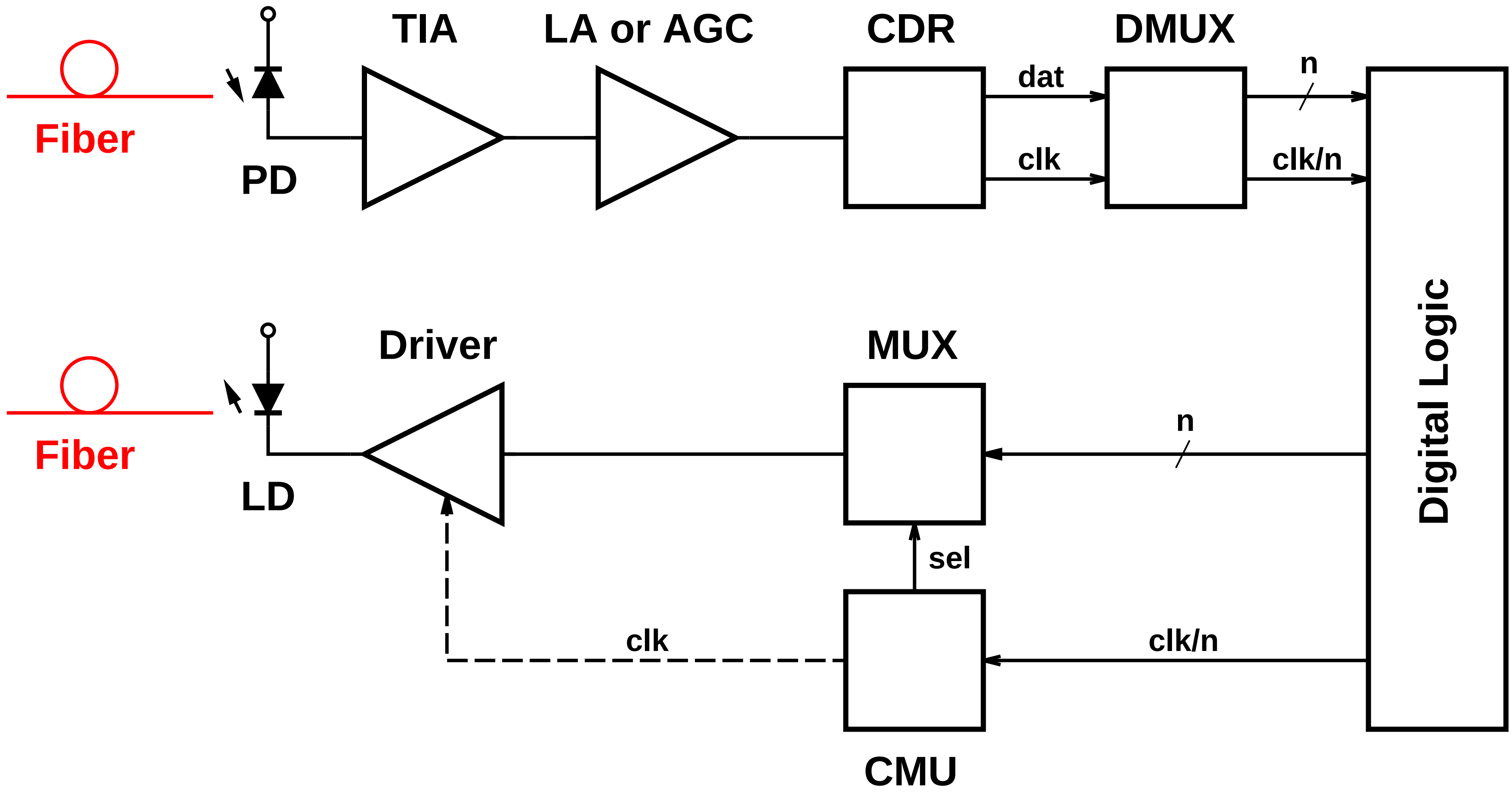
Backbone, Metro, LAN:

- Short to ultra−long reach
- High−speed (2.5 ... 40 Gb/s)
- Point−to−point
  → Continuous mode

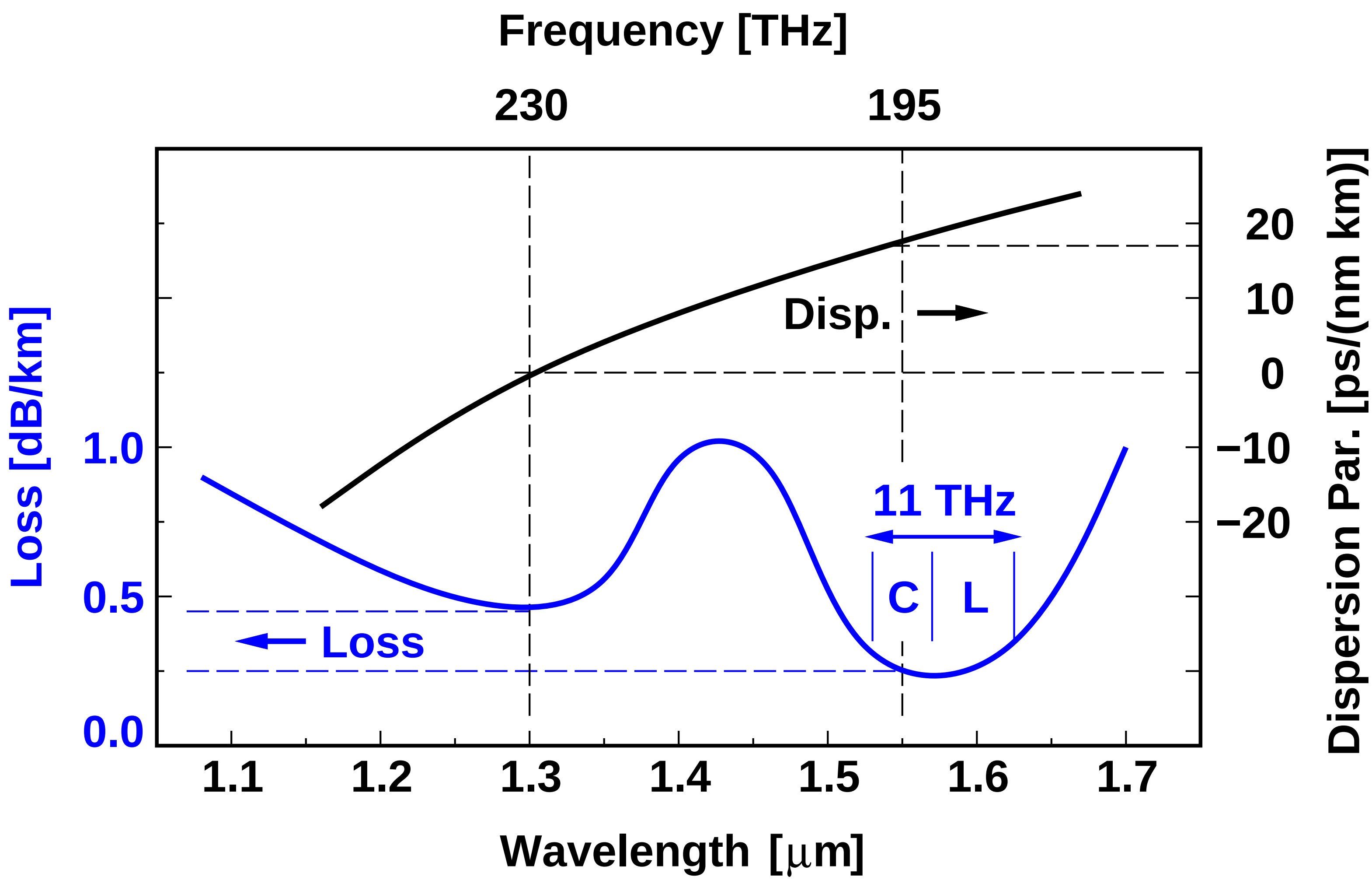
Access (PON):

- Short distance
- Low−speed (50 Mb/s ... 1.25 Gb/s)
- Point−to−multipoint
  → Burst mode (upstream)
  → TDMA protocol

Optical Fiber



Loss & Bandwidth



- **Extremely low loss**

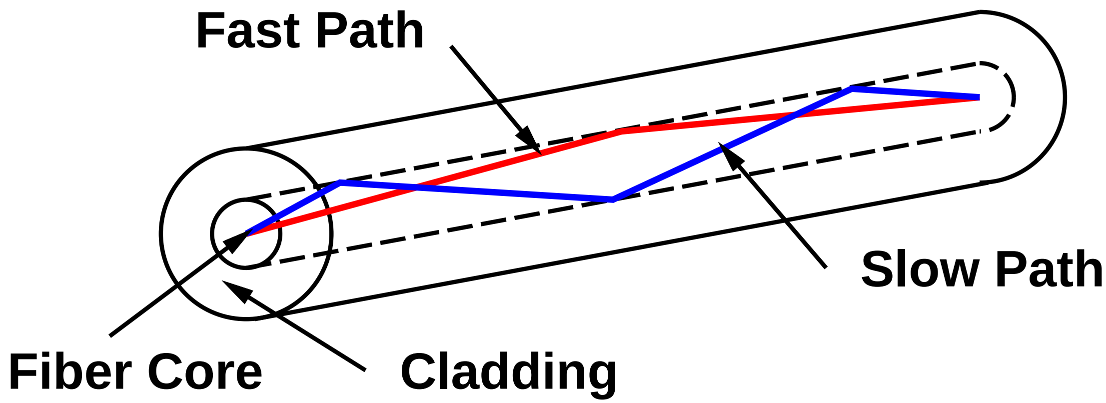
  1000x ... 2000x better (in dBs!) than coax cable at 10 GHz!

- **Extremely high bandwidth**

  >10 THz in 1.55 um band (C + L) alone!

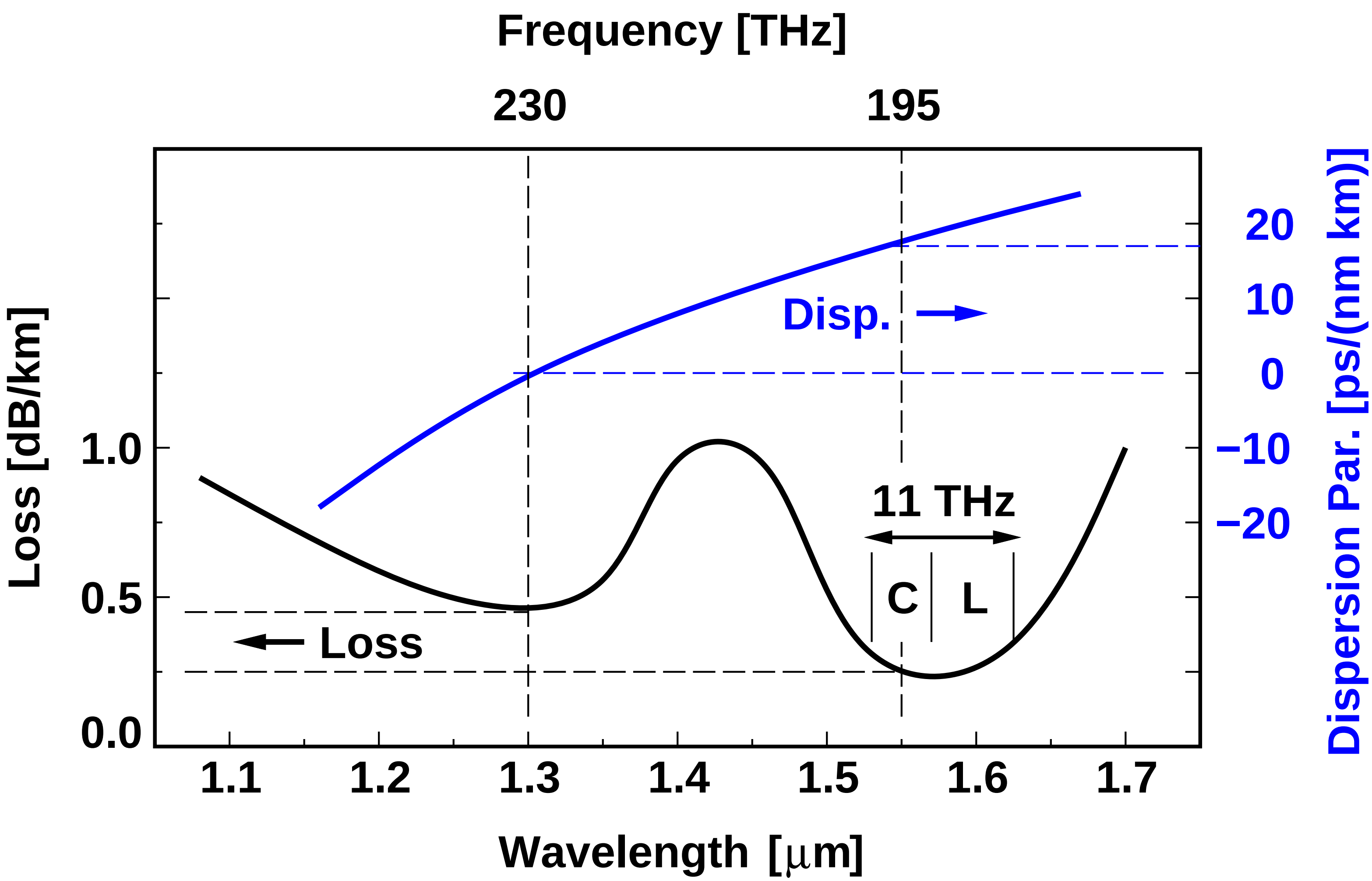
E. Säckinger, "Broadband Circuits for Optical Fiber Communication," John Wiley & Sons, 2005.

Modal Dispersion



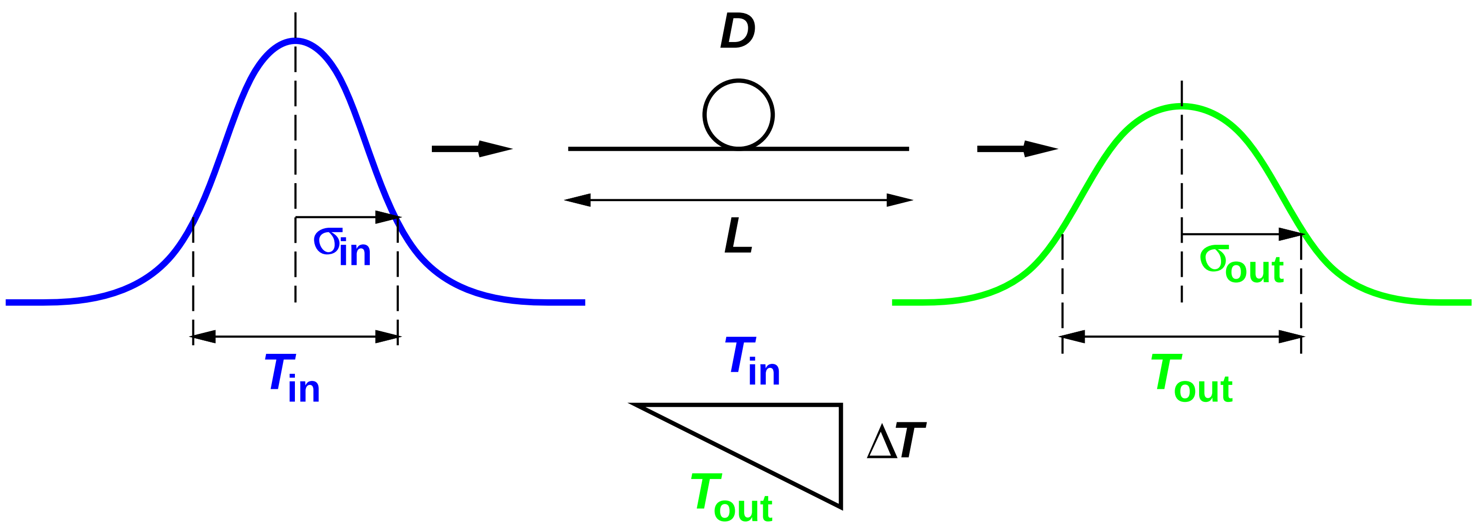
- Multimode fiber (MMF):
  - Fiber core = 50 ...100 um
  - Easy alignment, cheaper systems (laser, connectors, ...)
  - Modal dispersion causes pulse distortions
    - → Limit: 100 ... 300 m at 10 Gb/s
- Single−mode fiber (SMF):
  - Fiber core = 8 ...10 um
  - No modal dispersion (only one pathway mode)

Chromatic Dispersion



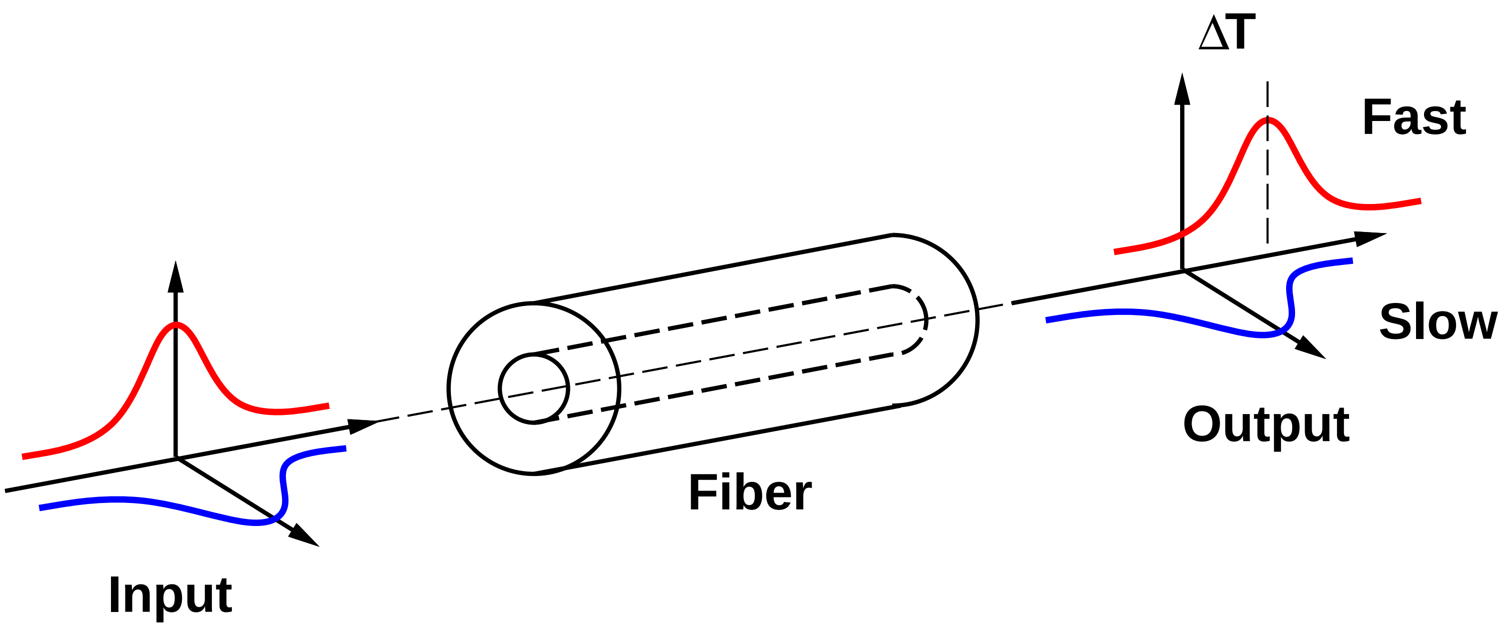
- **Standard SMF:**
  - **Almost no chromatic dispersion at 1.3 um**
  - ***D* = 17 ps/(nm km) at 1.55 um**

Pulse Spreading due to Chromatic Dispersion



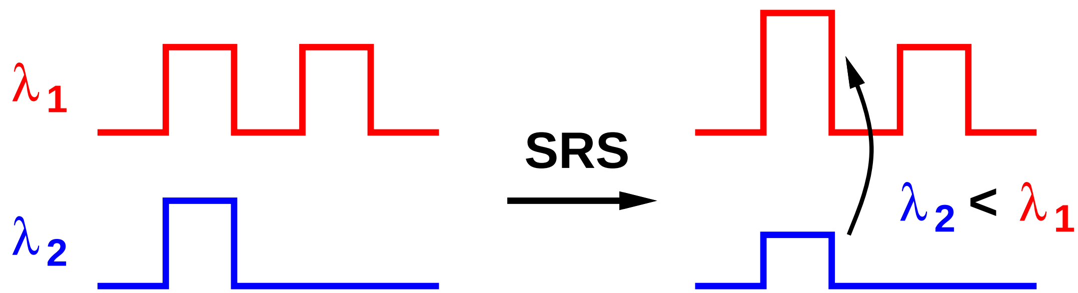
- $\Delta T = |D|\, L\, \Delta\lambda$
- **Pulse spreading depends on**
  - **Chromatic dispersion parameter *D***
  - **Link length *L***
  - **Spectral linewidth of transmitter** $\Delta\lambda$
- **Keep** $\Delta T < T_{in} / 2$

Polarization−Mode Dispersion (PMD)



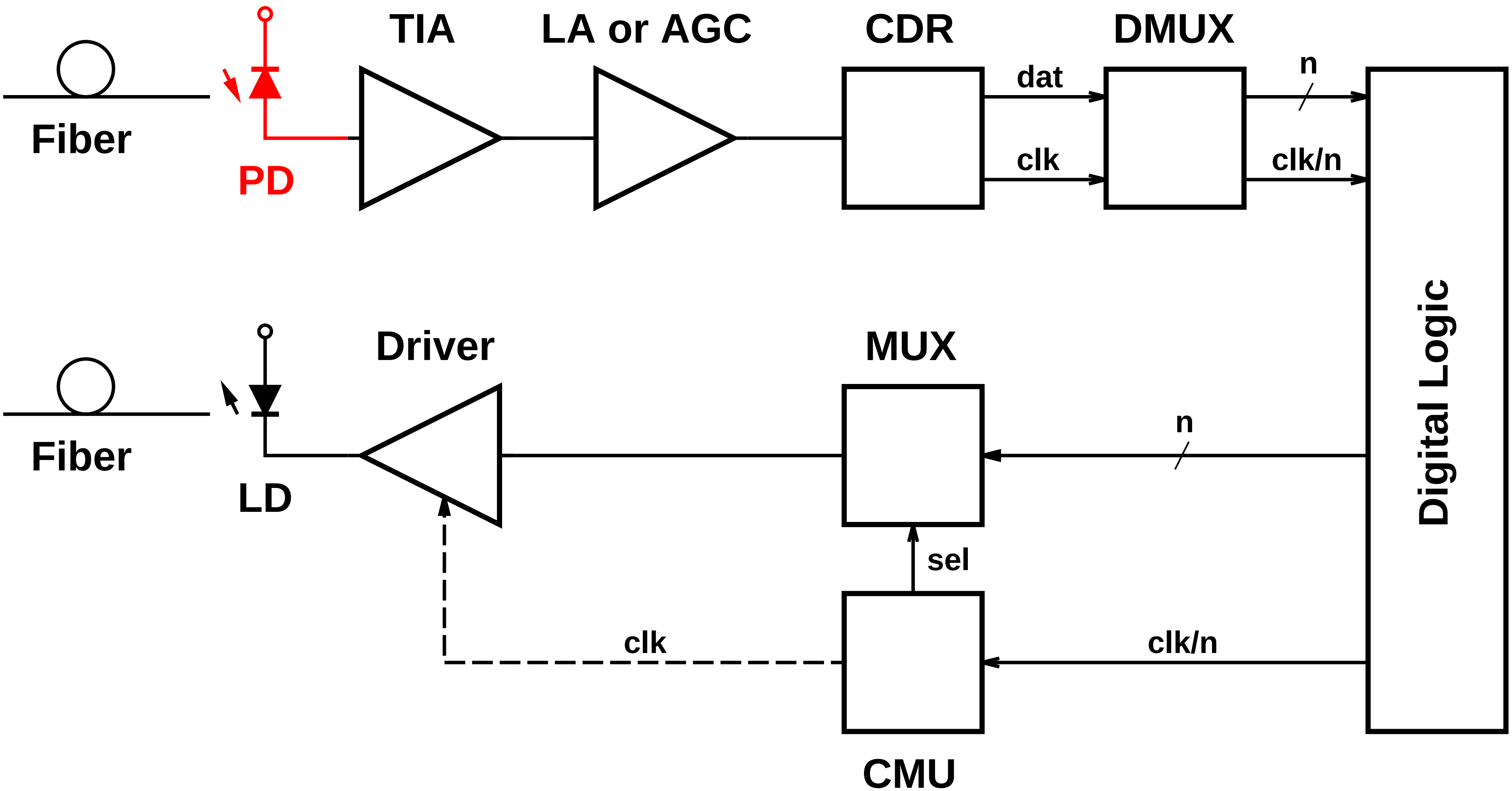
- **The two principal polarization modes propagate at different speeds**
  → Pulse distortions
- **Distortions are slowly varying with time**
- **Caused by slightly elliptic fiber core**
  - **Mostly a problem with older fiber**

Nonlinearities

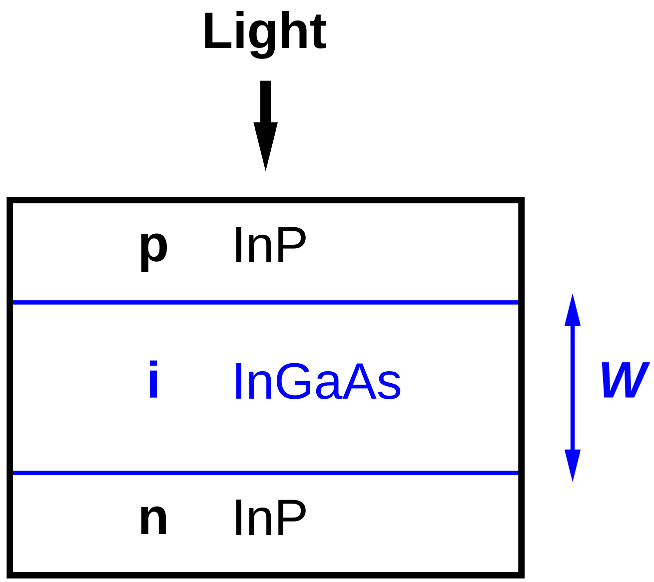


- **Nonlinear effects:**
  - **Self−phase modulation (SPM)**
  - **Cross−phase modulation (CPM, XPM)**
  - **Four−wave mixing (FWM)**
  - **Stimulated Raman scattering (SRS)**
  - **Stimulated Brillouin scattering (SBS)**
- **At high optical power levels:**
  ➞ **Pulse distortion, attenuation**
- **In WDM (wavelength division multiplexing) systems:**
  ➞ **Crosstalk between channels (see illustration)**

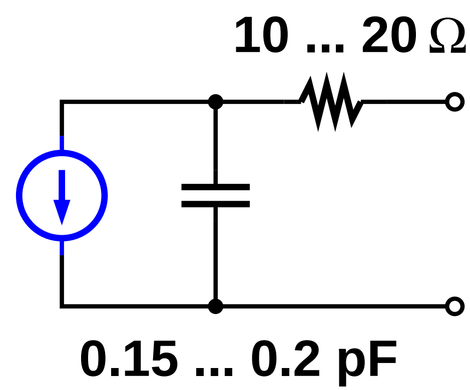
Photodetectors



p–i–n Photodetector

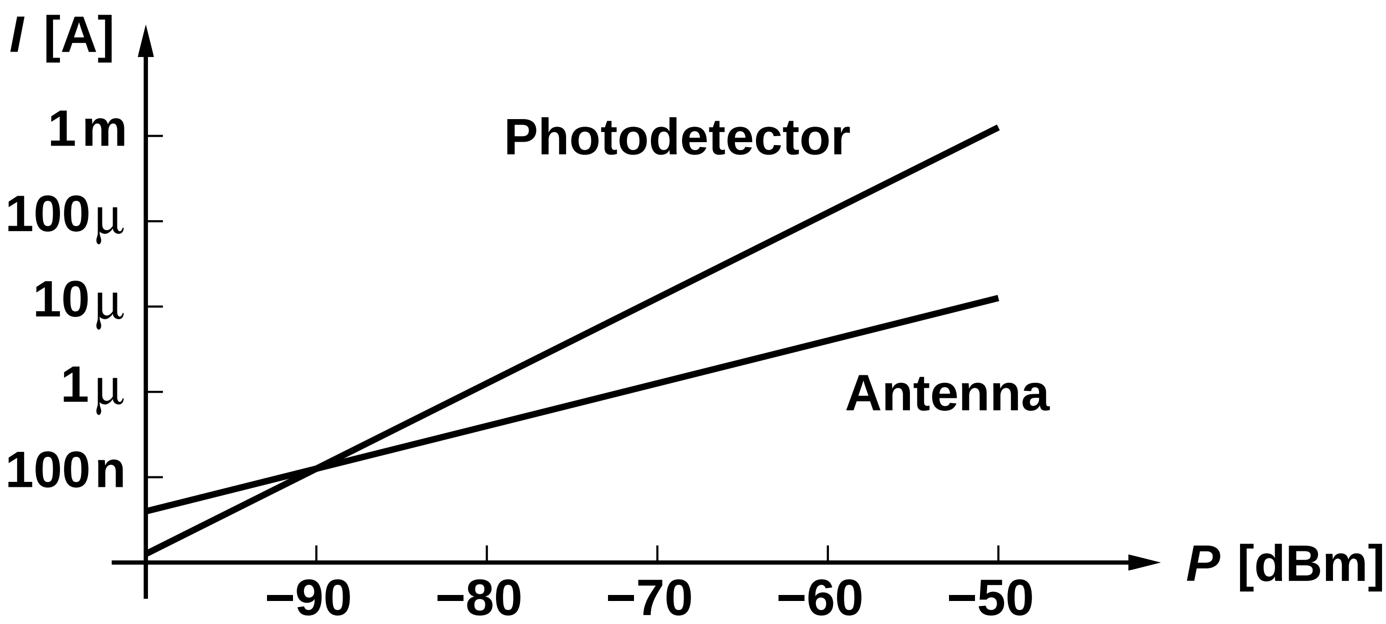


Model of 10–Gb/s p–i–n:



- **InGaAs material absorps photons at 1.0 ... 1.65 um**
- **Photodiode reverse voltage of 5 ... 10 V required**
- **Responsivity:**
  - ***R* = (electrical current) / (optical power)**
  - ***R* = 0.6 ... 0.9 A/W for InGaAs p–i–n**
- **Trade–off:**
  - **Large *W*: high quantum efficiency (high responsivity)**
  - **Small *W*: high bandwidth**

Photodetector vs. Antenna



Photodetector:

- Current ~ EM Power

  Double power (+ 3 dB)

  → 2 x current (+ 6 dB)

Antenna:

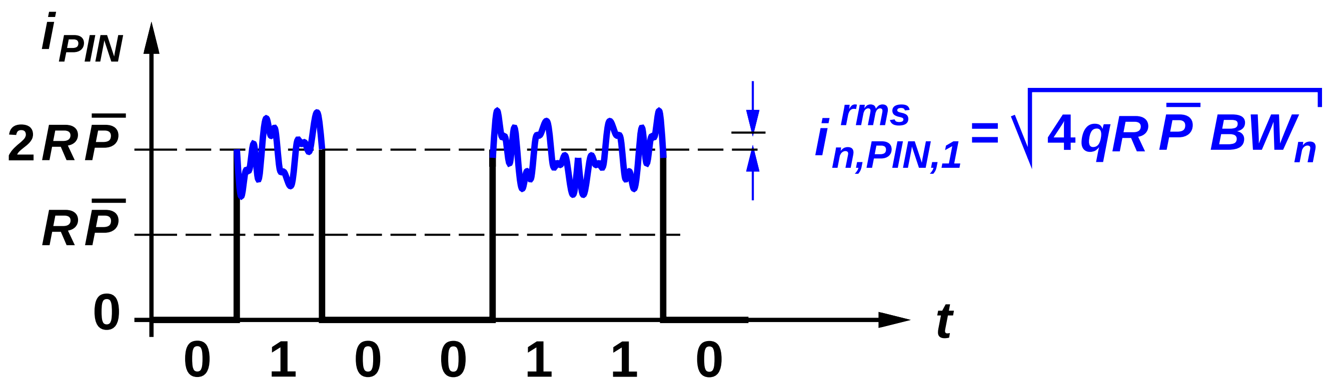
- Current ~ $\sqrt{\text{EM Power}}$

  Double power (+ 3 dB)

  → 1.41 x current (+ 3 dB)

- Warning: It is easy to get confused with dBs when going from the optical to the electrical domain!

Shot Noise



- **Shot noise caused by short current pulses (electron/hole pairs)**
- **Shot noise is signal dependent:**

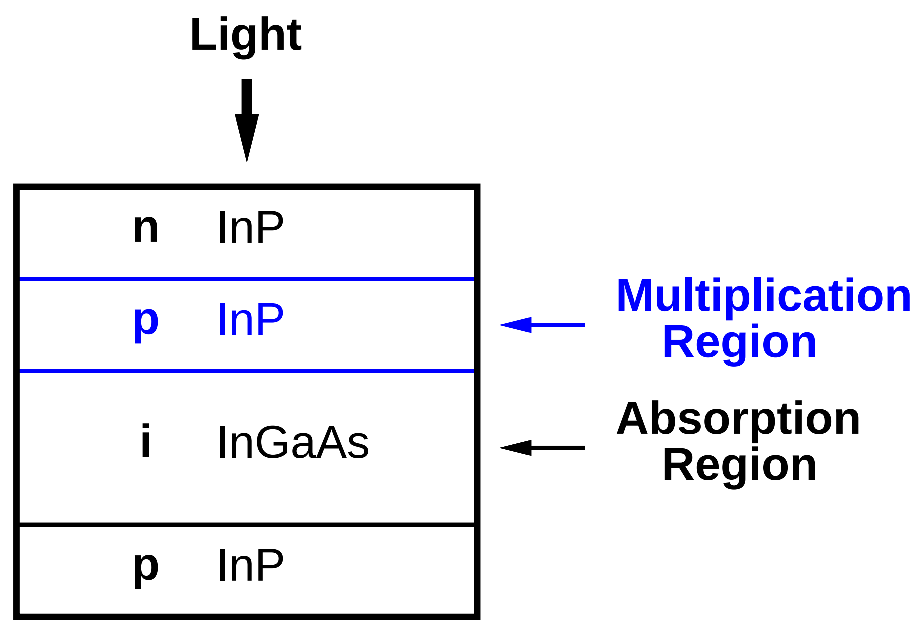
  Increase optical signal by +3 dB

  → Electrical signal: +6 dB

  → Electrical noise: +3 dB

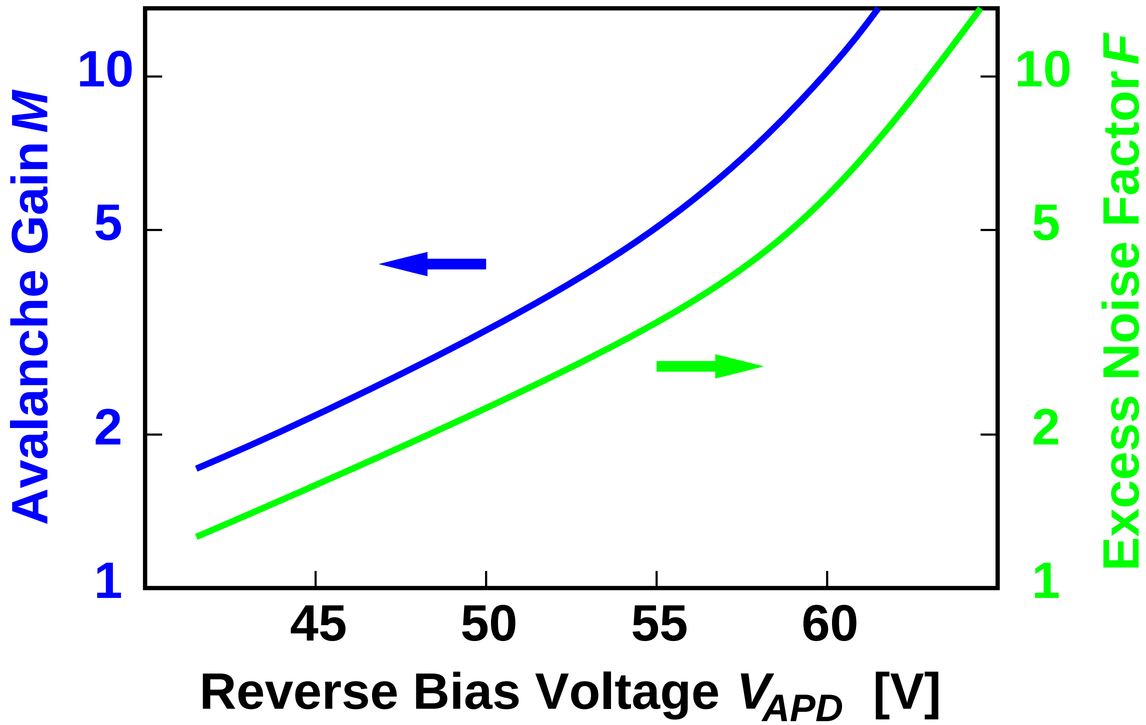
  → Electrical SNR: +3 dB
- **Shot noise on logical "ones," but not on "zeros" (ideally)**

Avalanche Photodetector (APD)



- **High reverse voltage of 40 ... 60 V required**
- **Responsivity:**
  - **Depends on avalanche gain *M***
  - R_{APD} **= 6 ... 9 A/W for** M **= 10**
- **Noise:**
  - **More noise than just amplified shot noise:**
    $\rightarrow$ **Excess noise factor *F***
- **Slower than p−i−n detector**

Dependence on Reverse Voltage

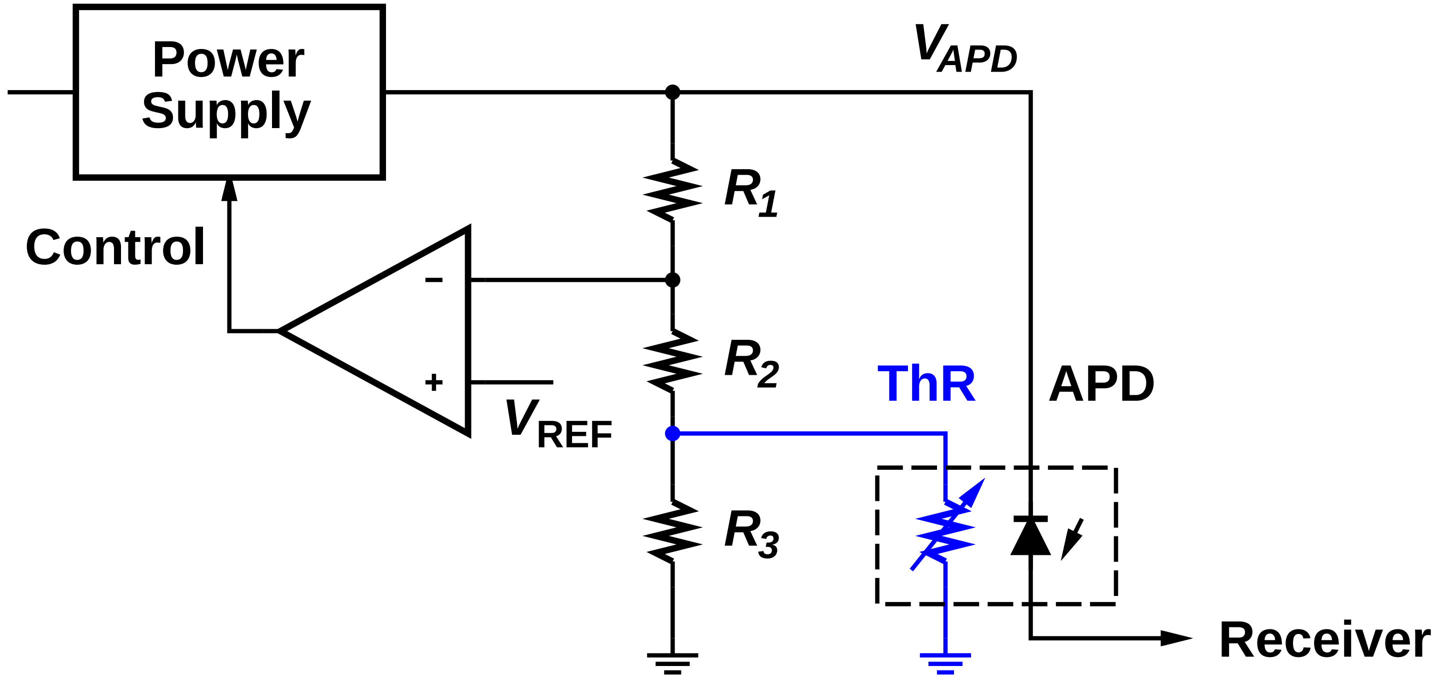


- **Avalanche gain M increases with reverse voltage**
  ... and decreases with temperature

- **Excess noise factor F increases with avalanche gain**
  Nearly linear dependence, $F(M)$, for InGaAs

- **Reverse bias controls trade−off: gain, noise, and speed**

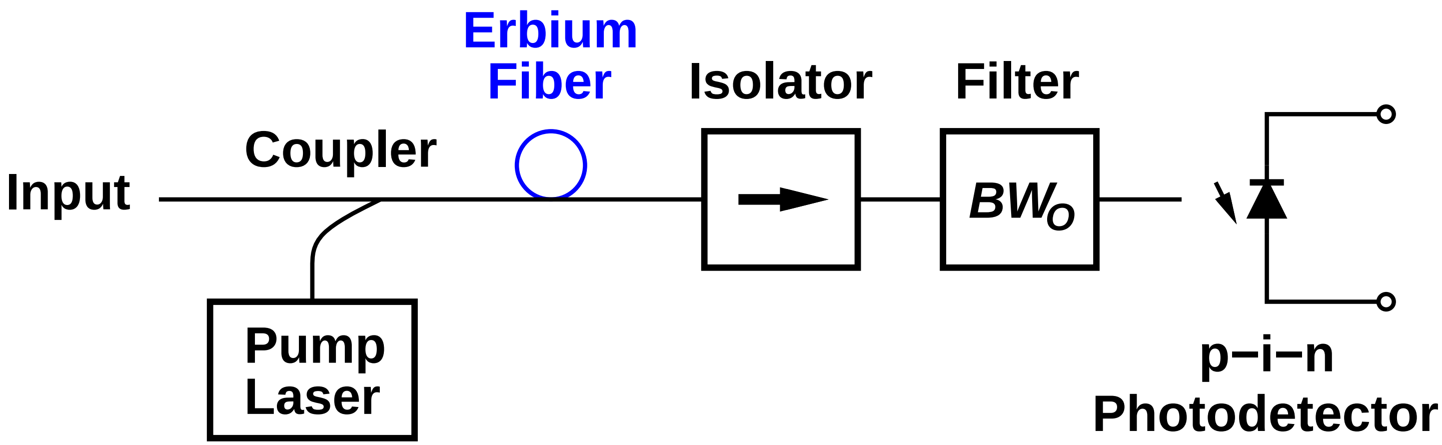
APD Bias Circuit



- Temperature compensated APD bias circuit
  - TC = +0.2% / °C

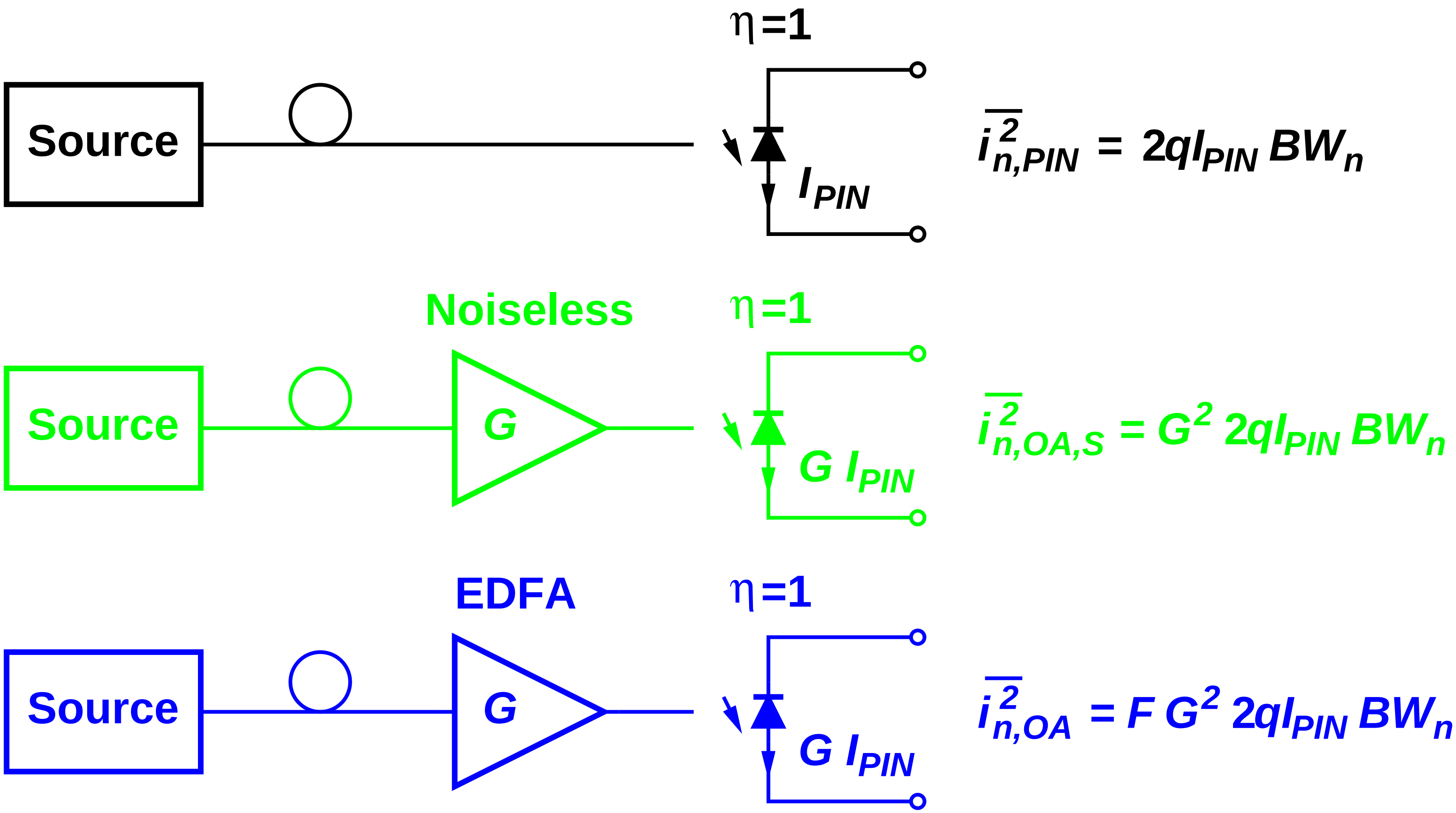
- Thermistor (ThR) packaged with APD

p−i−n Detector with Optical Preamplifier



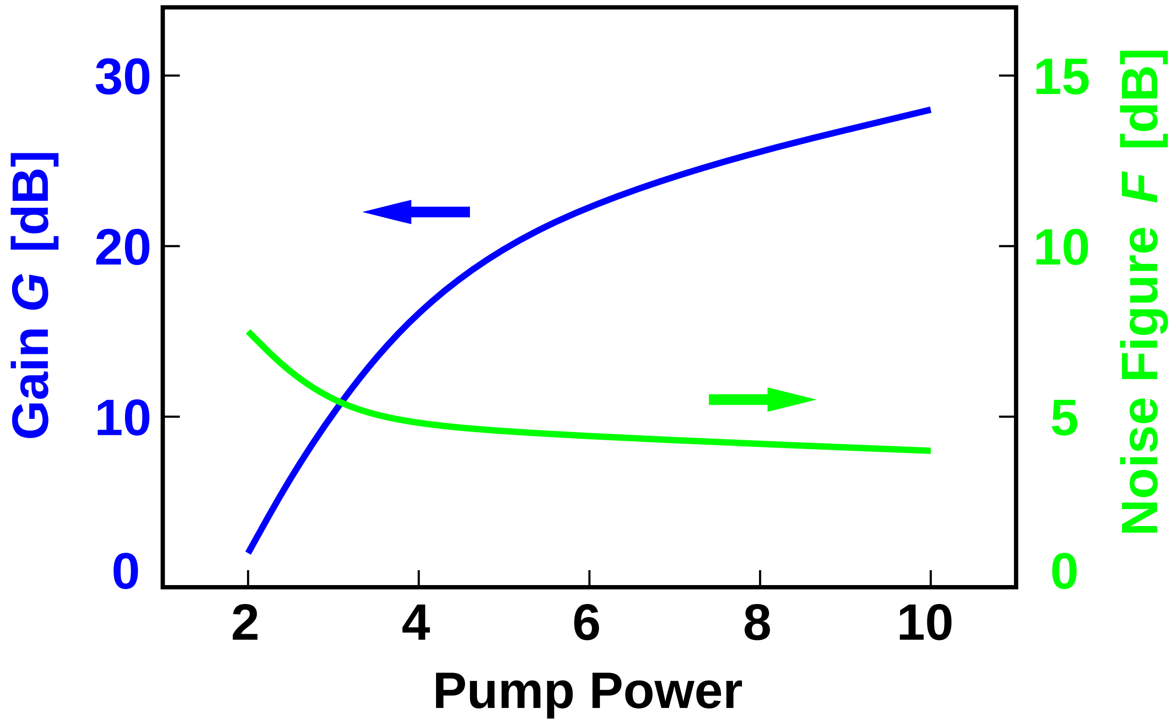
- Erbium doped fiber amplifier (EDFA) provides gain in 1.55−um band
- Responsivity:
  - Depends on optical amplifier (OA) gain G
  - R_{OA+pin} = 60 ... 90 A/W for G = 20 dB
- Noise:
  - Amplified spontaneous emission (ASE) noise
  - Reduce ASE noise with optical filter
  - Several (beat) noise components in electrical domain
  - Electrical noise is signal dependent, like shot noise

Noise Figure of Optical Amplifier



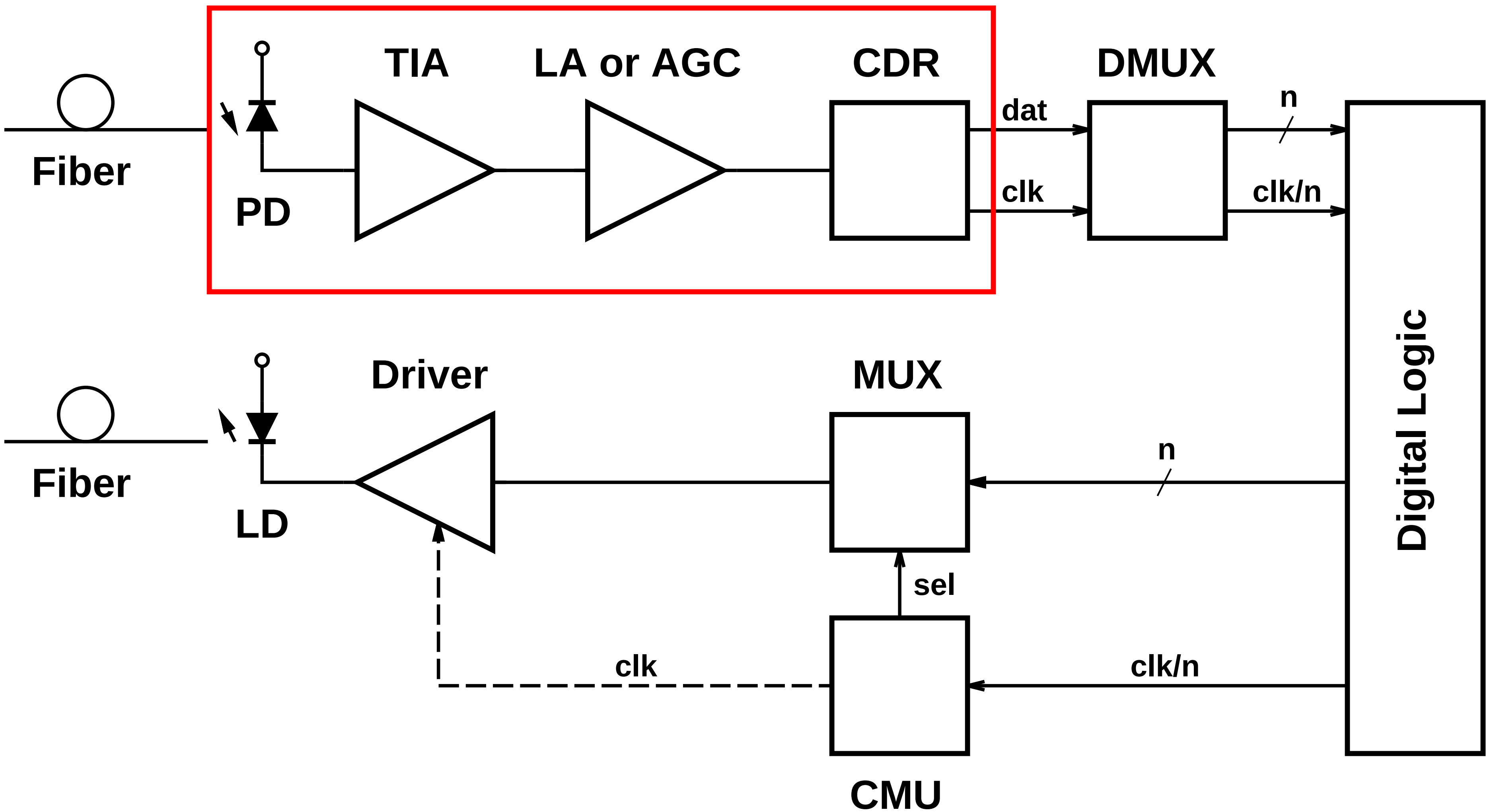
- **Noise figure F = $\dfrac{\text{total output noise power}}{\text{output noise power due to the source (shot noise)}}$**
- **Noise powers are measured in electrical domain with ideal p–i–n detectors**
- **Typical EDFA noise figure = 5 dB**

Dependence on Pump Power

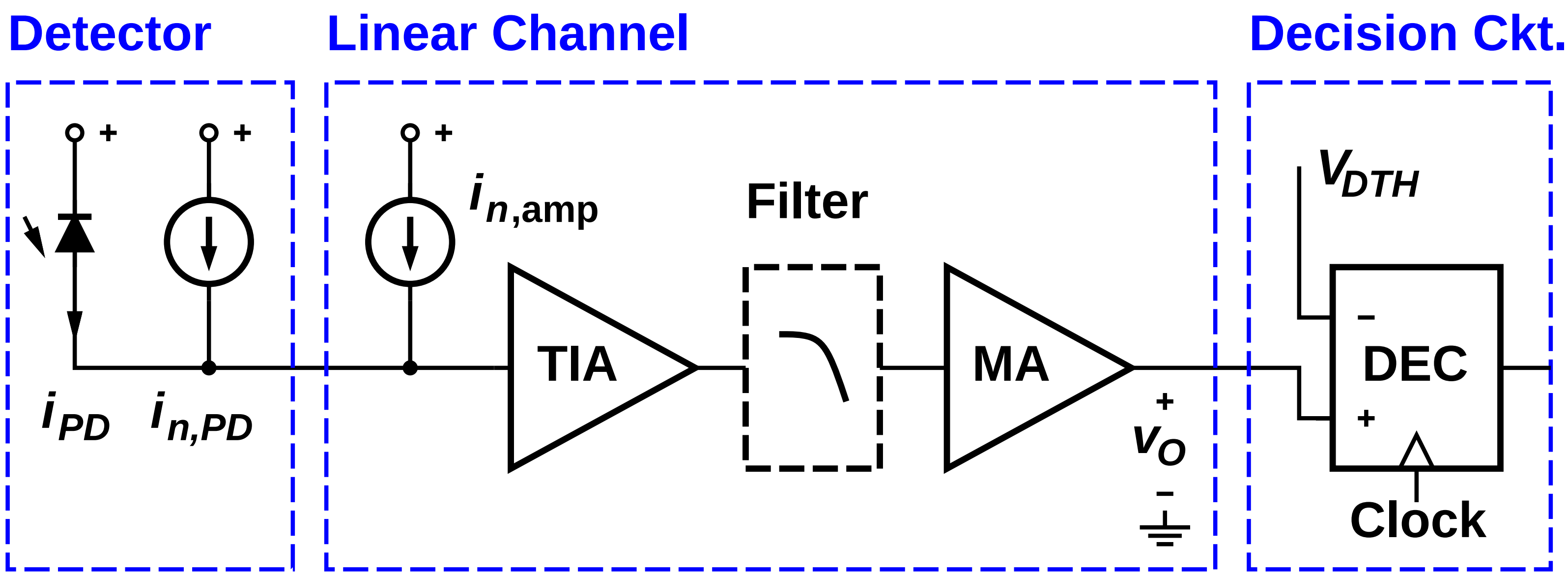


- Gain G increases with pump power
- Noise figure F decreases with pump power
- Theoretical limit F > 3 dB

Receiver Fundamentals



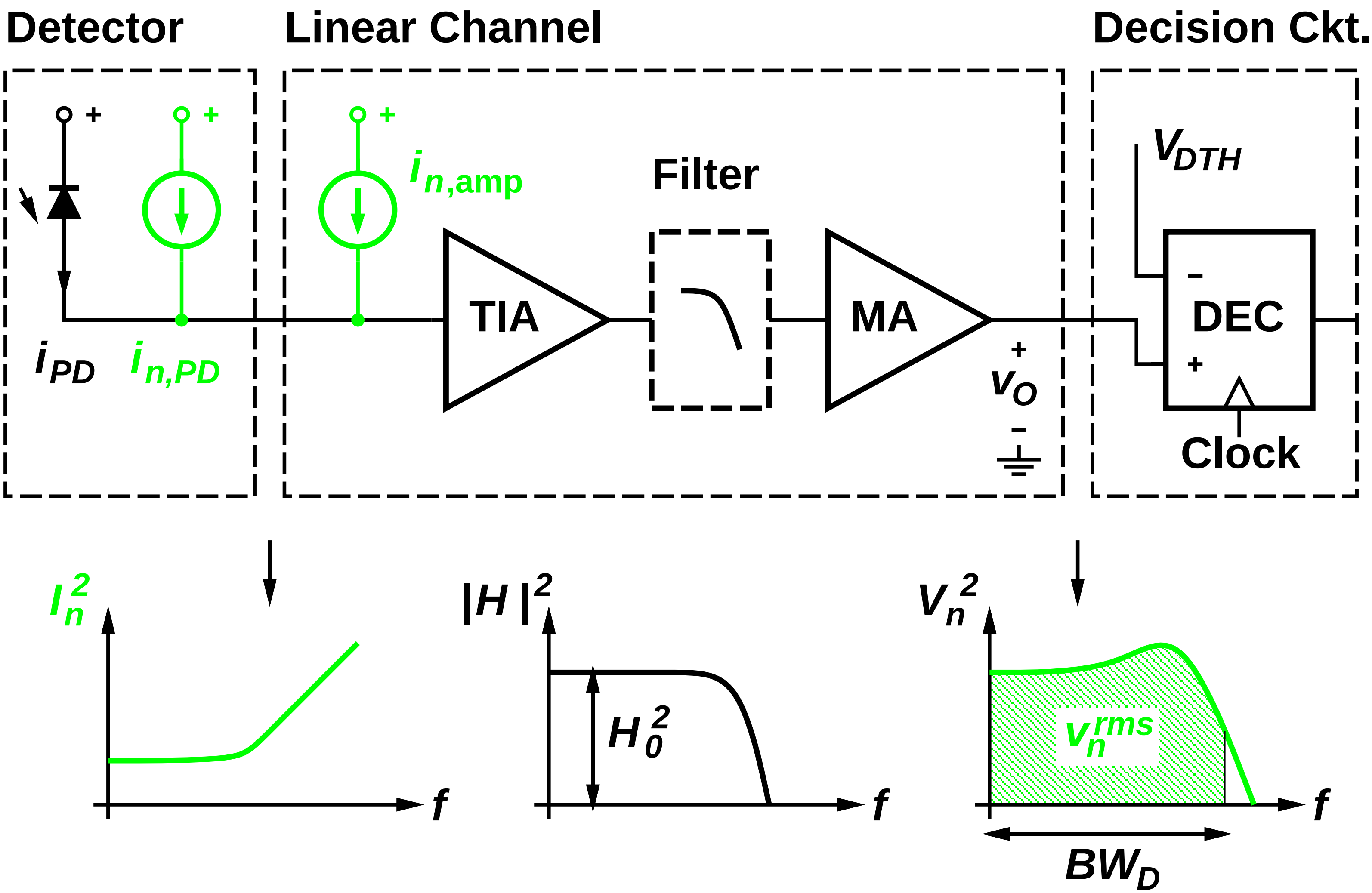
Basic Receiver Model



- How does noise impact the bit−error rate?
- What is receiver sensitivity?
- What is a power penalty?
- What is the optimum receiver bandwidth?
- Extensions of the basic receiver model ...

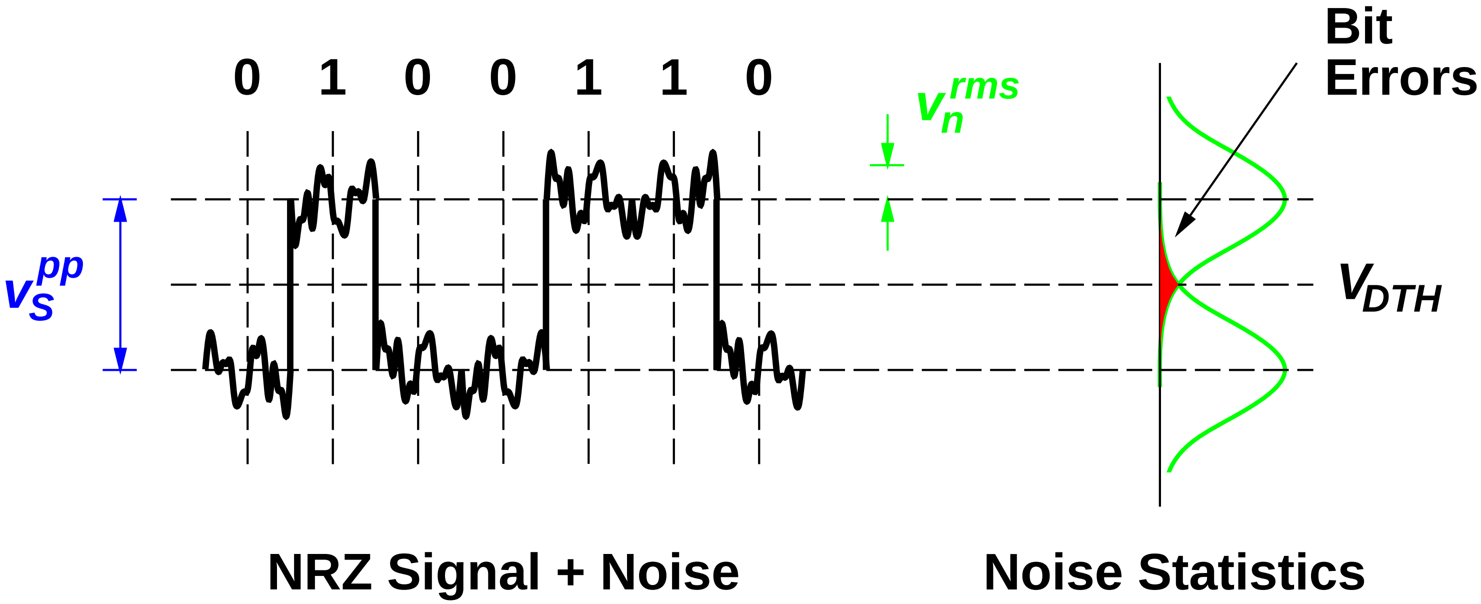
Receiver Noise

- **Calculation of output−referred rms noise:**



Receiver Noise & Bit−Error Rate

- **Output voltage of linear channel:**



$$BER = \int_Q^{\infty} \text{Gauss}(x)\, dx \quad \text{with} \quad Q = \frac{v_S^{pp}}{2\, v_n^{rms}}$$

Example: BER = 10^{-12} for $Q = 7.0$

Input−Referred Quantities

- Define input−referred signal and noise:

$$i_S^{pp} = v_S^{pp} / H_0$$

$$i_n^{rms} = v_n^{rms} / H_0$$

- Calculate BER based on input−referred quantities:

$$BER = \int_Q^{\infty} \text{Gauss}(x)\, dx \quad \text{with} \quad Q = \frac{i_S^{pp}}{2\, i_n^{rms}}$$

- Warning:

$$\overline{i_n^2} = \frac{1}{H_0^2} \int_{BW_D} |H(f)|^2 I_n^2(f)\, df \neq \int I_n^2(f)\, df$$

  - Use Personick integrals to calculate input−referred rms noise from input noise spectrum!

Receiver Sensitivity

- **Electrical sensitivity:**
  Minimum peak−to−peak signal current necessary to achieve a specified bit−error rate:

$$\boxed{i_{sens}^{pp} = 2\,Q\,i_n^{rms}}$$

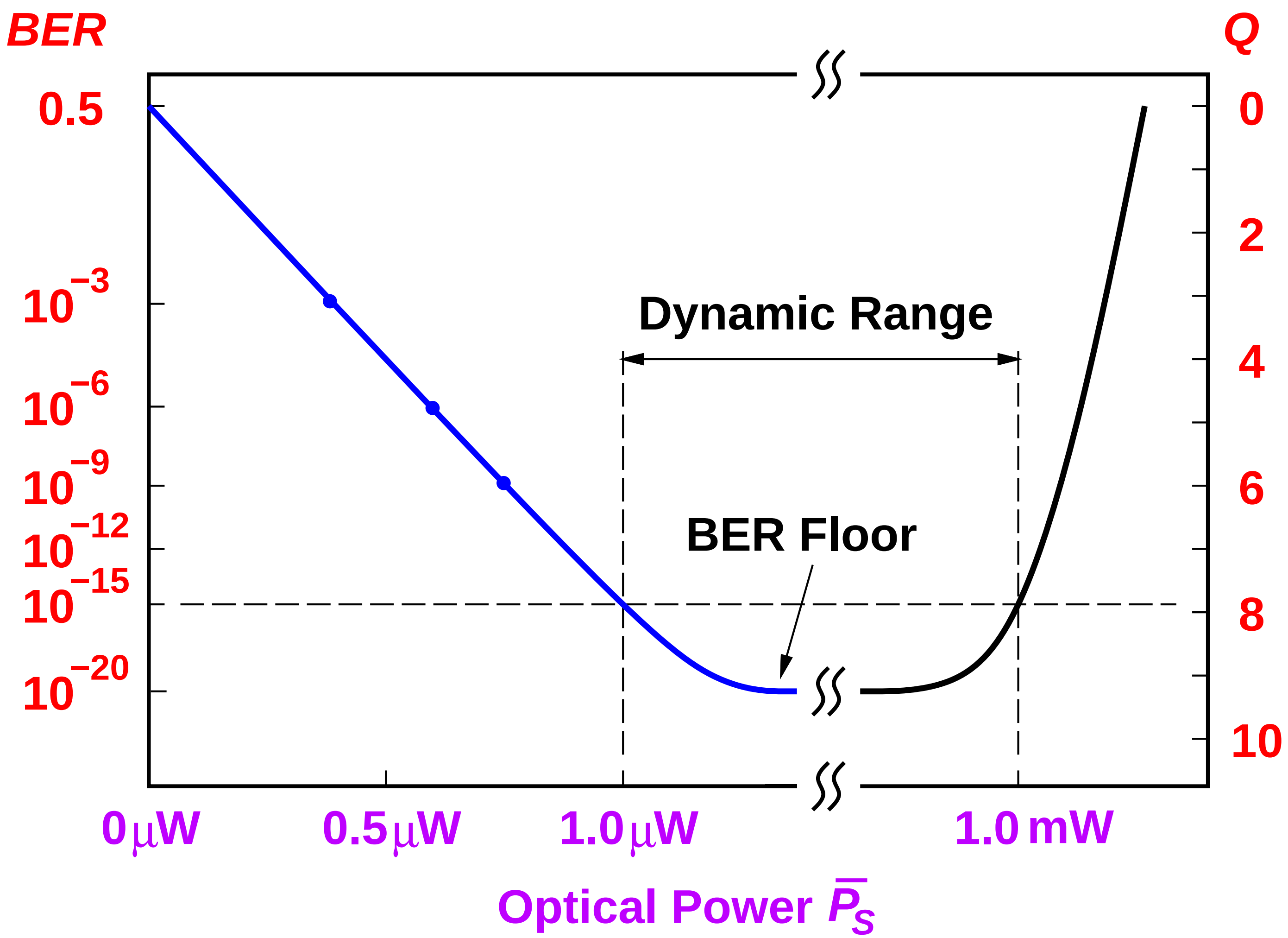
- **Optical sensitivity:**
  Minimum optical power, averaged over time, necessary to achieve a specified bit−error rate:

$$\boxed{\overline{P}_{sens} = \frac{Q\,i_n^{rms}}{R}}$$

R = responsivity of photodetector [A/W]

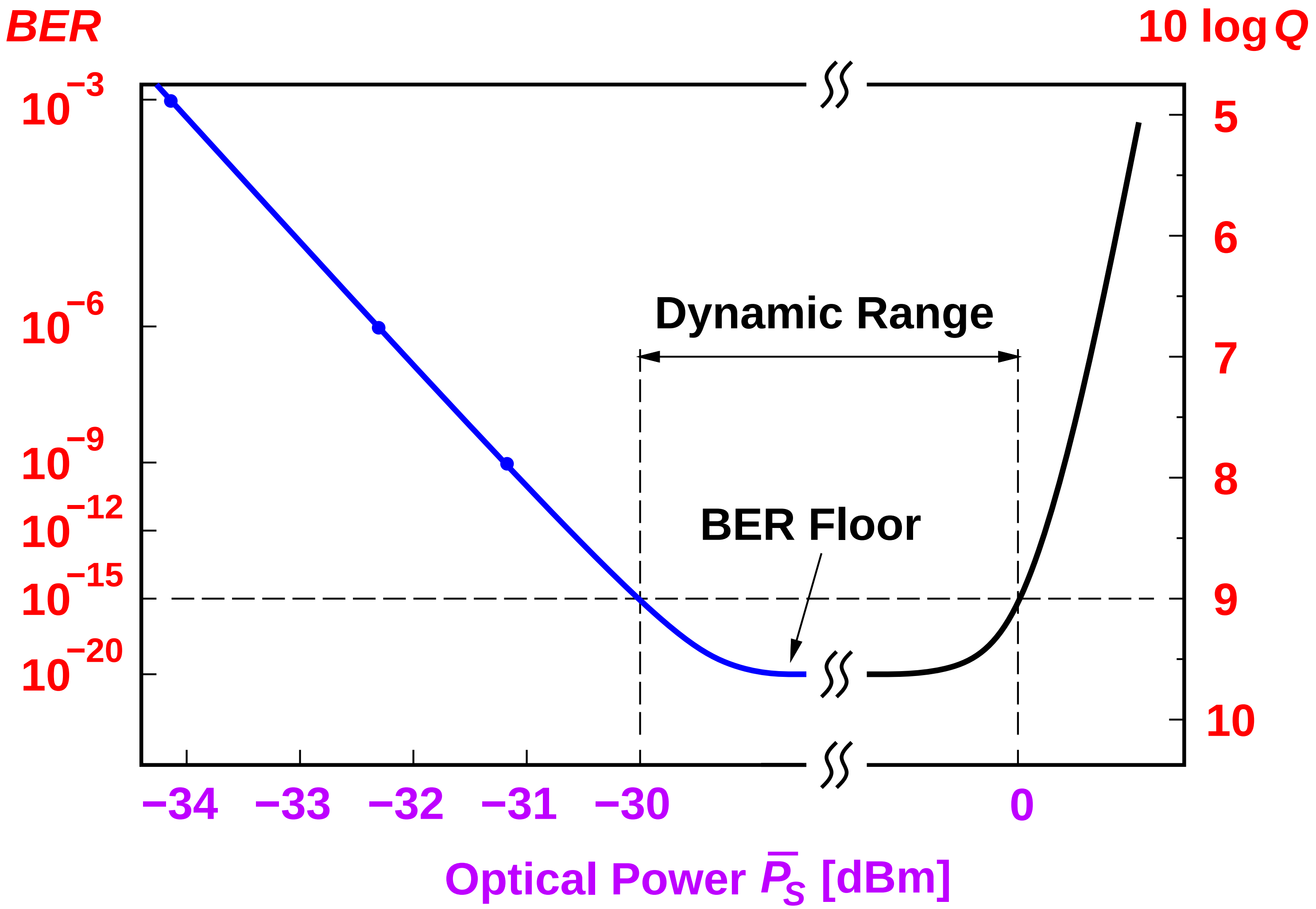
- **Typical bit−error rates used to define sensitivity:**
  - **BER = 10^{-12} Q = 7.0 SONET OC−192 (10 Gb/s)**
  - **BER = 10^{-10} Q = 6.4 SONET OC−48 (2.5 Gb/s)**

BER Plot (lin–lin Scale)



- **Linear relationship between Q and $\overline{P}_S$ for low power values**
  - **Infer receiver noise from slope**
  - **Extrapolate to low BERs (beware of the BER floor)**

BER Plot (log–log Scale)



- Linear relationship between $\log Q$ and $\log \overline{P}_S$ for low power values
  - Logarithmic power scale in dBm
  - Extrapolate to low BERs (beware of the BER floor)

Amplifier Noise and Detector Noise

- p−i−n Photodiode:
  - p−i−n photodiode (shot) noise usually is negligible
  - Most of the receiver noise contributed by amplifier
  - → Amplifier noise (TIA) mostly determines sensitivity
  - Equal amount of noise on ones and zeros
- Avalanche photodiode (APD):
  - Both amplifier noise and APD noise matters
  - → Amplifier noise (TIA) can be used to estimate sensitivity
  - More noise on ones than zeros
  - Mostly used up to 2.5 Gb/s
- Optical preamplifier followed by p−i−n photodiode:
  - Noise of optical amplifier(s) often dominates receiver noise
  - More noise on ones than zeros
  - Mostly used for 10 Gb/s and above

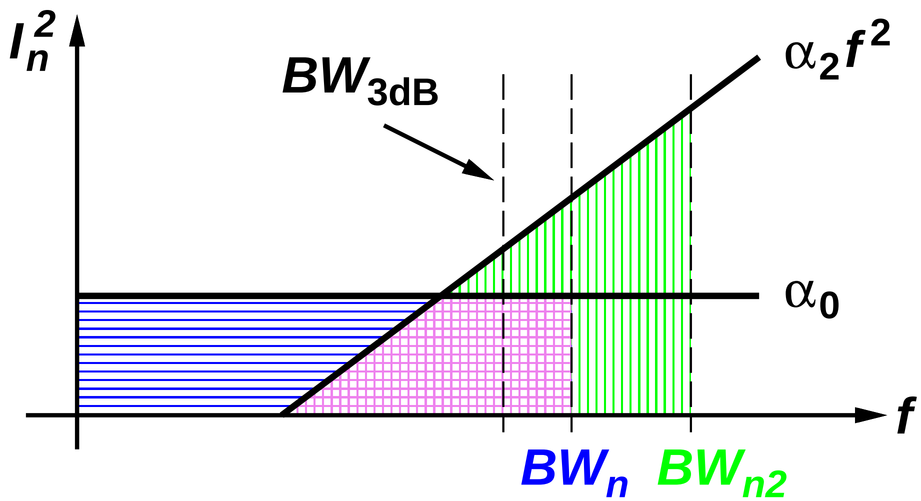
Sensitivity Examples

	2.5 Gb/s	10 Gb/s
Typical TIA noise, rms	**380 nA**	**1.4 μA**
Input signal, peak−peak, for BER =10^{-12}	**5.3 μA**	**19.7 μA**
Sensitivity @ p−i−n (*R* = 0.8 A/W)	**−24.8 dBm**	**−19.1 dBm**
Estim. sensitivity @ APD (R_{APD} = 8.0 A/W)	**−34.8 dBm**	**−29.1 dBm**
Typical sensitivity @ optical amplifier + p−i−n	−41.5 dBm	−35.6 dBm
Theoretical maximum sensitivity (quantum limit)	−53.6 dBm	−47.6 dBm

Note: 0.25 dB better sensitivity = 1 km more distance!
(standard SMF at 1.55 um, no optical in−line amps)

Personick Integrals (1)

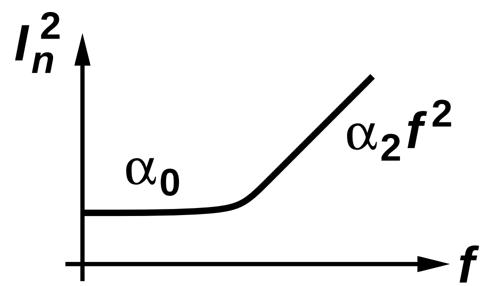
- **Can we compute the input rms noise from the input noise spectrum? Yes, but we need to integrate the white and f^2 parts separately and up to different frequencies!**



$H(f)$	BW_n	BW_{n2}
1st−order low pass	1.57 BW_{3dB}	∞
2nd order (Q=0.50)	1.22 BW_{3dB}	2.07 BW_{3dB}
2nd order (Q=0.71)	1.11 BW_{3dB}	1.49 BW_{3dB}
brick wall	1.00 BW_{3dB}	1.00 BW_{3dB}

Personick Integrals (2)

- **Input noise spectrum:** $I_n^2(f) = \alpha_0 + \alpha_2 f^2$



- **Calculate input rms noise:**

$$\overline{i_n^2} = \frac{1}{H_0^2} \int_{BW_D} |H(f)|^2 (\alpha_0 + \alpha_2 f^2)\, df$$

$$= \alpha_0 \underbrace{\frac{1}{H_0^2} \int_{BW_D} |H(f)|^2\, df}_{} + \alpha_2/3 \underbrace{\frac{3}{H_0^2} \int_{BW_D} |H(f)|^2 f^2\, df}_{}$$

$$= \underbrace{\alpha_0 \quad BW_n}_{} + \underbrace{\alpha_2/3 \quad BW_{n2}^3}_{}$$

White noise integrated up to BW_n

f^2 noise integrated up to BW_{n2}

Personick Integrals (3)

- **Noise bandwidth and Personick integrals:**
  - BW_n **is known as the "Noise Bandwidth"**
  - BW_n **and** BW_{n2}^3 **are related to the "Personick Integrals"** I_2 **and** I_3 **as follows:**

$$I_2 = BW_n / B$$

$$I_3 = BW_{n2}^3 / (3B^3)$$

where B **is the bit rate**

Power Penalty (1)

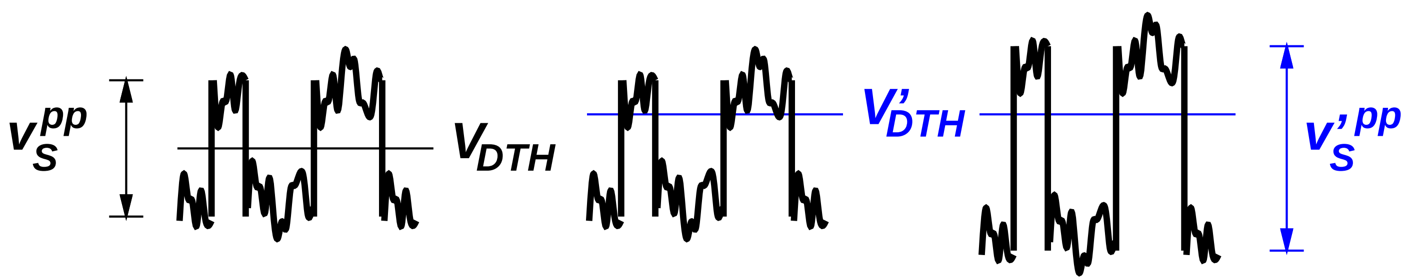
- **Definition:**

  Additional optical power needed to overcome an impairment (i.e., obtain same BER as without impairment)

  → Useful tool to quantify impairments and derive specs

- **Example:**

  Impairment = error in decision threshold:

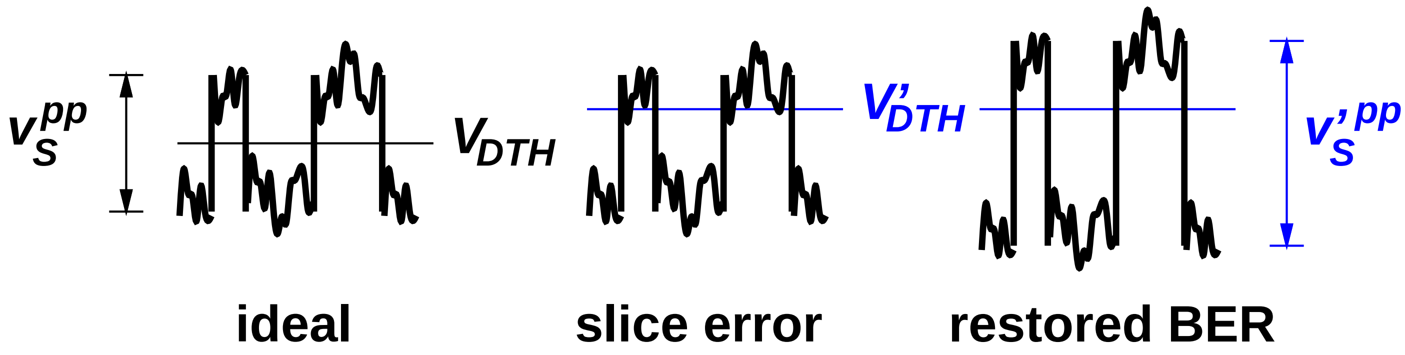


ideal **slice error** **restored BER**

$$\text{Power Penalty} = PP = \frac{v'^{pp}_S}{v_S^{pp}}$$

Power Penalty (2)

- **Calculation of power penalty (p−i−n detector w/o OA):**



$$v'^{pp}_S / 2 = v_S^{pp} / 2 + (V'_{DTH} - V_{DTH})$$

$$PP = 1 + 2\,\frac{(V'_{DTH} - V_{DTH})}{v_S^{pp}} = 1 + 2\,(\text{Slice Error})$$

→ **For a 10% slice error, we get *PP* = 0.79 dB**

- **Derivation of specs from power penalty:**

$$(\text{Slice Error}) = (PP - 1) / 2$$

→ **For *PP* < 0.05 dB, we need a slice error < 0.58%**

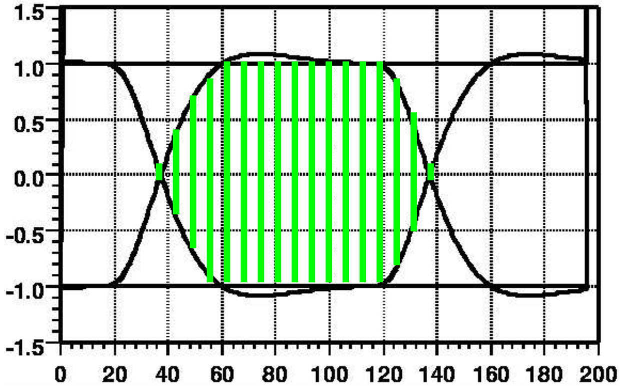
Receiver Bandwidth

- What is the optimum receiver bandwidth?
  - High bandwidth:
    - → Noise causes errors
  - Low bandwidth:
    - → Intersymbol interference (ISI) causes errors

  → **Good trade−off: bandwidth = 2/3 bit rate** (for NRZ modulation)

- Example (next slide):
  - Signal: 10−Gb/s NRZ
  - Noise: white (frequency independent)
  - Filter: second−order Butterworth response
    (maximally flat amplitude response)
    3−dB bandwidth @ 13.33, 6.67, and 3.33 GHz

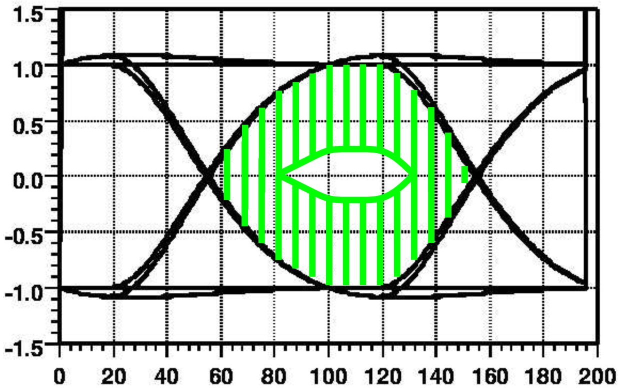
Receiver Bandwidth Examples



Bandwidth = 4/3 bit rate

(= 13.33 GHz @ 10 Gb/s)

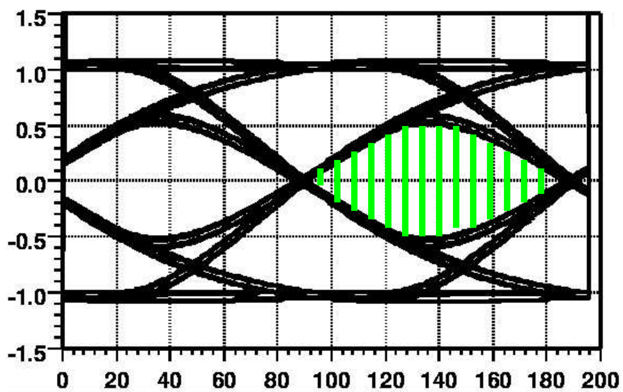
Noise = 1.0 units



Bandwidth = 2/3 bit rate

(= 6.67 GHz @ 10 Gb/s)

Noise = 0.71 units



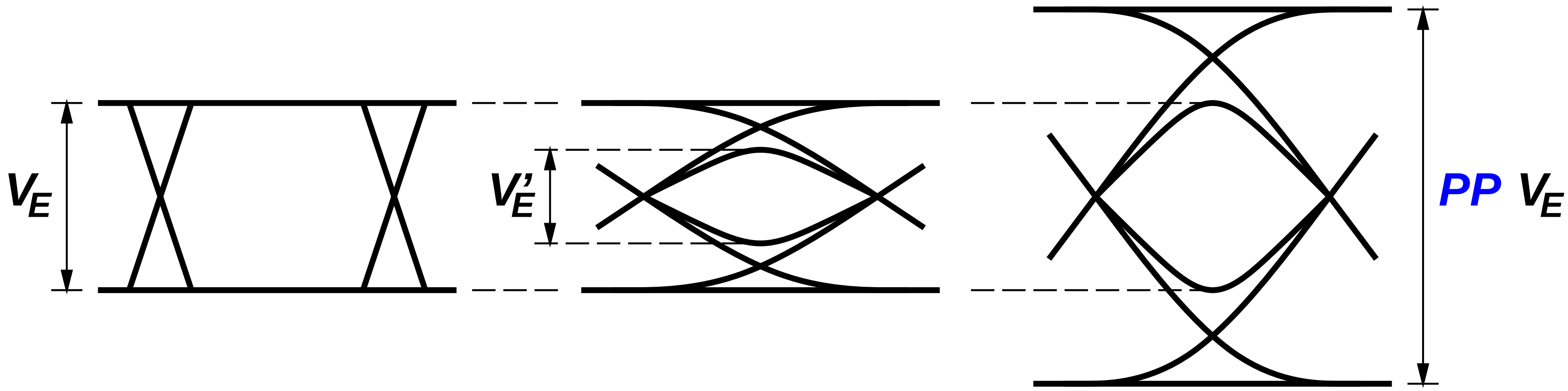
Bandwidth = 1/3 bit rate

(= 3.33 GHz @ 10 Gb/s)

Noise = 0.5 units

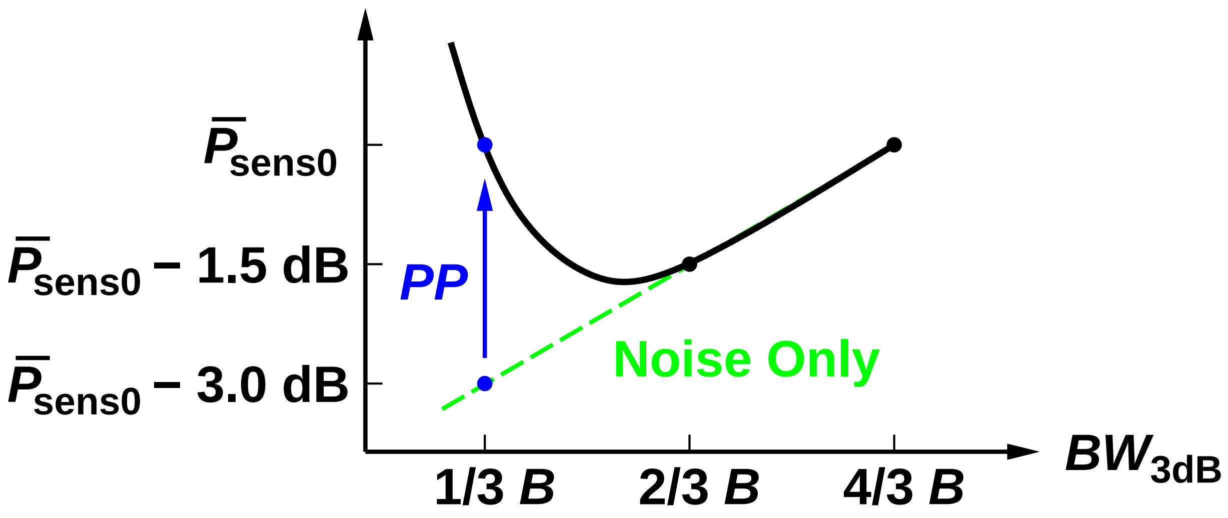
Power Penalty due to ISI

- **Power penalty (*PP*) is the additional optical power needed to restore the BER in the presence of ISI:**



Without ISI | **With ISI** | **With ISI and increased power to restore BER**

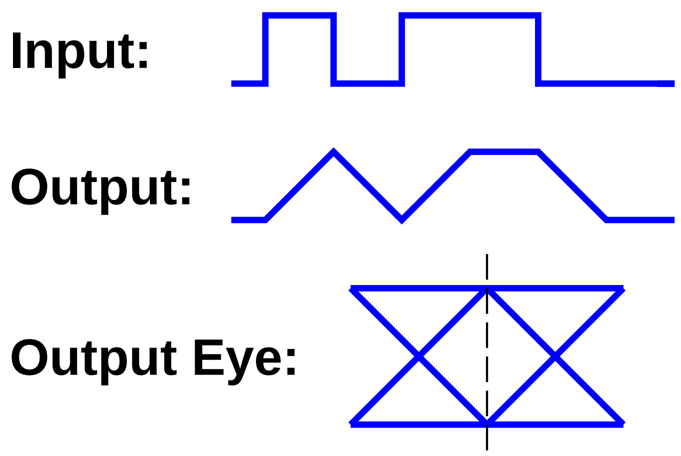
Optimum Receiver Bandwidth

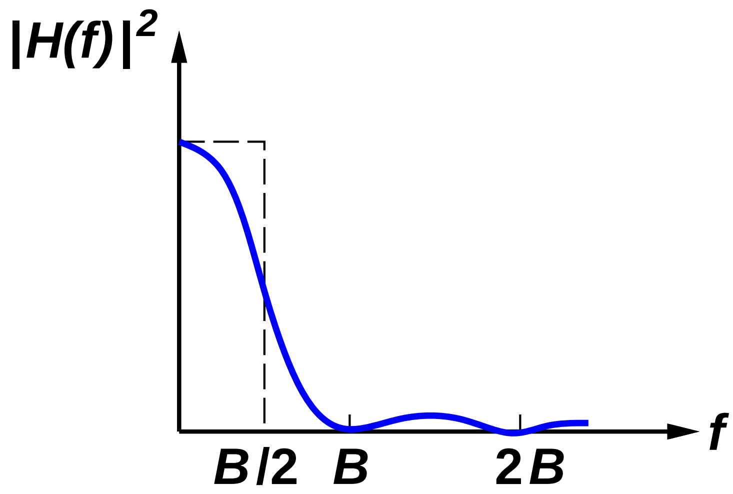


- Sensitivity degrades at high bandwidths due to noise
- Sensitivity degrades at low bandwidths due to ISI
- Optimum receiver bandwidth is about 2/3 of the bit rate

Rectangular Receiver Response

- Rectangular filter is the optimum frequency response to receive undistorted NRZ pulses with white noise:





- 3−dB bandwidth is $0.44B$
- Noise bandwidth is $0.50B$
- Zero ISI when sampling at the center of the eye
- Implementation with "integrate & dump" circuit
- But in practice, pulses are distorted and noise is not white ...

Bandwidth Allocation

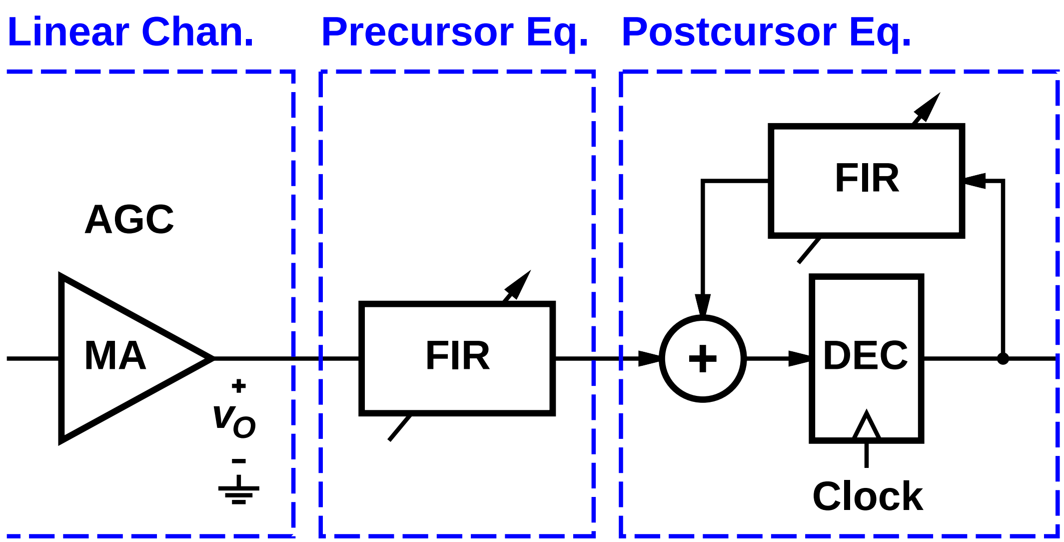
- How do we choose the bandwidth for the TIA, MA, etc. ?

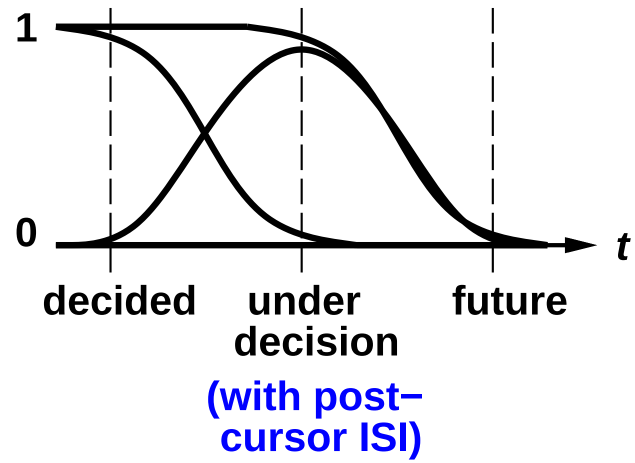
  Goal: combined bandwidth = 2/3 B

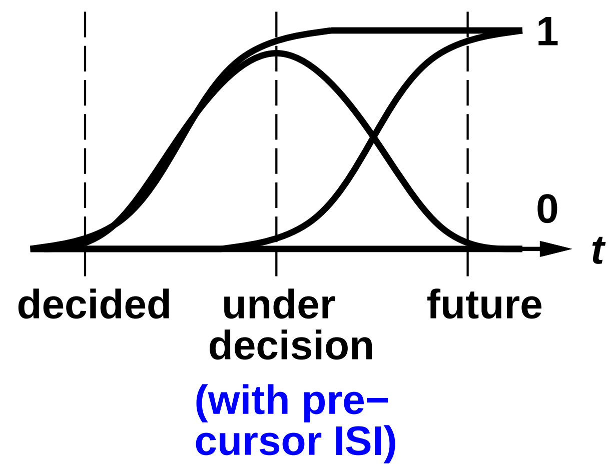
  $1/BW^2 \approx 1/BW_1^2 + 1/BW_2^2 + 1/BW_3^2 + ...$

- Several strategies:
  - Use precise filter with bandwidth 2/3 B
    Make all other components (det., TIA, MA, CDR) wideband ($\gg$ 2/3 B)
    → Good stability, controlled frequency response
  - Make bandwidth of TIA equal 2/3 B
    Make all other components wideband ($\gg$ 2/3 B)
    → Permits low−noise TIA, saves filter
  - Make bandwidth of all components about B
    In combination the bandwidth will be about 2/3 B
    → Used in high−speed receivers (10 Gb/s +)

Adaptive Equalizer







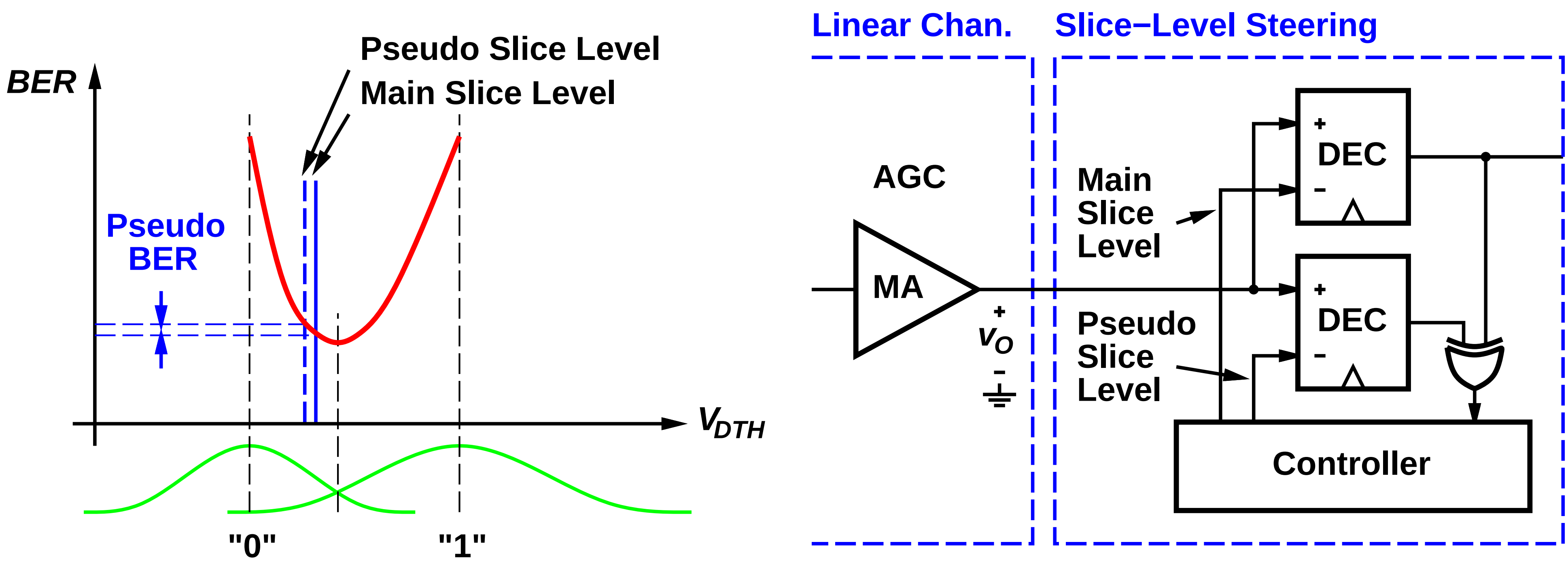
- **Cancel ISI due to fiber dispersion and receiver response**

  → Adapt to changing pulse shapes

- **Popular implementation:**

  Decision−feedback equalizer (DFE)
  - **Precursor equalizer (linear FIR)**
  - **Postcursor equalizer (nonlinear)**

Decision Threshold Control

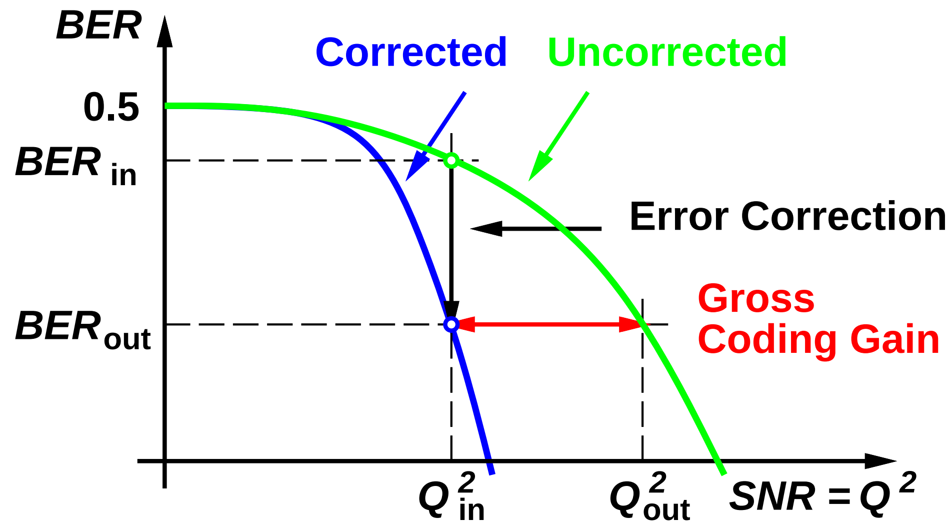


- **Optimum decision threshold is not at halfway point for receivers with APD or OA + p−i−n (more noise on ones than zeros)**
- **Find optimum automatically with slice−level steering**

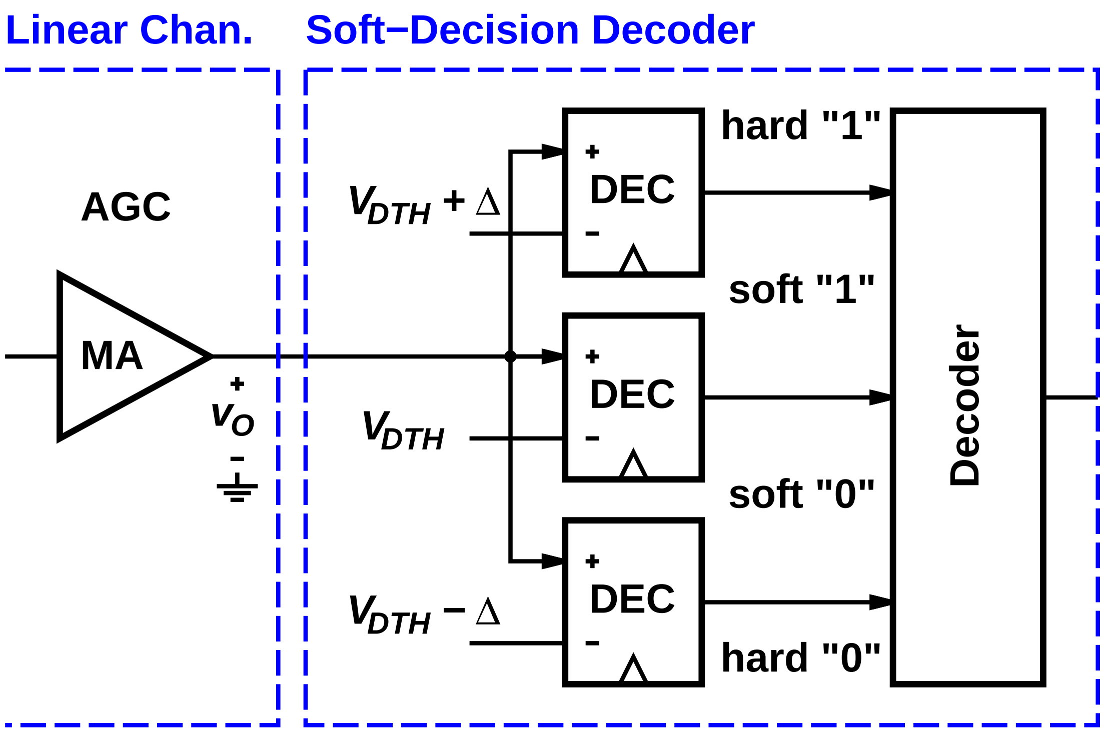
Forward Error Correction (FEC)

- **Forward error correction improves BER**

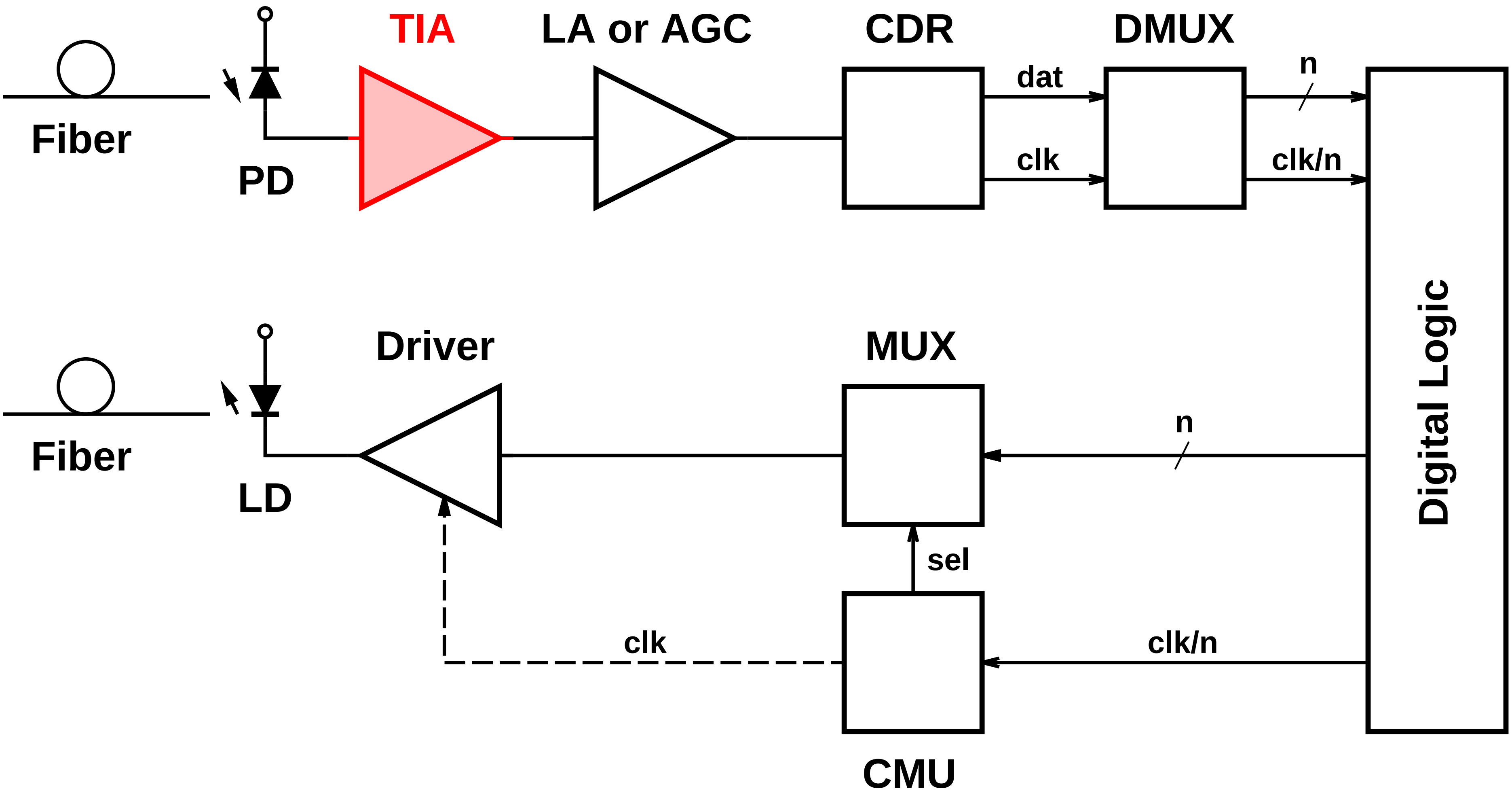
  Example:
  Input BER = 10^{-4} (after CDR)
  Output BER = 10^{-12} (after decoder)
  Bit−rate overhead = 7%
  Gross coding gain = 5.5 dB



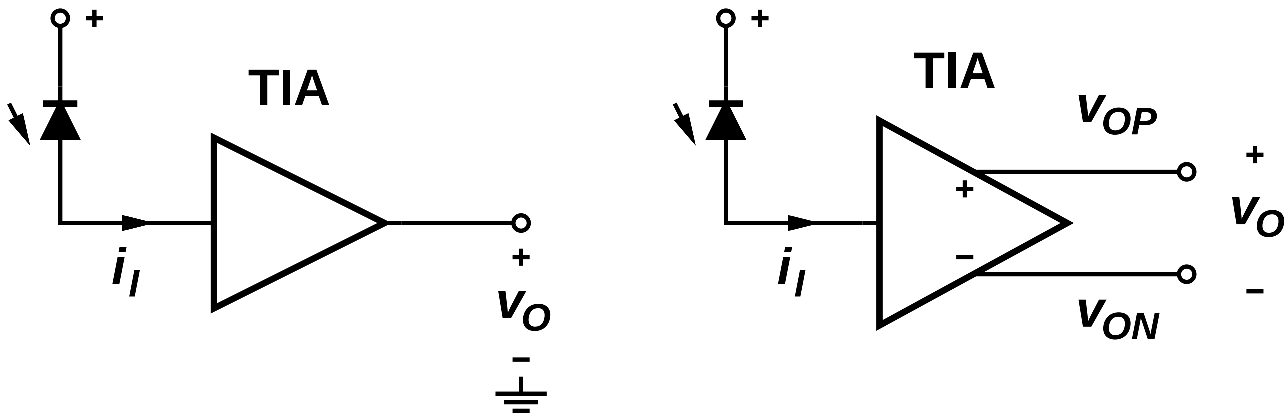
- **Two types of decoder:**
  - **Hard−decision decoder:**
    Binary slicer followed by decoder
  - **Soft−decision decoder:**
    Multilevel slicer followed by decoder (better performance)



Transimpedance Amplifier (TIA)

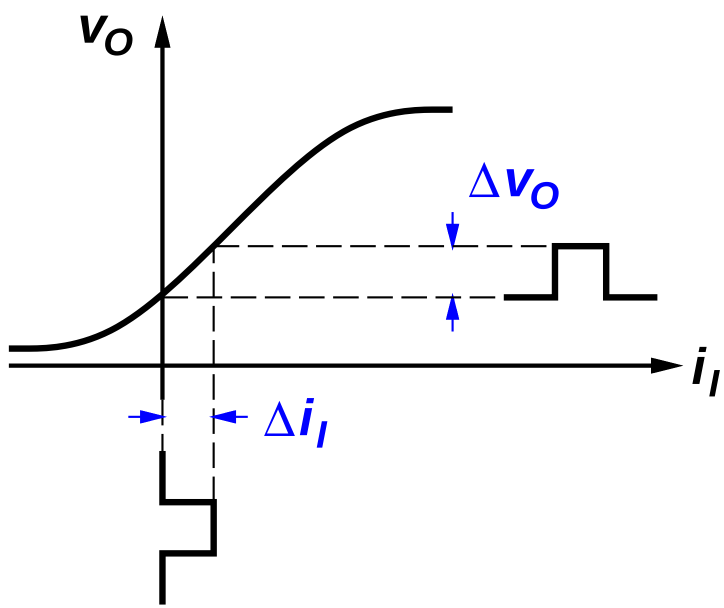


Transimpedance



- **Transimpedance definition:**

$$Z_T = \frac{\Delta v_O}{\Delta i_I} \qquad [\Omega, \text{dB}\Omega]$$



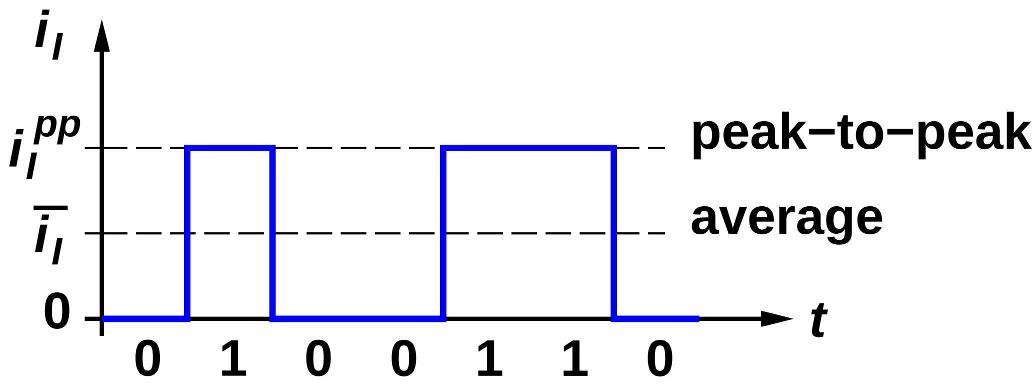
- **Typical values:**

  2.5 Gb/s: 2.0 kΩ ... 4.0 kΩ
  10 Gb/s: 500 Ω ... 2.0 kΩ

- **Generally, faster TIAs have lower transimpedance**

Input Overload Current

- TIA input signal:

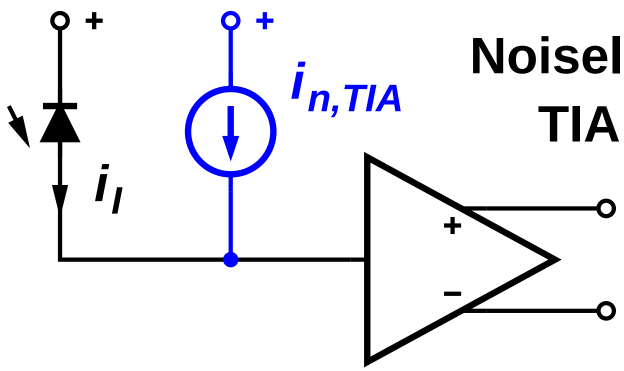


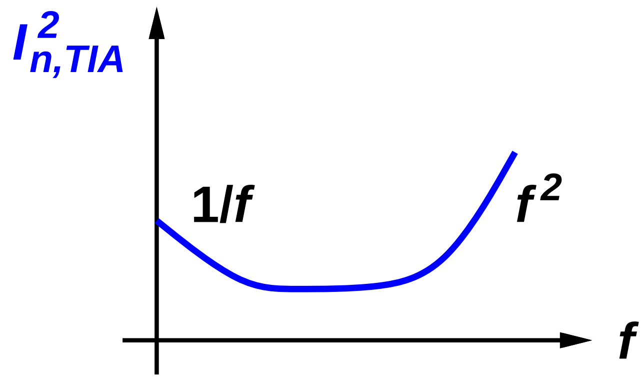
- Input overload current:
  - Maximum peak−to−peak input current before pulse−width distortion and jitter degrade BER
  - Typical value: 1.5 ... 2.5 mA

- Maximum input current for linear operation:
  - Maximum peak−to−peak input current before nonlinear distortions become harmful
  - e.g., input current for 1−dB gain compression

Input−Referred Noise Current

- Model TIA noise with equivalent noise current source at the input:





- Noise current depends on source impedance (PD capacitance)
- Input−referred noise current spectrum is not white
- Input−referred rms noise current is calculated by integrating the output noise and referring it back to the input (Personick integrals!)
- Typical values:
  2.5 Gb/s: 380 nA rms
  10 Gb/s: 1,400 nA rms
- Generally, faster TIAs are noisier

Bandwidth & Group−Delay Variation

- Depends on bandwidth allocation strategy
  The TIA bandwidth is usually 0.6 ... 1.2 the bit rate

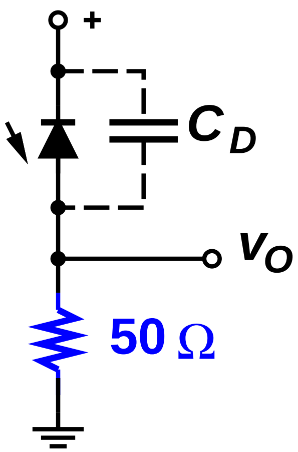
- Typical values:
  2.5 Gb/s: BW = 1.5 ... 3 GHz
  10 Gb/s: BW = 6.0 ... 12 GHz

- Group−delay variation (phase linearity) also causes distortions (ISI and jitter)
  → Limit group−delay variations over bandwidth to less than 0.1 unit interval (UI)

- Typical values:
  2.5 Gb/s: $|\Delta\tau| < 40$ ps
  10 Gb/s: $|\Delta\tau| < 10$ ps

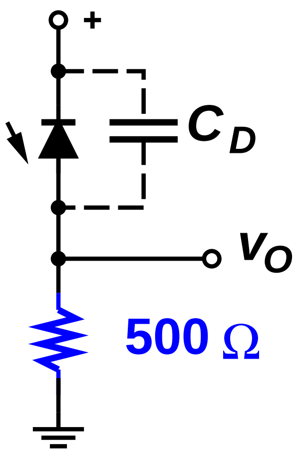
Low− and High−Impedance Front−Ends

Low−impedance front−end:



- Low transimpedance
- Fast
- Noisy
- High overload

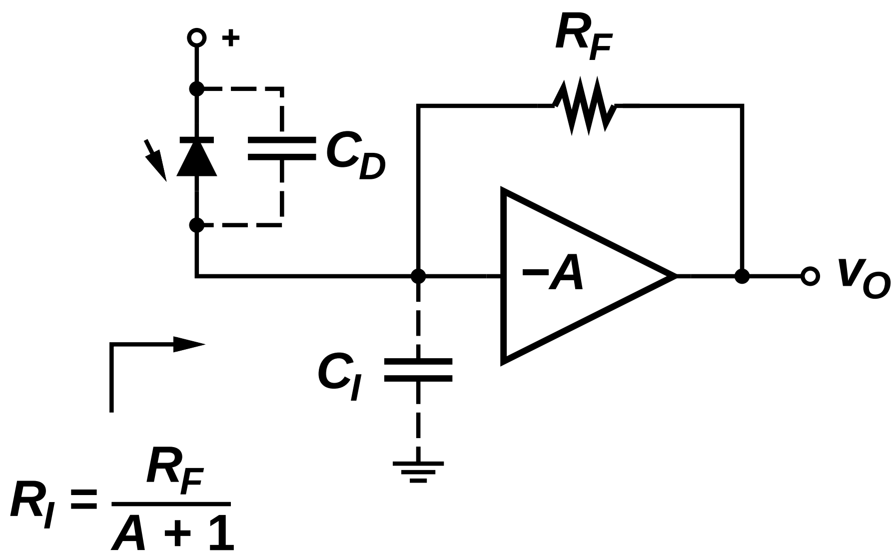
High−impedance front−end:



- High transimpedance
- Slow
- Low noise
- Low overload

Shunt Feedback TIA (1)

- **Principle (single ended):**



$$Z_T(s) = -R_T \frac{1}{(1+sT)}$$

$$R_T = \frac{A}{A+1} R_F$$

$$BW = \frac{1}{2\pi} \frac{A+1}{R_F C_T}$$

with $C_T = C_D + C_I$

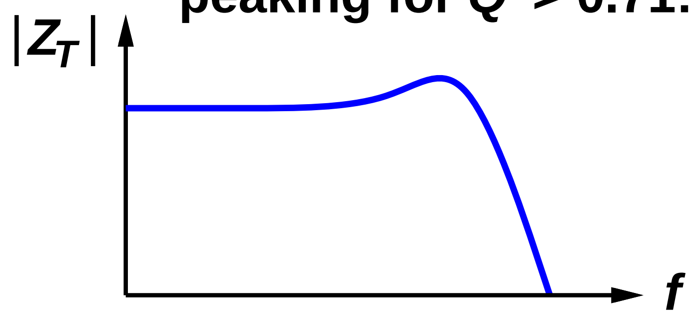
- **Assumptions for amplifier:**
  - Bandwidth $\rightarrow \infty$
  - Input resistance $\rightarrow \infty$

Shunt Feedback TIA (2)

- Consider amplifier with one pole at f_A:

$$Z_T(s) = -R_T \frac{1}{(1 + sT/Q + s^2T^2)}$$

peaking for $Q > 0.71$:



- For flat pass band ($Q < 0.71$):

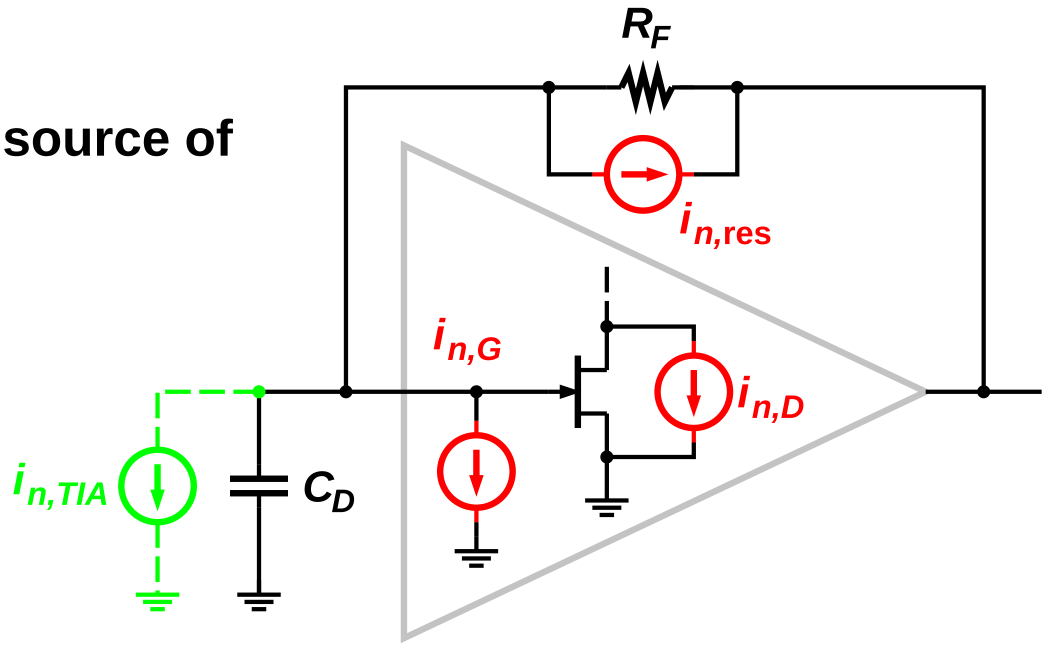
Amplifier pole: $f_A > \frac{1}{2\pi} \frac{2A}{R_F C_T}$

- TIA bandwidth: $BW = \frac{1}{2\pi} \frac{\sqrt{2A(A+1)}}{R_F C_T}$ (for $Q = 0.71$)

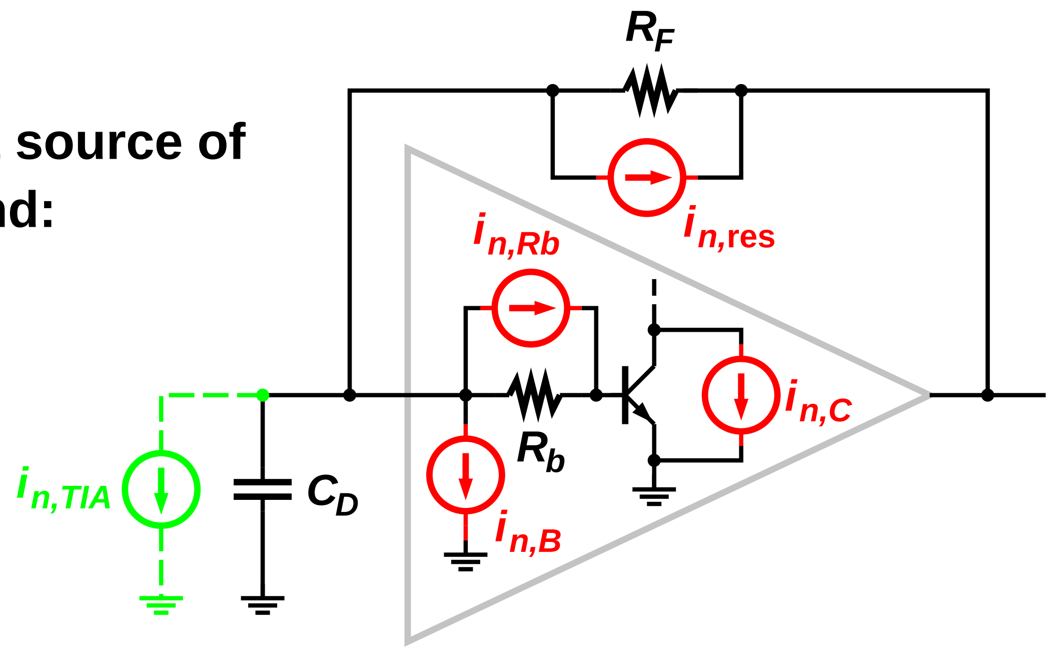
- Transimpedance limit: $\boxed{R_T < \frac{A f_A}{2\pi C_T BW^2}}$

TIA Noise Optimization (1)

- **Equivalent noise current source of TIA with FET front−end:**

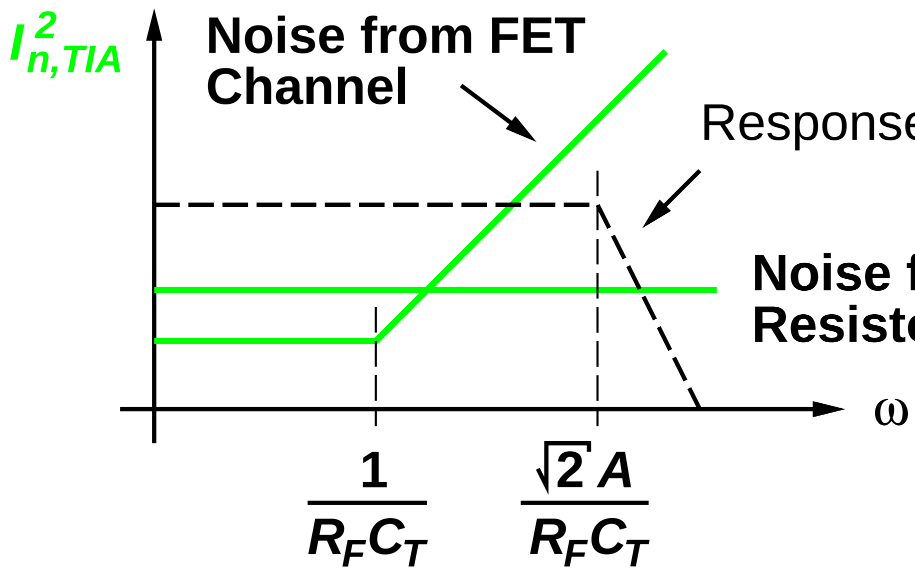


- **Equivalent noise current source of TIA with bipolar front−end:**



TIA Noise Optimization (2)

- **Input−referred noise current spectrum (FET front−end):**



→ **White noise from feedback resistor and gate current**

→ **f^2 noise from FET channel**

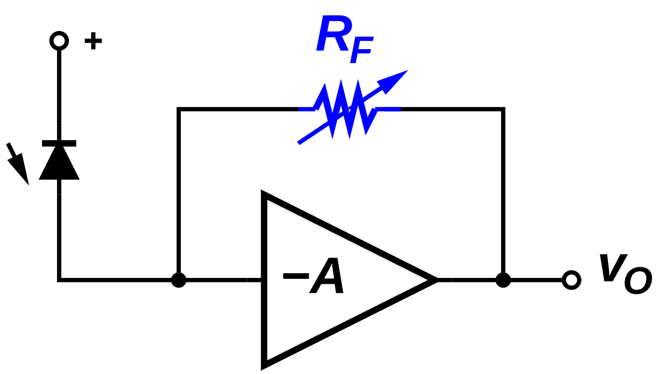
→ **Some of the f^2 noise is passed to the TIA output**

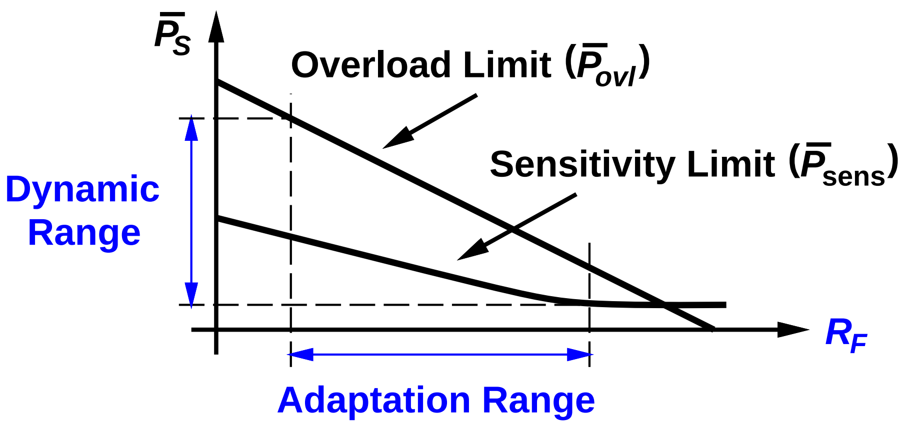
TIA Noise Optimization (3)

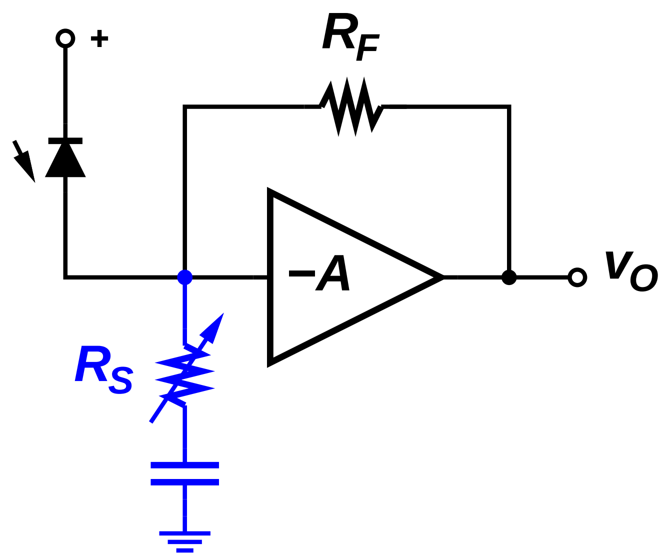
- **TIA noise:** $\overline{i^2_{n,TIA}} = \frac{4kT}{R_F} BW_n + \ldots$

FET front−end	Bipolar front−end
$2qI_G BW_n + \frac{8kT}{3} \frac{(2\pi C_T)^2}{g_m} \frac{BW_{n2}^3}{3} + \ldots$ $\downarrow$ $C_T = C_I + C_D$ $g_m = \omega_T C_I$ smallest for: $C_I = C_D$	$\frac{2qI_C}{\beta} BW_n + 2qI_C \frac{(2\pi C_T)^2}{g_m^2} \frac{BW_{n2}^3}{3} + \ldots$ $\downarrow$ up with I_C $\downarrow$ down with I_C find optimum I_C

Adaptive Transimpedance



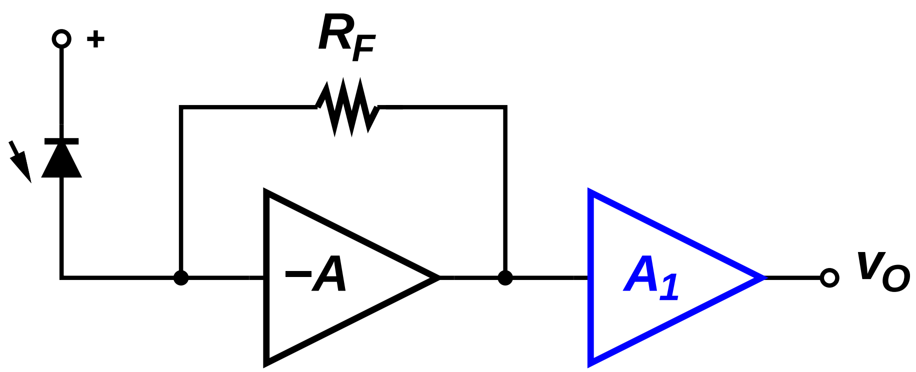




- **Variable feedback:**
  - → **Increase dynamic range**
  - → **Watch stability & peaking!**

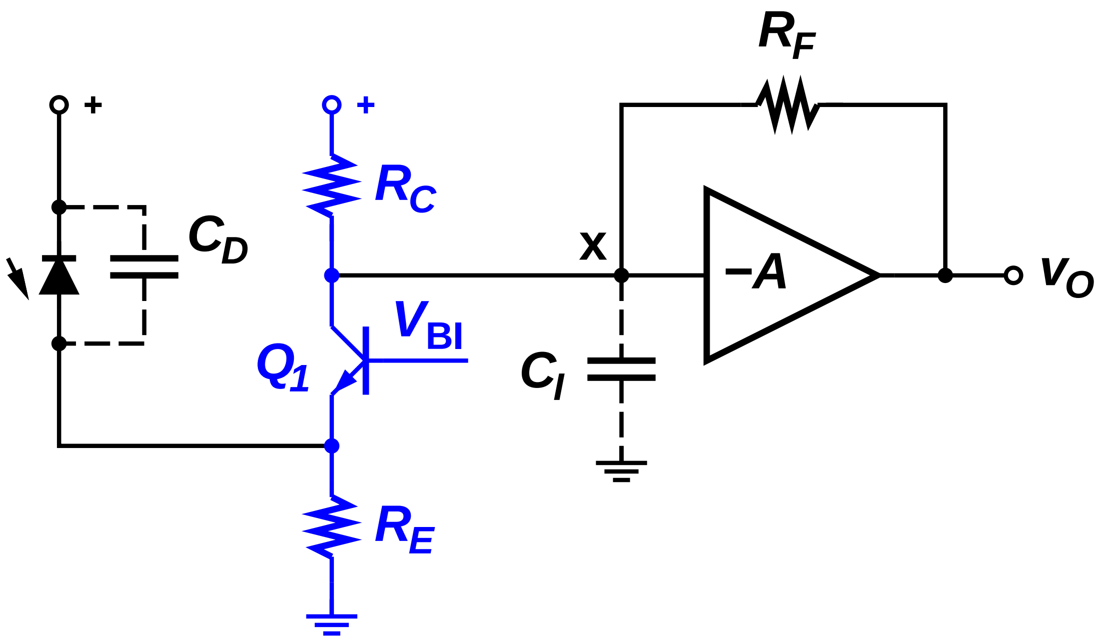
- **Variable input shunt:**
  - → **Increase dynamic range**

Post Amplifier



- **Post amplifier:**
  - ➛ **Boost transimpedance value**
  - ➛ **But make R_F as large as possible to keep noise low**

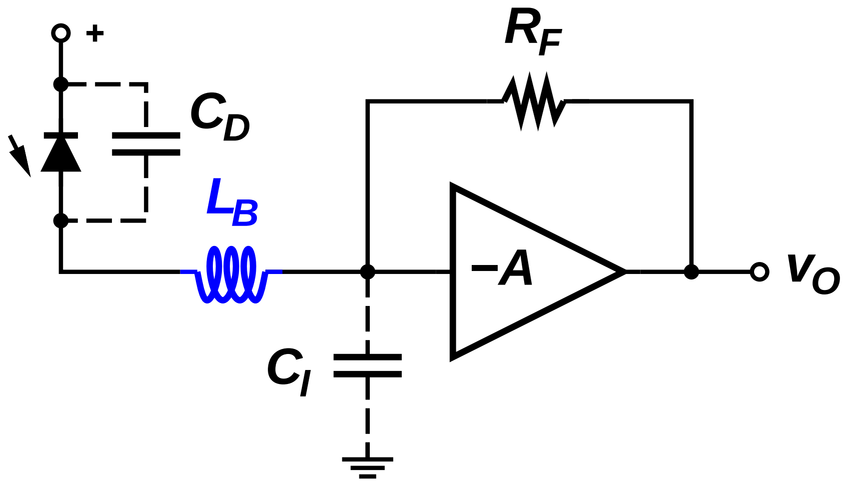
Common−Base/Gate Input Stage



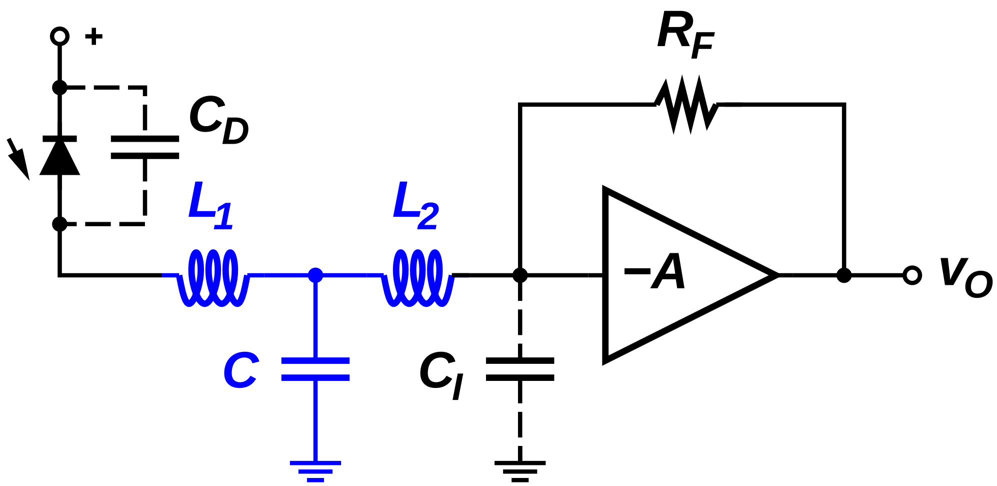
- Common−base (common−gate) input stage:
  - → Photodiode capacitance has less impact on bandwidth
  - → Less capacitance at node x
    - → Higher transimpedance (increase R_F)
    - → Lower noise
  - → But new noise sources: Q_1, R_C, R_E
  - → Higher power dissipation

Inductive Input Coupling

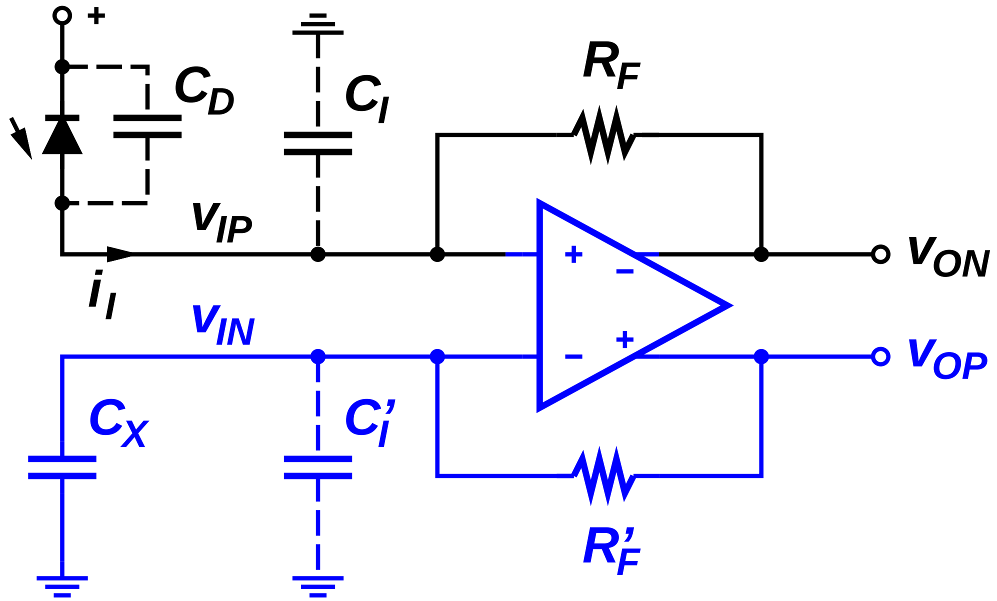
- **Series inductor:**
  - → **Improve bandwidth and noise**
  - → **Use bond wire**



- **L−C low−pass network:**

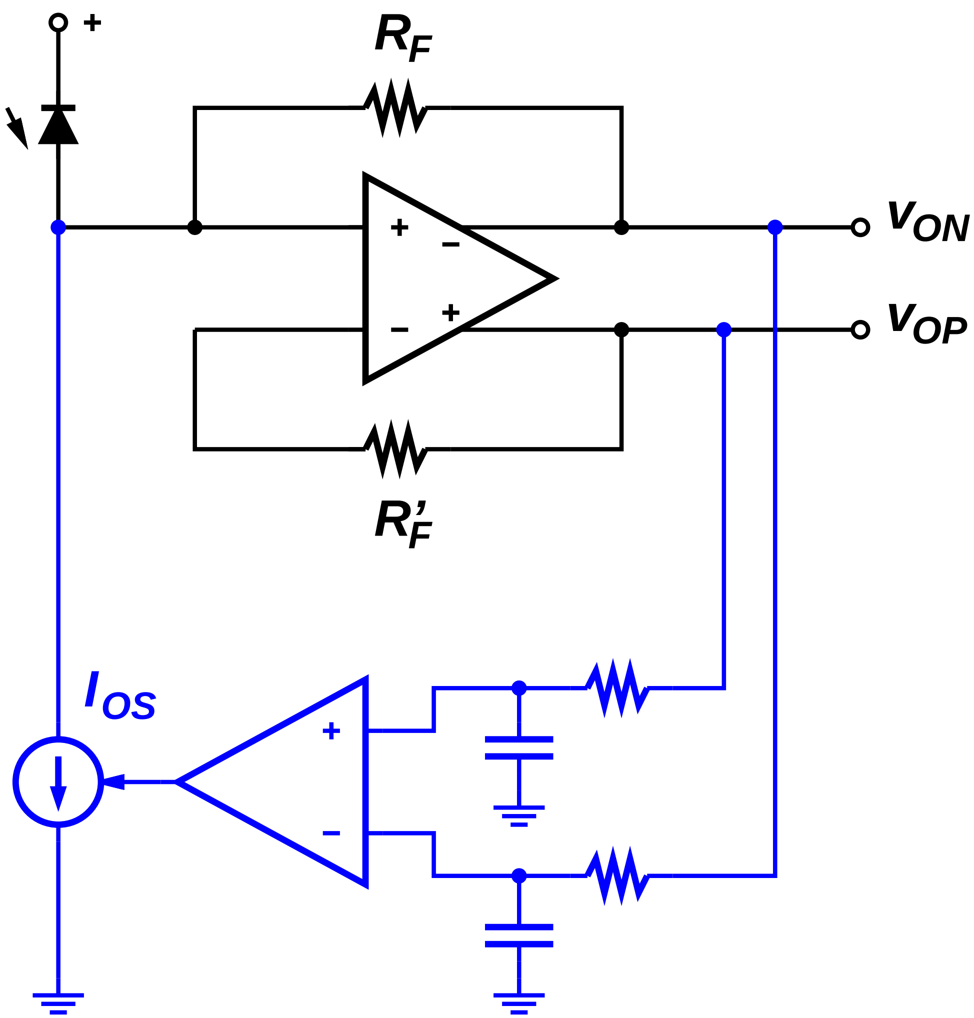


Differential TIA



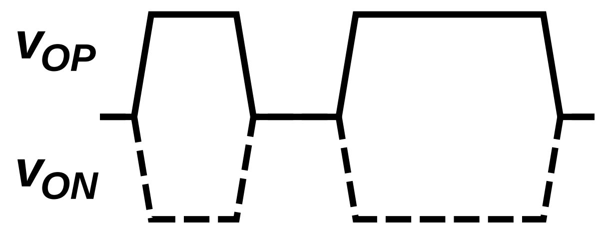
- $C_X = C_D$:
  - → **Differential transimpedance =** R_F
  - → **Fully balanced circuit**
- **Large** C_X:
  - → **Differential transimpedance =** $2R_F$
  - → **Eliminate noise from** R'_F

Offset Control

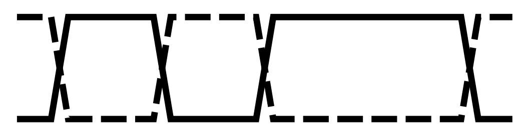


- **Improve output dynamic range:**

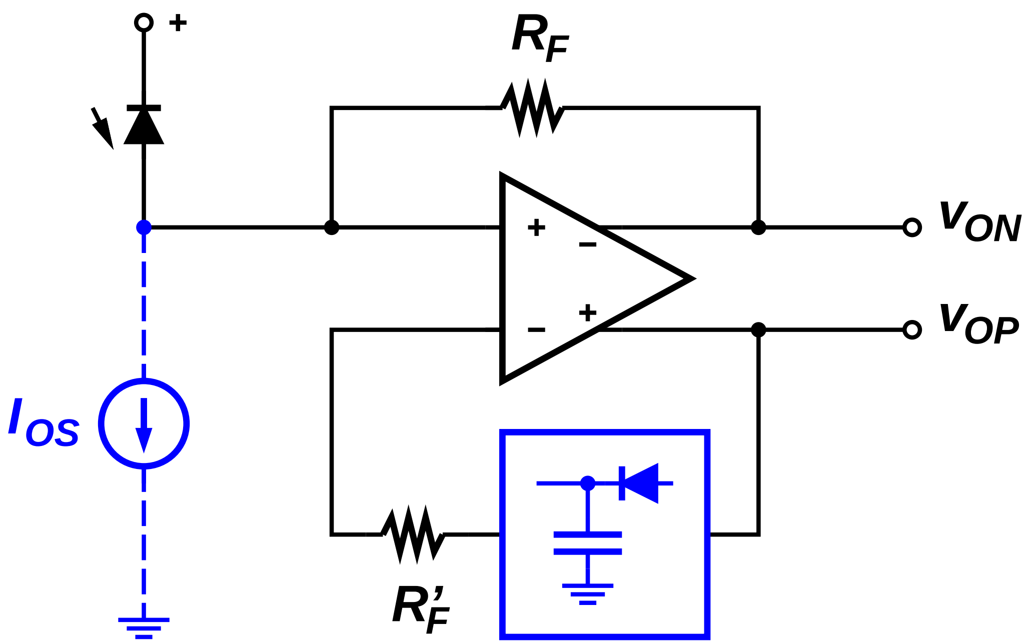
Without offset control:



With offset control:



Burst–Mode TIA



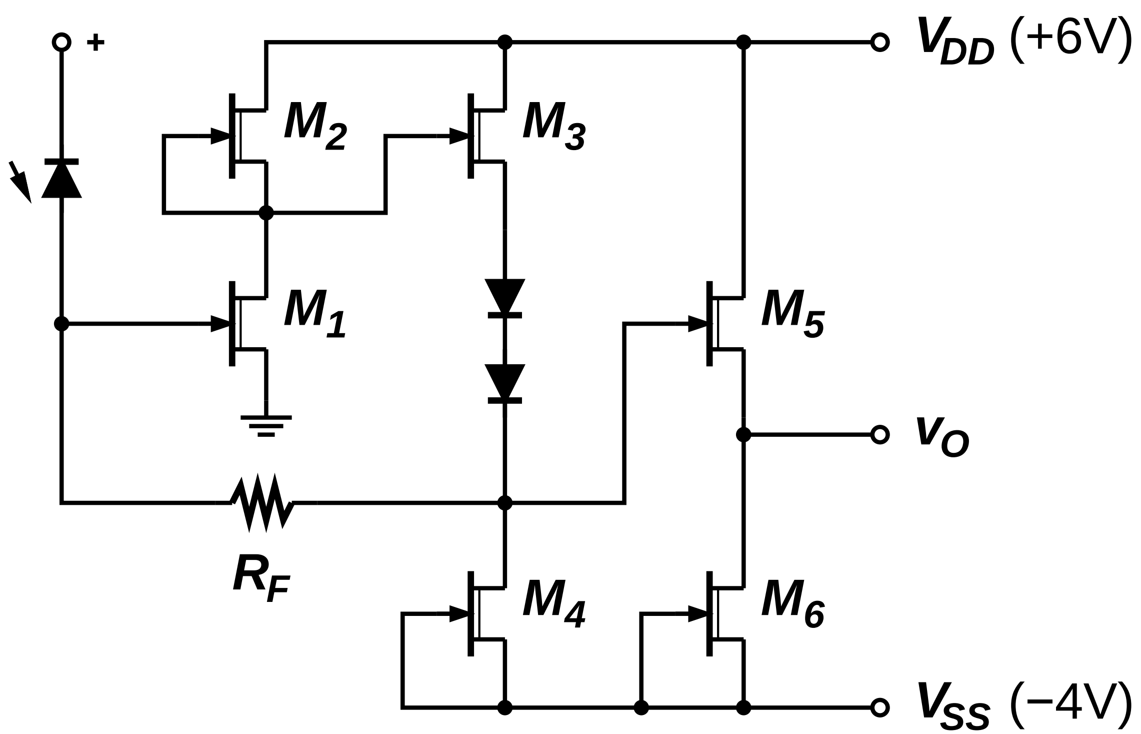
- **Burst amplitude varies up to 30 dB in PON systems**

  ➞ **Set decision threshold (offset) for each burst; reset peak–detector after burst**

- **Suppress "chatter" with small intentional offset**

MESFET, HFET Implementation

- **Single−ended TIA:**

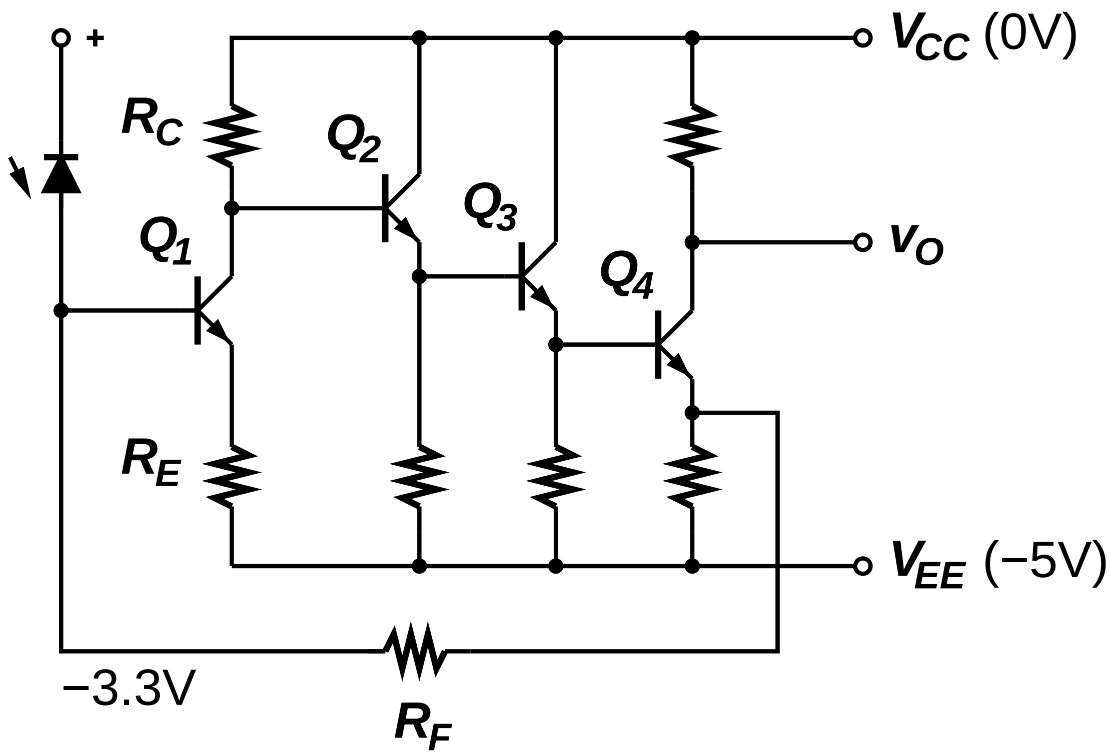


- **Depletion−mode FETs (e.g. GaAs)**

[O. Wada et al. 1985]

BJT, HBT Implementation

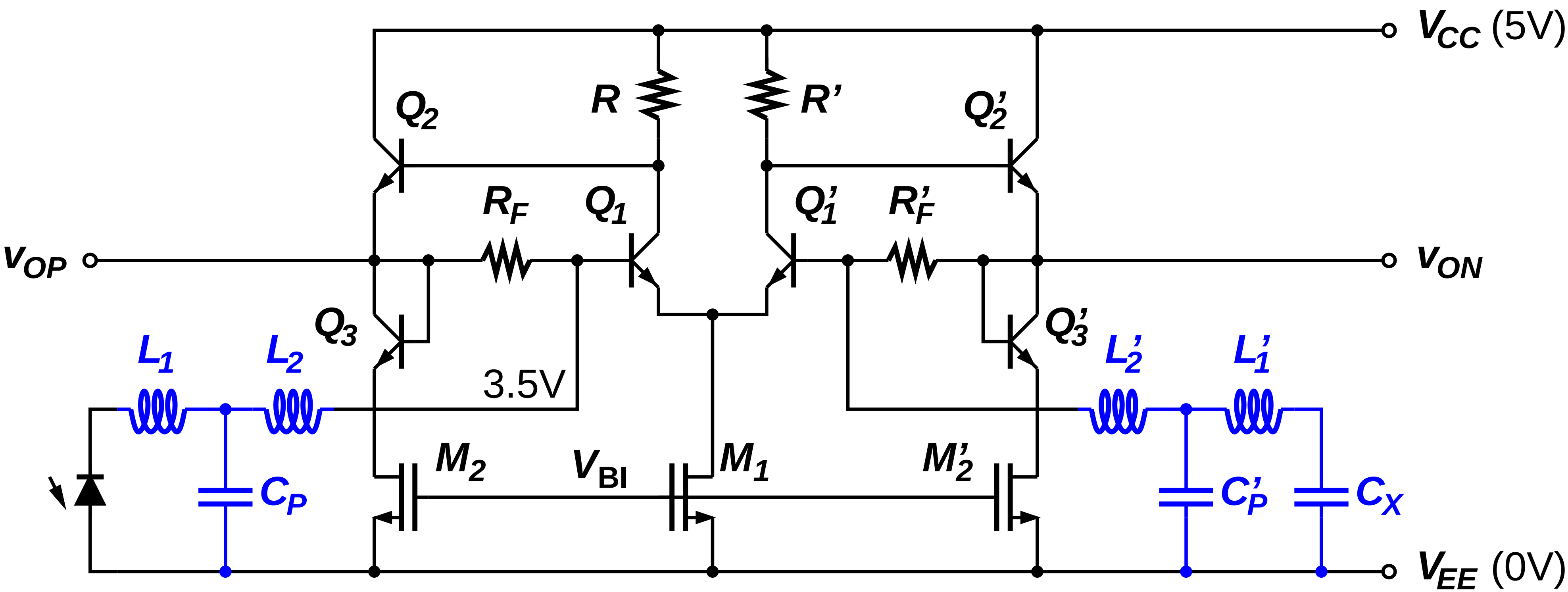
- **Single−ended TIA (core):**



[H. Khorramabadi et al. 1995]

BiCMOS Implementation

- **Differential TIA (core):**

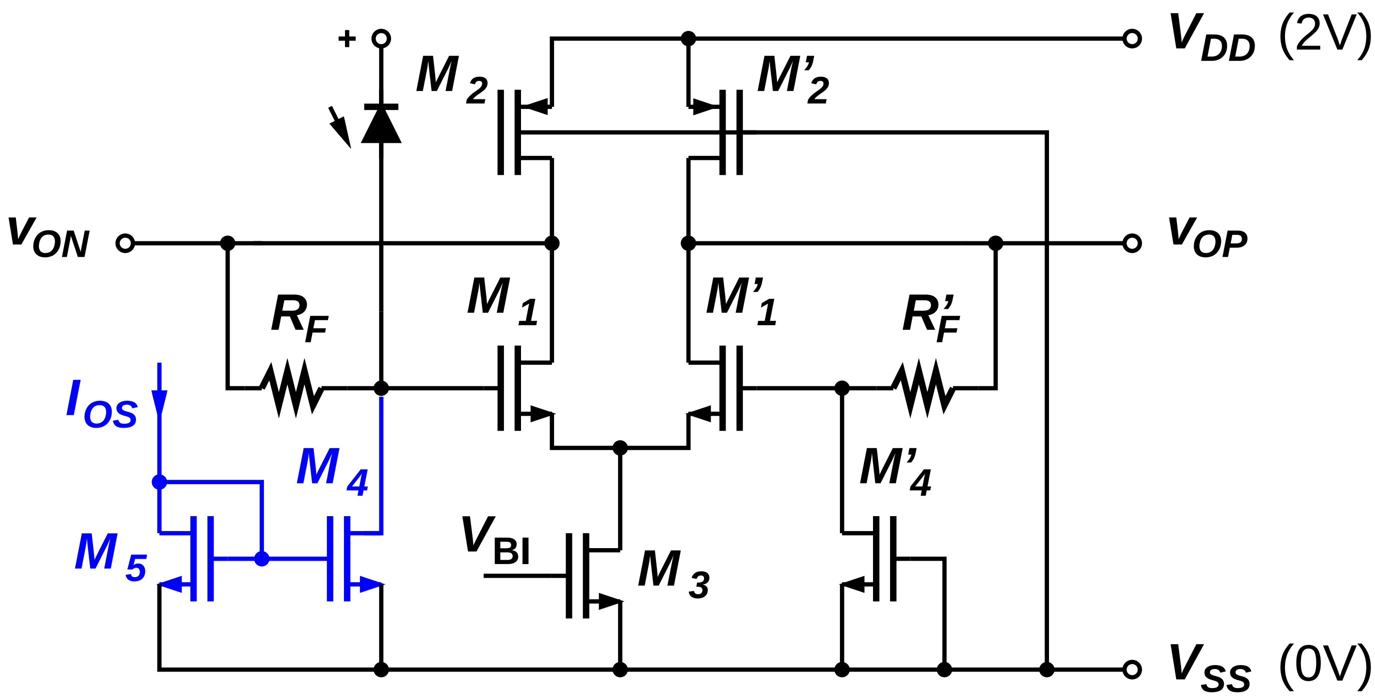


- **BJTs in signal path; MOS for current sources**
- **Inductive input coupling**

[H. Kim et al. 2001]

CMOS Implementation (1)

- **Low−voltage TIA (core):**

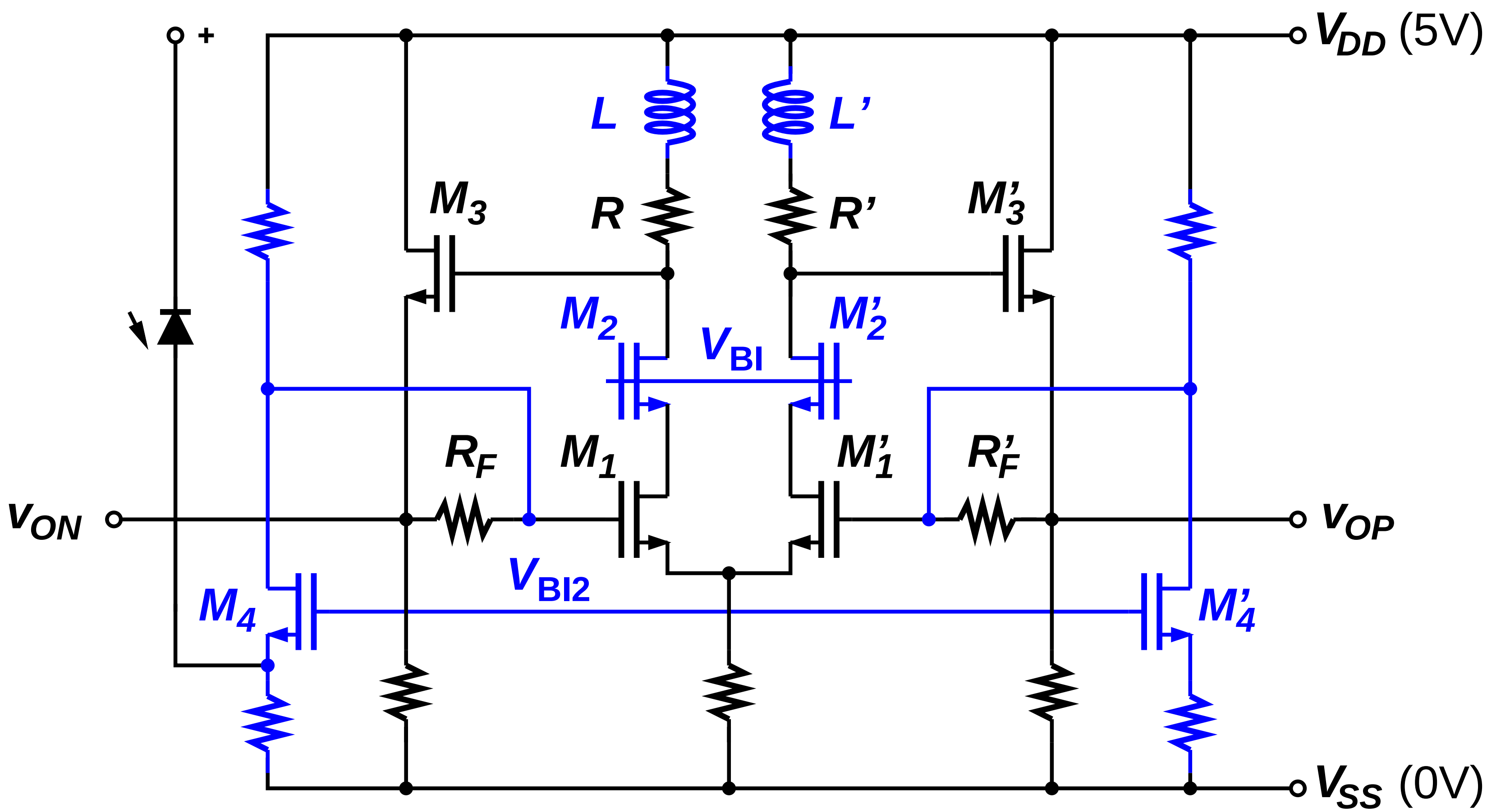


- **p−MOS loads in linear regime**
- **Offset control**

[A. Tanabe et al. 1998]

CMOS Implementation (2)

- **Differential TIA (core):**

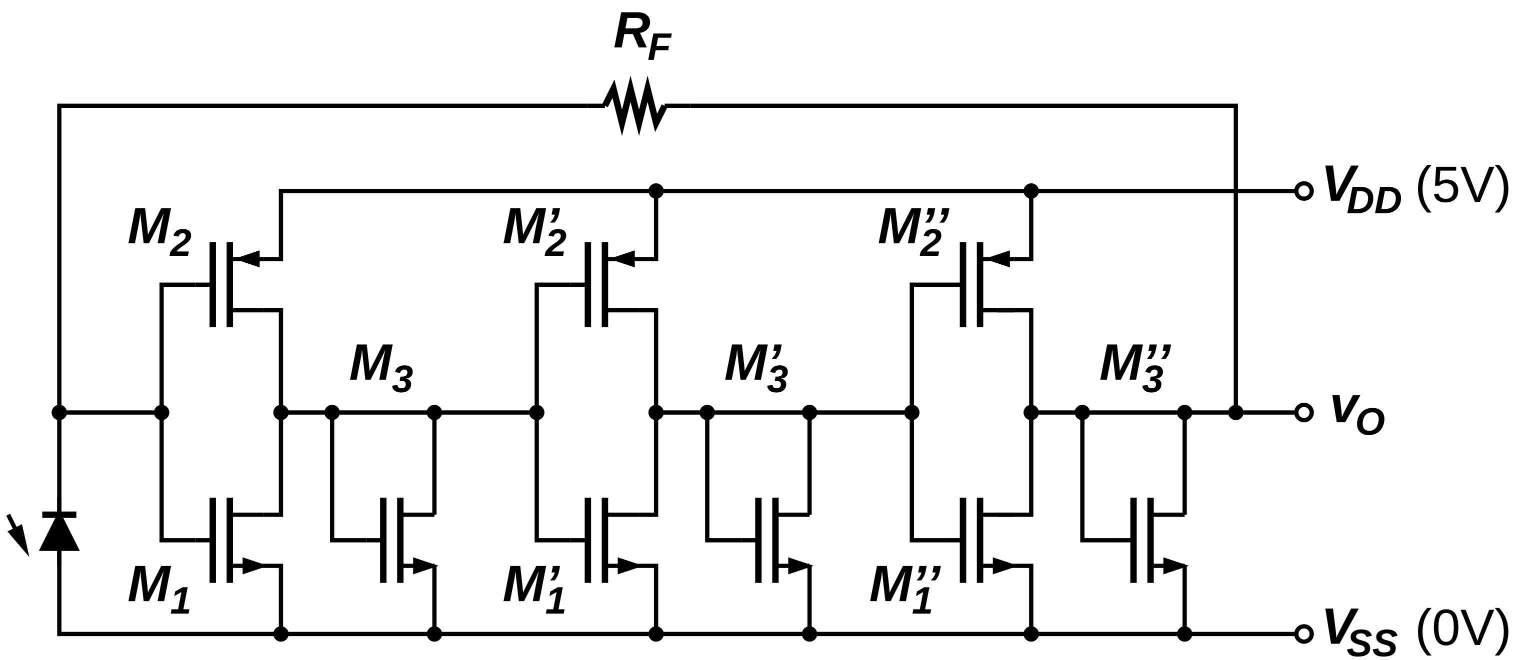


- **Common−gate input stage**
- **Inductive loads (shunt peaking)**
- **Cascode transistors**

[S. Mohan et al. 2000]

CMOS Implementation (3)

- **Single−ended TIA:**



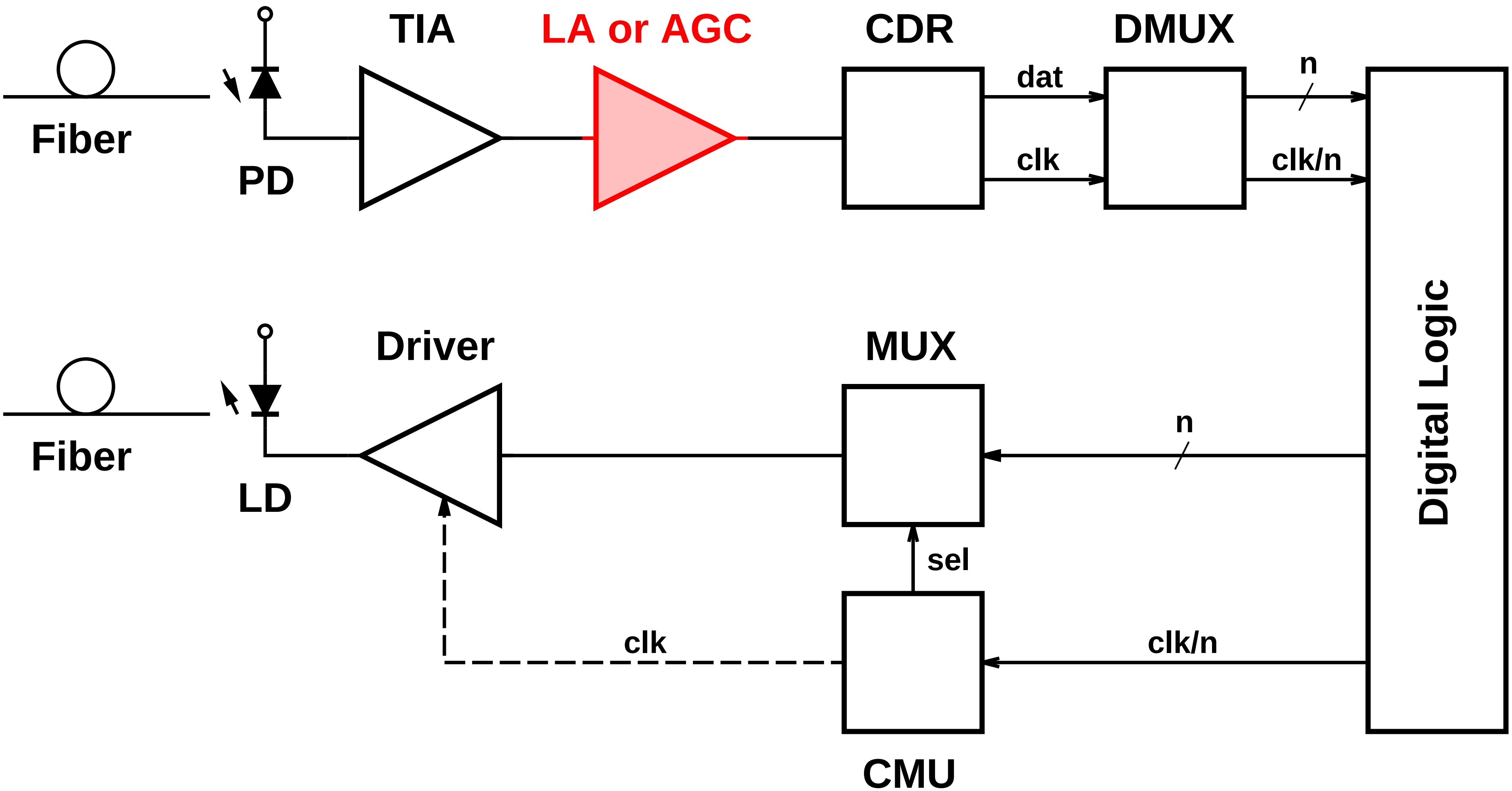
- **Multistage feedback amplifier**
- **Gain determined by transistor geometry**

[M. Ingels et al. 1994]

Research Directions

- Higher speed: 40 Gb/s and beyond
  - Use heterostructure devices (HBTs and HFETs) based on compound semiconductors (SiGe, GaAs, InP)
- Higher integration: OEIC
  - Integrate TIA & InP photodetector for 1.3 ... 1.6−um receivers (monolithic of flip−chip)
  - Integrate TIA & photodetector in silicon for 0.8−um receivers
- Lower cost:
  - Use mainstream technology (CMOS, BiCMOS)
  - TIA as part of a CMOS "system on a chip"
- Lower noise:
  - Eliminate noise of resistor in shunt−feedback TIA (e.g., capacitive or optical feedback)

Main Amplifiers (MA)

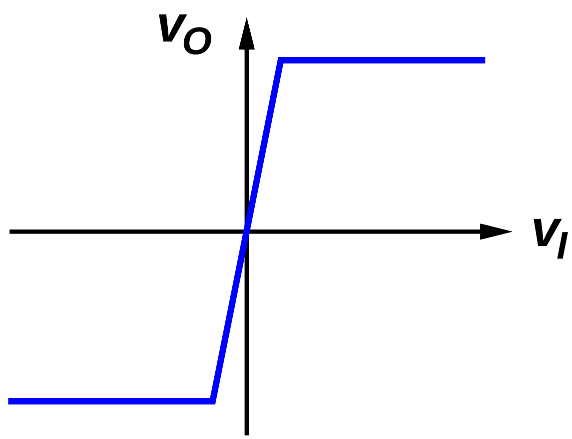


Limiting vs. AGC Amplifiers

Limiting amplifier	Automatic gain control amplifier

Limiting amplifier

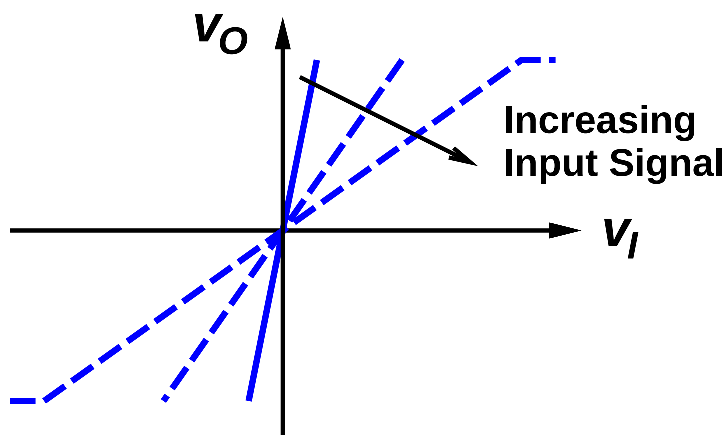
- Nonlinear:



- Drive decision circuit directly
- Easier to design
- Generally, lower power, lower noise, etc.

Automatic gain control amplifier

- Linear:

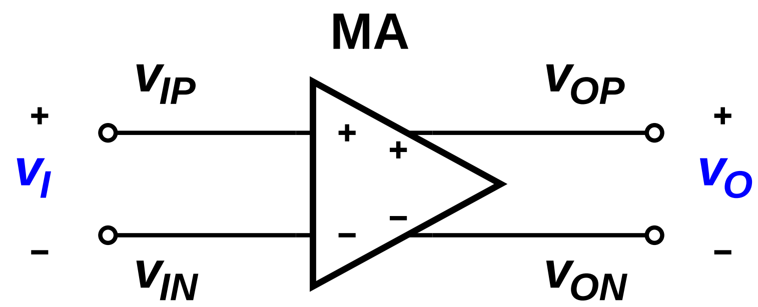


- Signal processing on output signal possible:
  - Equalization
  - Slice−level steering
  - Soft−decision decoding

Voltage Gain

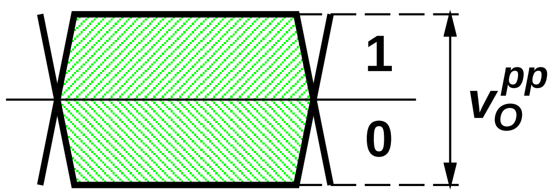
- **Gain definition:**

$$A = \frac{\Delta v_O}{\Delta v_I}$$

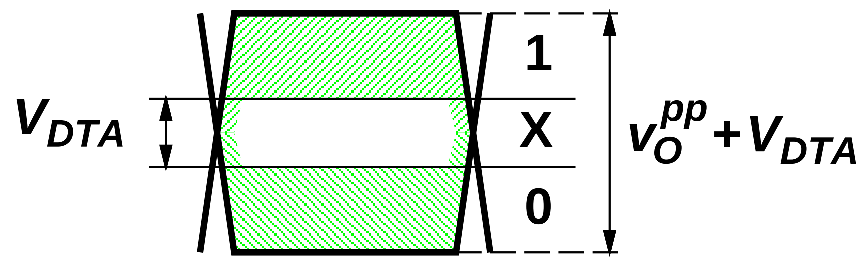


- **Needed gain is given by minimum signal from TIA and minimum signal required by the decision circuit (DEC)**

- **Output signal:**



Ideal DEC



Real DEC

- **Typical value: 30 ... 40 dB**

Bandwidth & Group−Delay Variation

- Make MA bandwidth larger than receiver bandwidth
  → Keep ISI contributed by MA small

- Typical values:
  2.5 Gb/s: BW = 2.5 ... 3 GHz
  10 Gb/s: BW = 10 ... 12 GHz

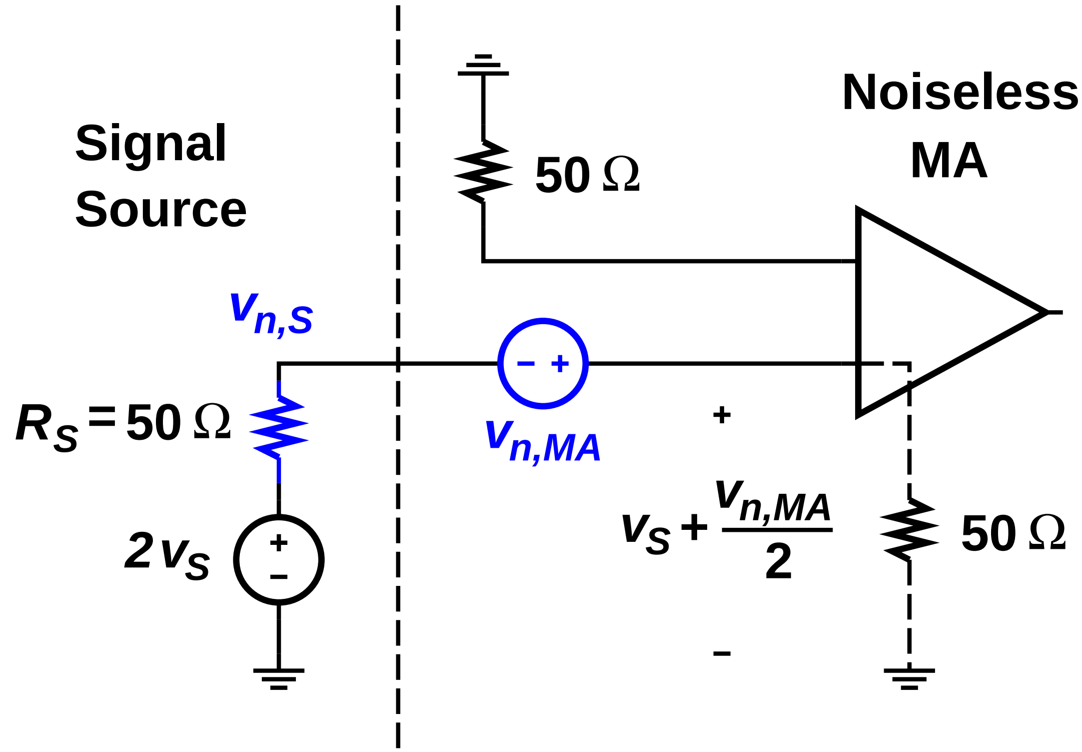
- Group−delay variation (phase linearity) also causes distortions (ISI and jitter)
  → Limit group−delay variations over bandwidth to less than 0.1 UI

- Typical values:
  2.5 Gb/s: $|\Delta\tau| < 40$ ps
  10 Gb/s: $|\Delta\tau| < 10$ ps

Noise Figure

- Noise figure definition (single ended):

$$F = \frac{\overline{v_{n,MA}^2}}{\overline{v_{n,S}^2}}$$



- MA adds noise to the total receiver noise and thus reduces the receiver sensitivity
  → Choose F such that power penalty < 0.05 dB

- Typical values: 2.5 Gb/s: F < 17 dB
  10 Gb/s: F < 13 dB

Input Dynamic Range & Sensitivity

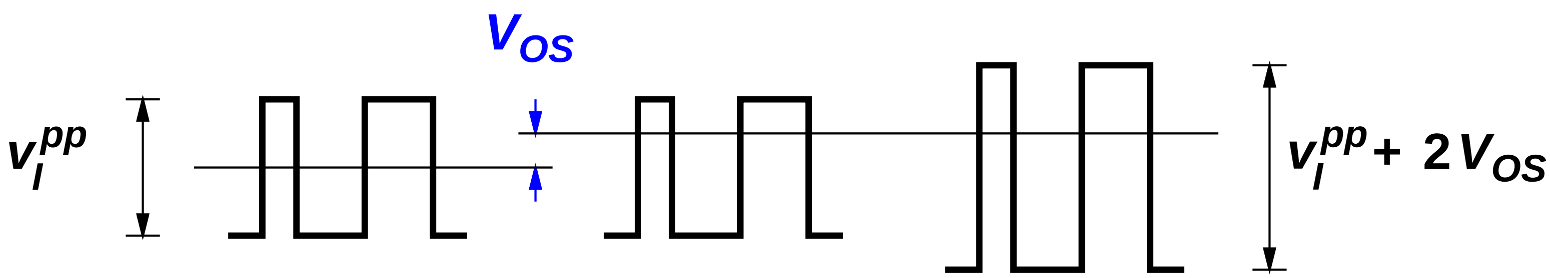
- **Sensitivity:**
  - **Minimum peak−to−peak input voltage signal necessary to achieve a specified bit−error rate:**

    $$v_{\mathrm{sens}}^{pp} = Q\, v_{n,MA}^{rms}$$

  - **Typical value: 2 mV$_{\mathrm{pp}}$**

- **Input dynamic range:**
  - **Low end = sensitivity**
  - **High end @ AGC amplifier = maximum signal before nonlinear distortions become harmful (e.g., 1−dB gain compr.)**
    @ LA = maximum signal before pulse−width distortion and jitter degrade BER
  - **Typical value: 2 mV$_{\mathrm{pp}}$ ... 2 V$_{\mathrm{pp}}$**

Input Offset Voltage



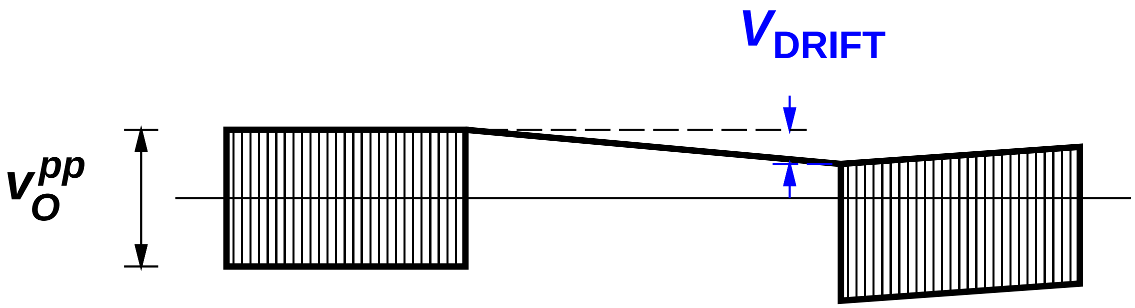
Without offset | **With offset** | **With offset and increased signal to restore BER**

- **In the presence of an offset voltage, nonoptimal slicing requires a larger input signal to meet a given BER**
  Thus, the receiver sensitivity is reduced

  → **Limit offset voltage such that power penalty < 0.05dB**

- **Typical value: V_{OS} < 0.1 mV**

Low−Frequency Cutoff



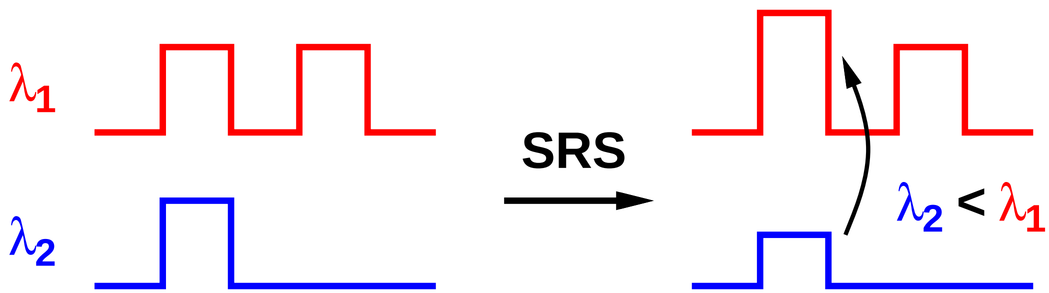
- For long strings of zeros or ones, the output signal drifts (if f_{LF} > 0 Hz) resulting in nonoptimal slicing (like offset)

  → Choose f_{LF} such that power penalty < 0.05 dB for 72 consecutive ones or zeros (SONET)

- Typical values (CID = 72, PP < 0.05 dB):

  2.5 Gb/s: f_{LF} < 60 kHz
  10 Gb/s: f_{LF} < 260 kHz
  (in practice, often lower)

AM−to−PM Conversion



- The received signal may contain amplitude variations, e.g., due to stimulated Raman scattering (SRS) in a WDM system

- The main amplifier (in particular an LA) may convert these variations (AM) into jitter (PM)

  → Limit delay variation over dynamic range to less than 0.1 UI

- Typical values:

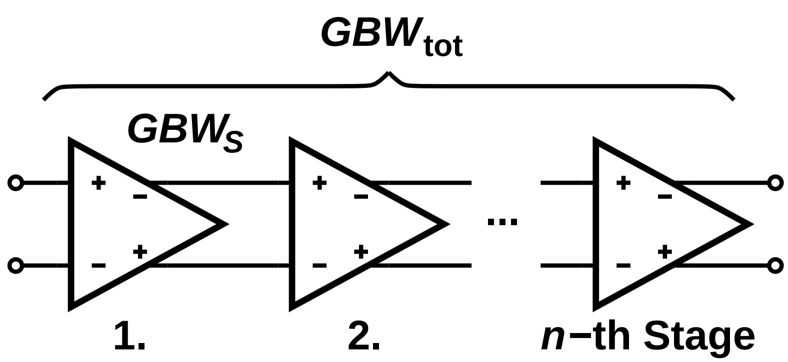
  2.5 Gb/s: $|\Delta\tau| < 40$ ps

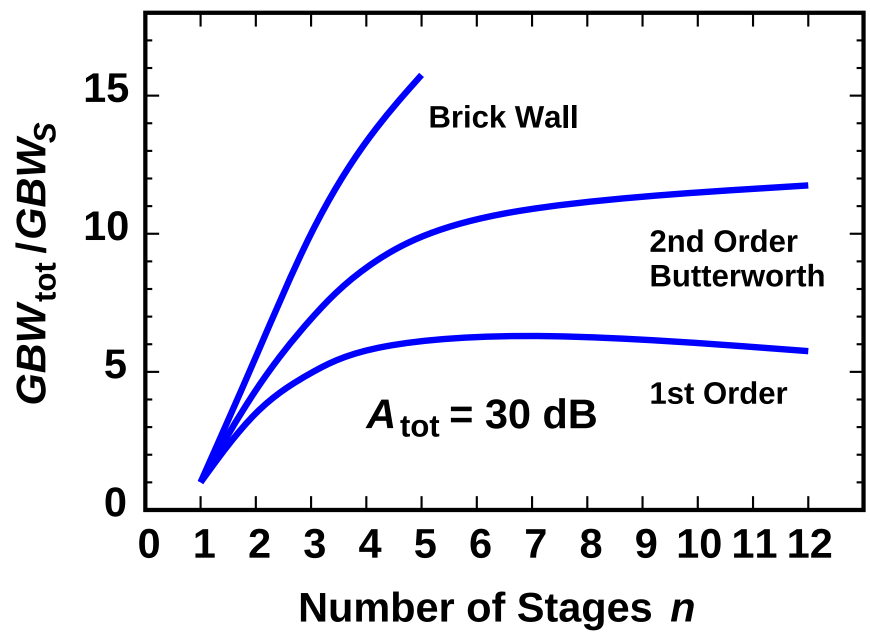
  10 Gb/s: $|\Delta\tau| < 10$ ps

Multistage Amplifier

- The gain−bandwidth product (GBW) required for the MA is often much higher than the f_T of the technology!
- Typical values:
  2.5 Gb/s: GBW = 100 GHz
  10 Gb/s: GBW = 400 GHz

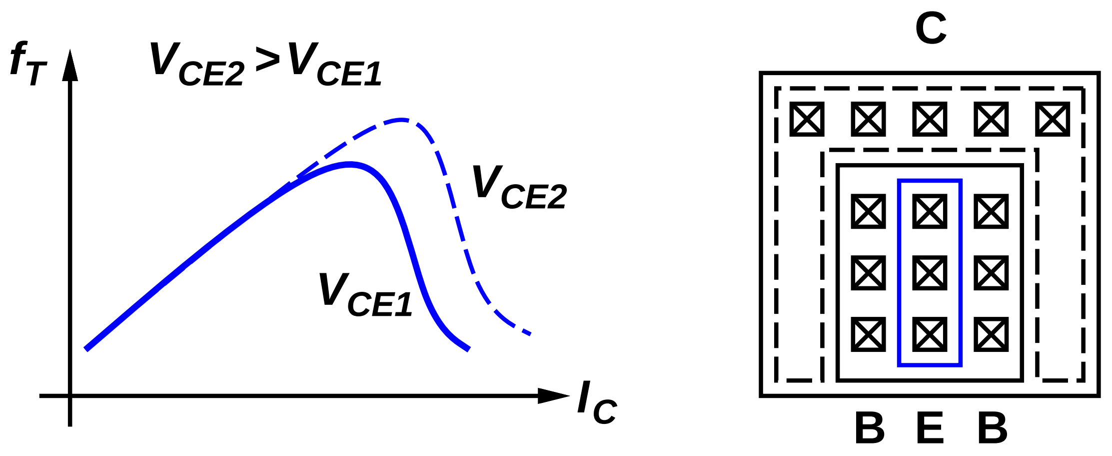
→ Use multistage amplifier:



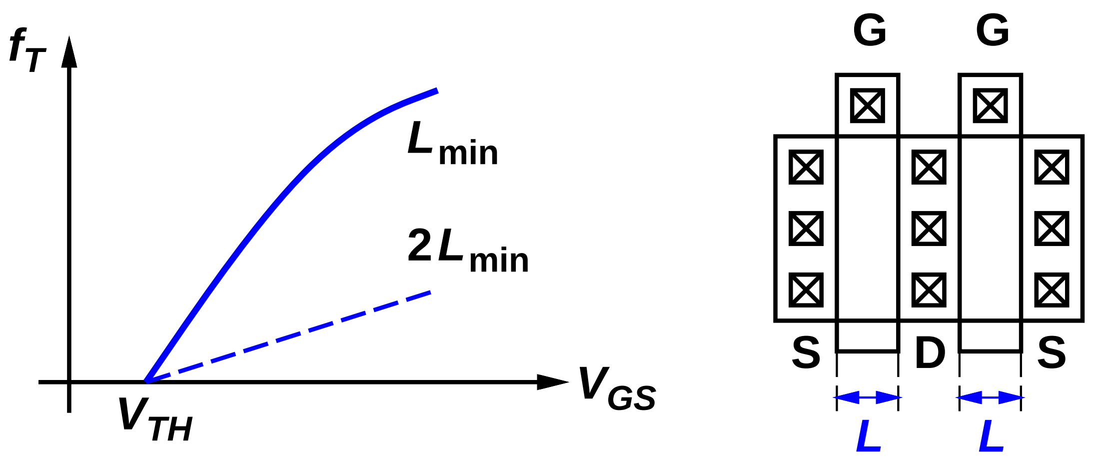


Broadband Stages (1)

- Use fast transistors (f_T, f_{max})
  - ➛ BJT: optimize emitter area; use large collector−emitter voltage

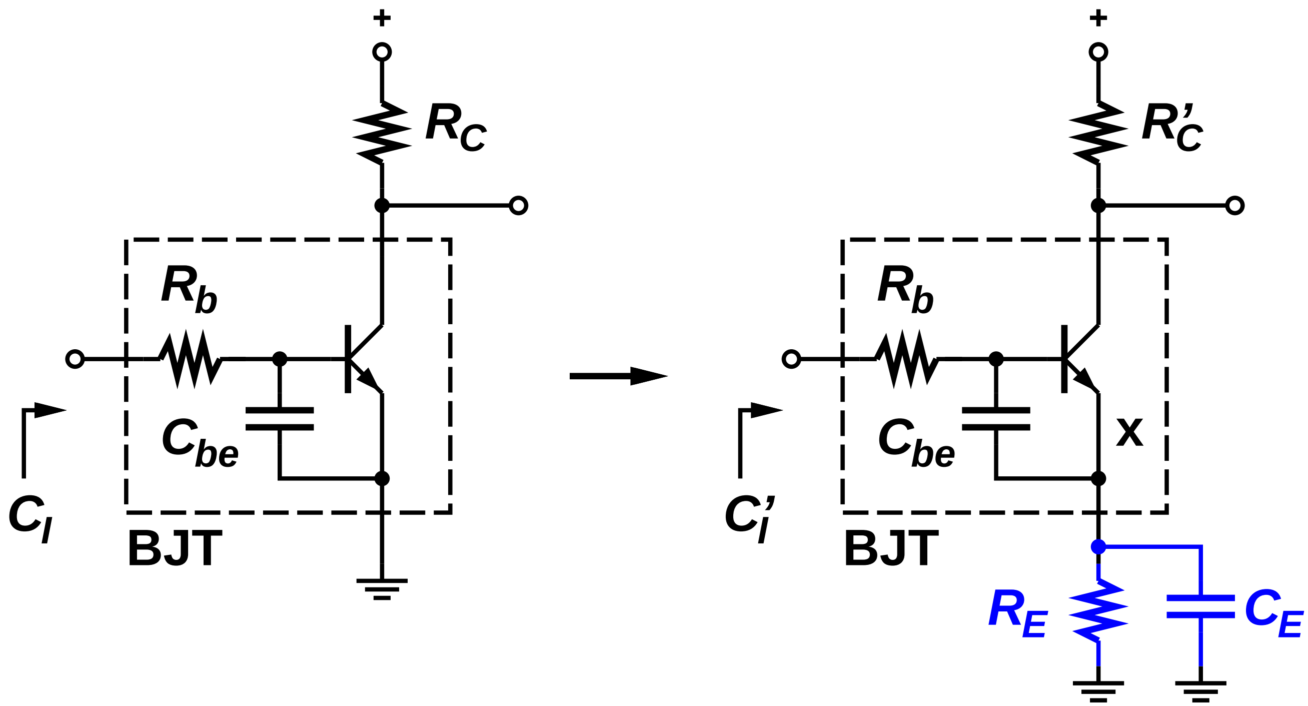


  - ➛ MOS: use minimum gate length; use large gate−source voltage



Broadband Stages (2)

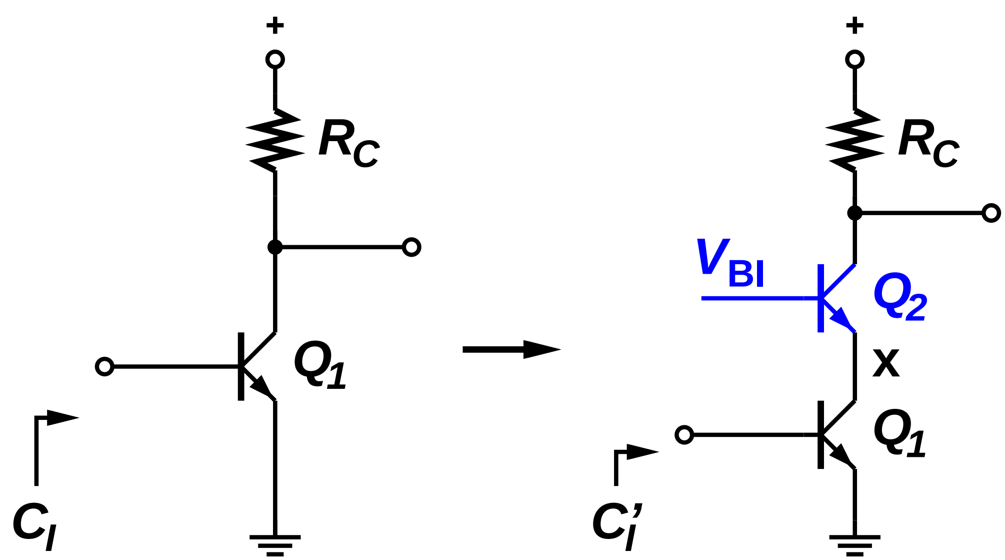
- Use emitter degeneration (series feedback)
  - → Speeds up input pole of BJTs



$$R_b C_{be} \rightarrow \frac{R_b C_{be}}{g_m R_E + 1}$$

Broadband Stages (3)

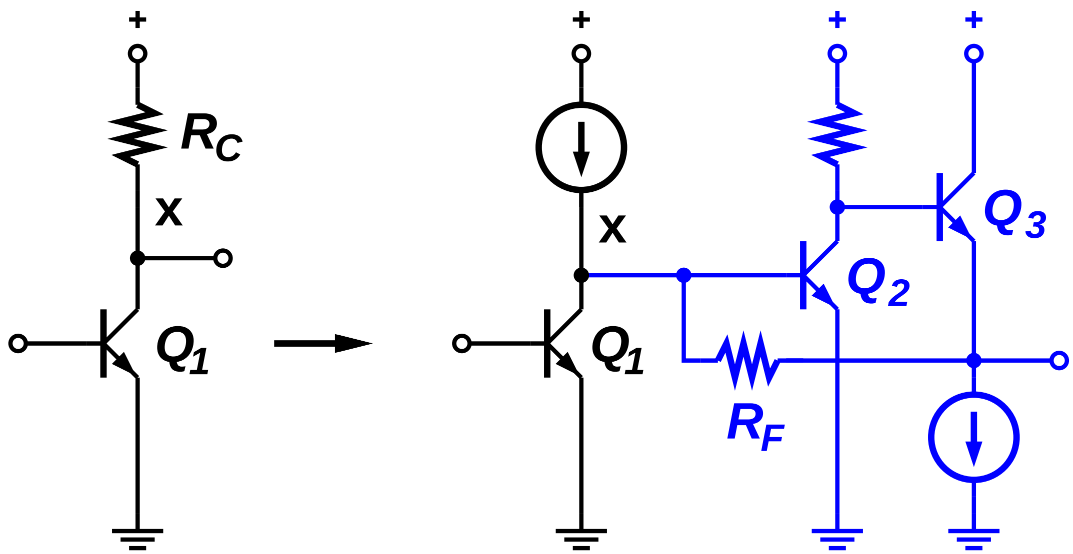
- **Cascoding**
  - ➞ **Suppress Miller capacitance**
  - ➞ **Improve isolation from output to input**



Without cascode **With cascode**

Broadband Stages (4)

- **Transimpedance load (Cherry−Hooper load)**
  - ➛ **Suppress capacitance at node x**
  - ➛ **Suppress Miller capacitance**

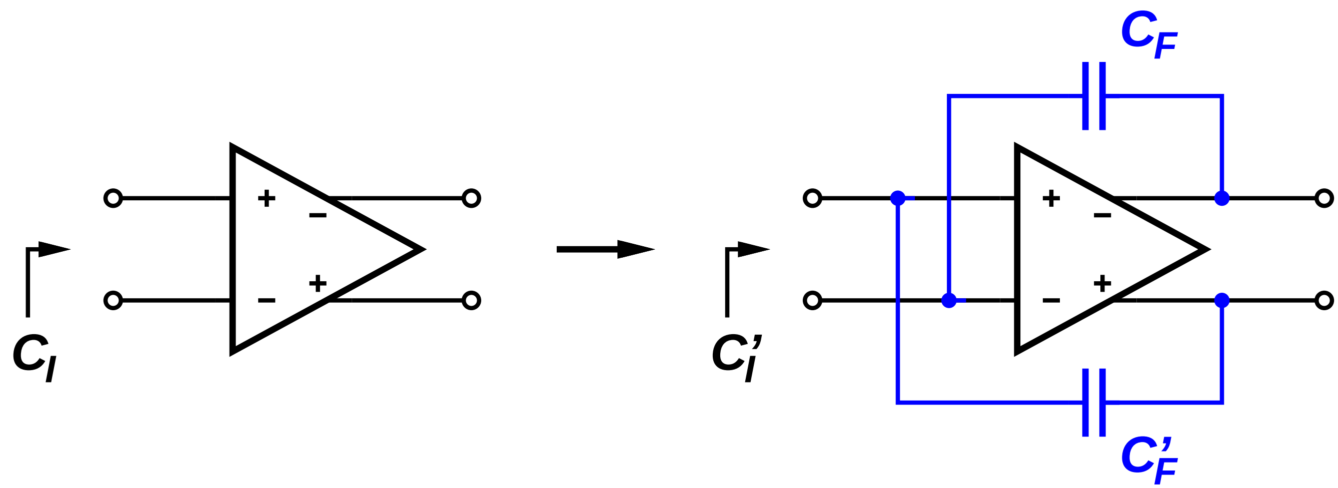


Resistive load **TIA load**

E. Säckinger, "Broadband Circuits for Optical Fiber Communication," John Wiley & Sons, 2005.

Broadband Stages (5)

- **Negative Miller capacitance**
  - ➛ **Cancel Miller capacitance (neutralization)**
  - ➛ **Reduce input capacitance**



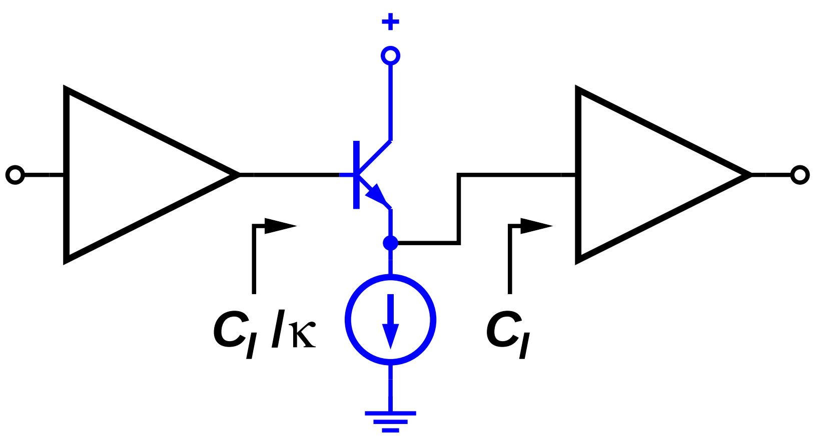
$$C_I' = C_I + (-|A| + 1)\, C_F$$

- **Alternative: invert regular (positive) capacitance with negative impedance converter (NIC)**

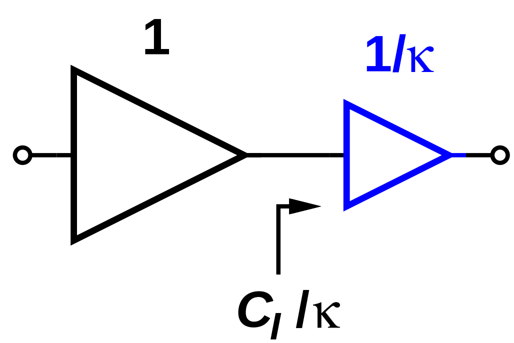
Broadband Stages (6)

- **Buffering or inverse scaling**
  - → **Reduce capacitive loading by next stage**
  - → **Buffer: shift DC level to boost V_{CE} of next stage**

Buffering:



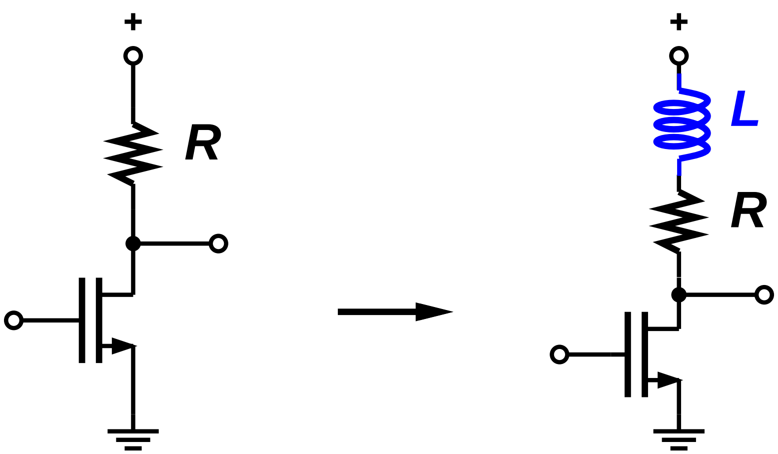
Inverse scaling:

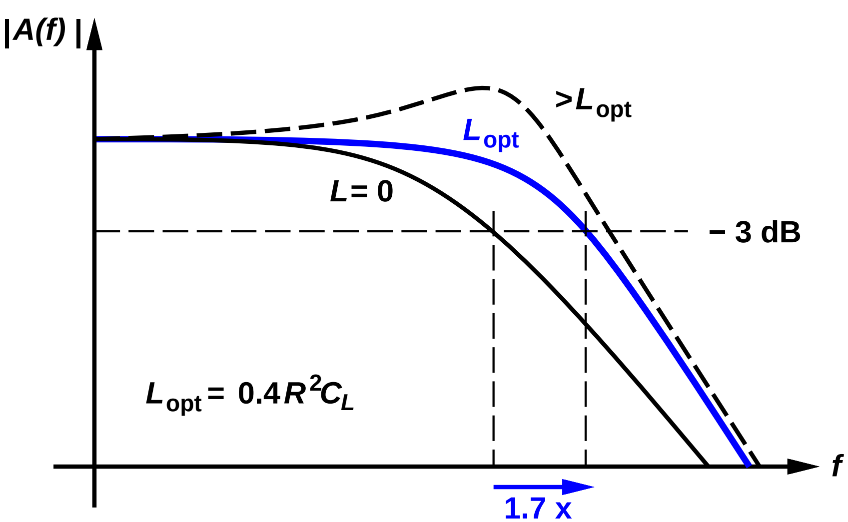


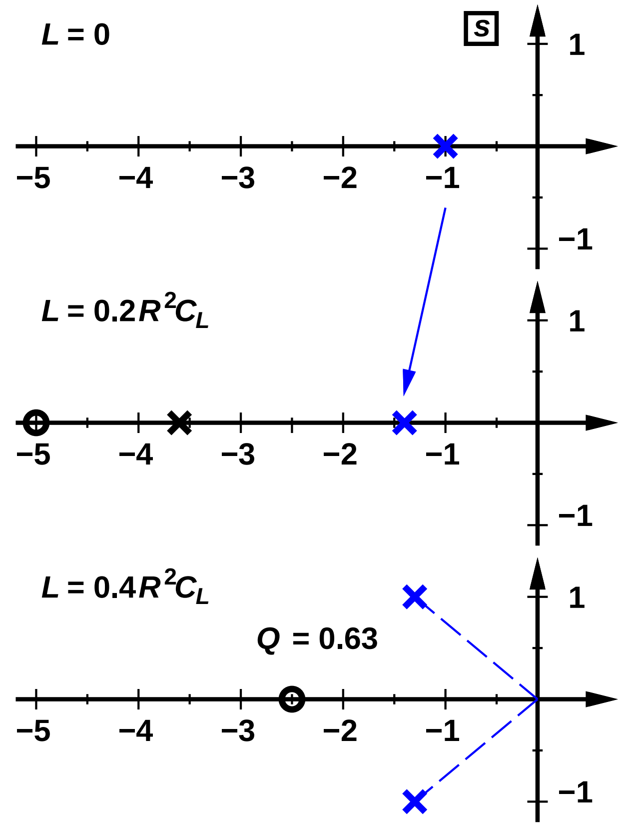
$$C_l' = C_l/\kappa$$

Broadband Stages (7)

- **Shunt peaking (inductive load)**
  - → **Tune out load capacitance with inductor(s)**

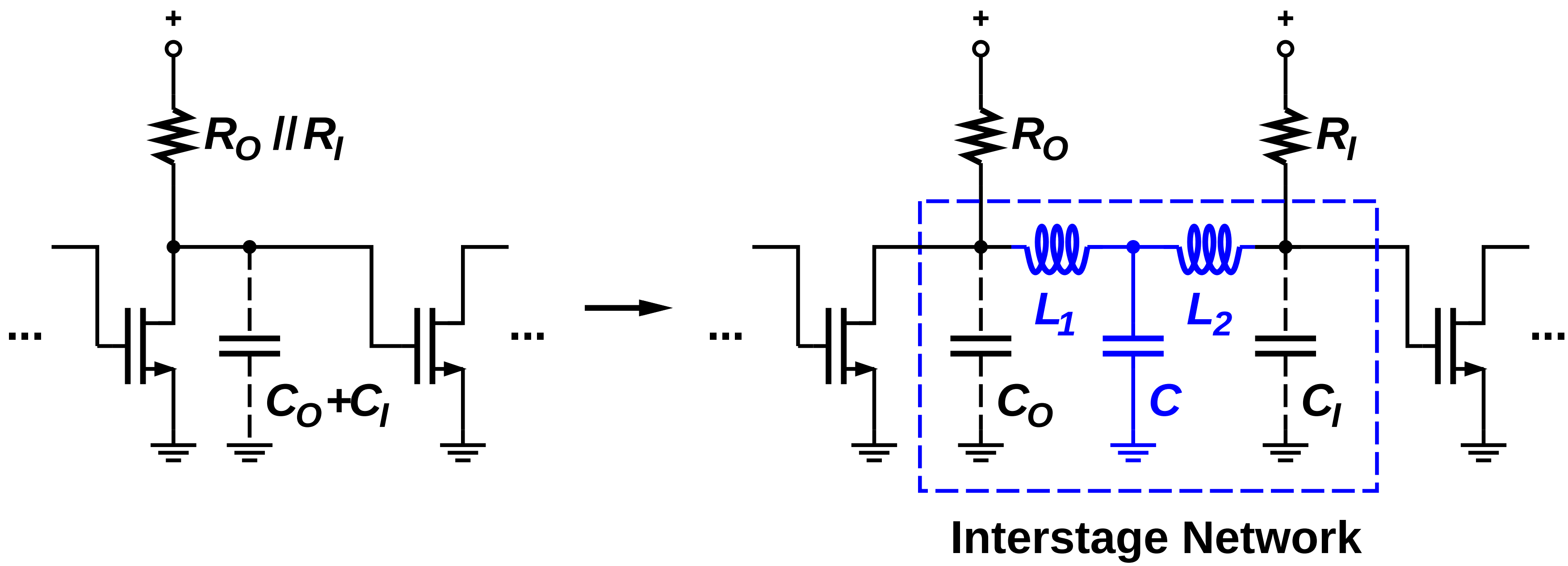






Broadband Stages (8)

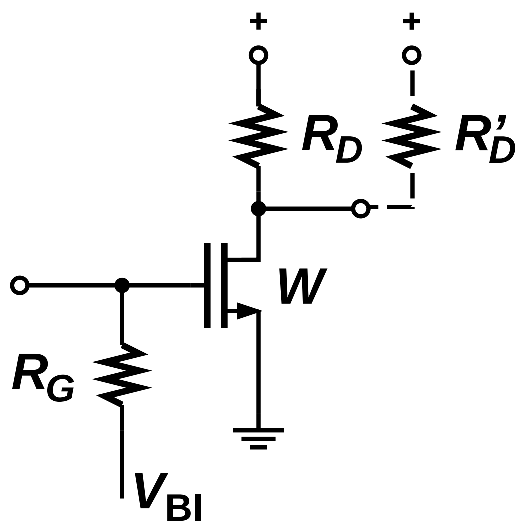
- **Inductive interstage network**
  - ➜ **Absorb input/output capacitances into coupling network**



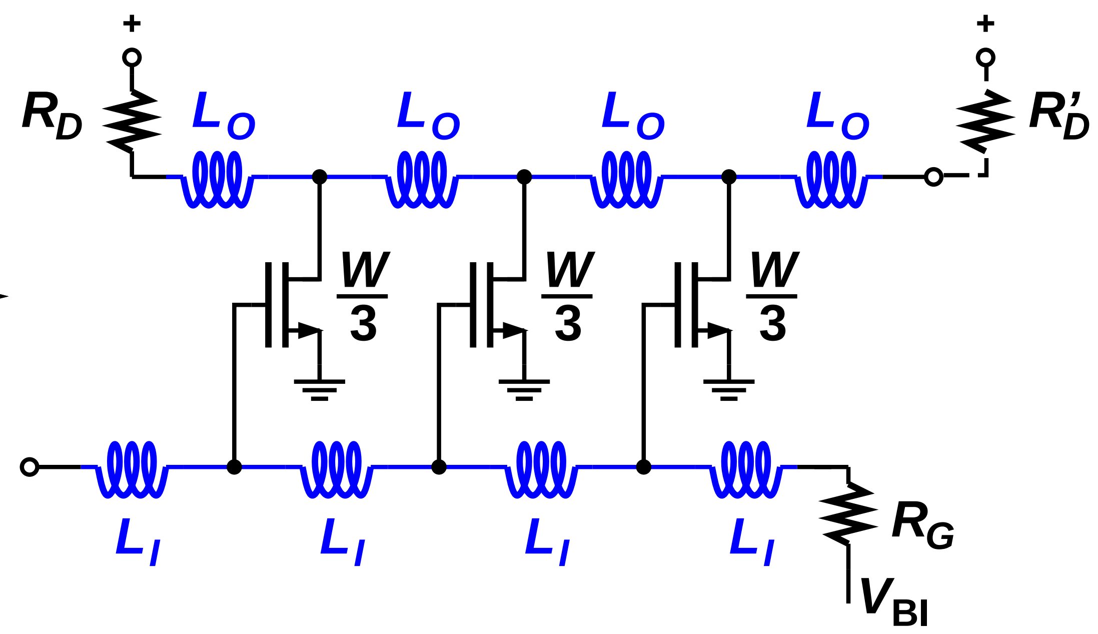
- **Examples:**
  - **Series peaking**
  - **T−coil network**

Broadband Stages (9)

- **Distributed amplifier**
  - ➞ **Absorb input/output capacitances into artificial transmission lines**

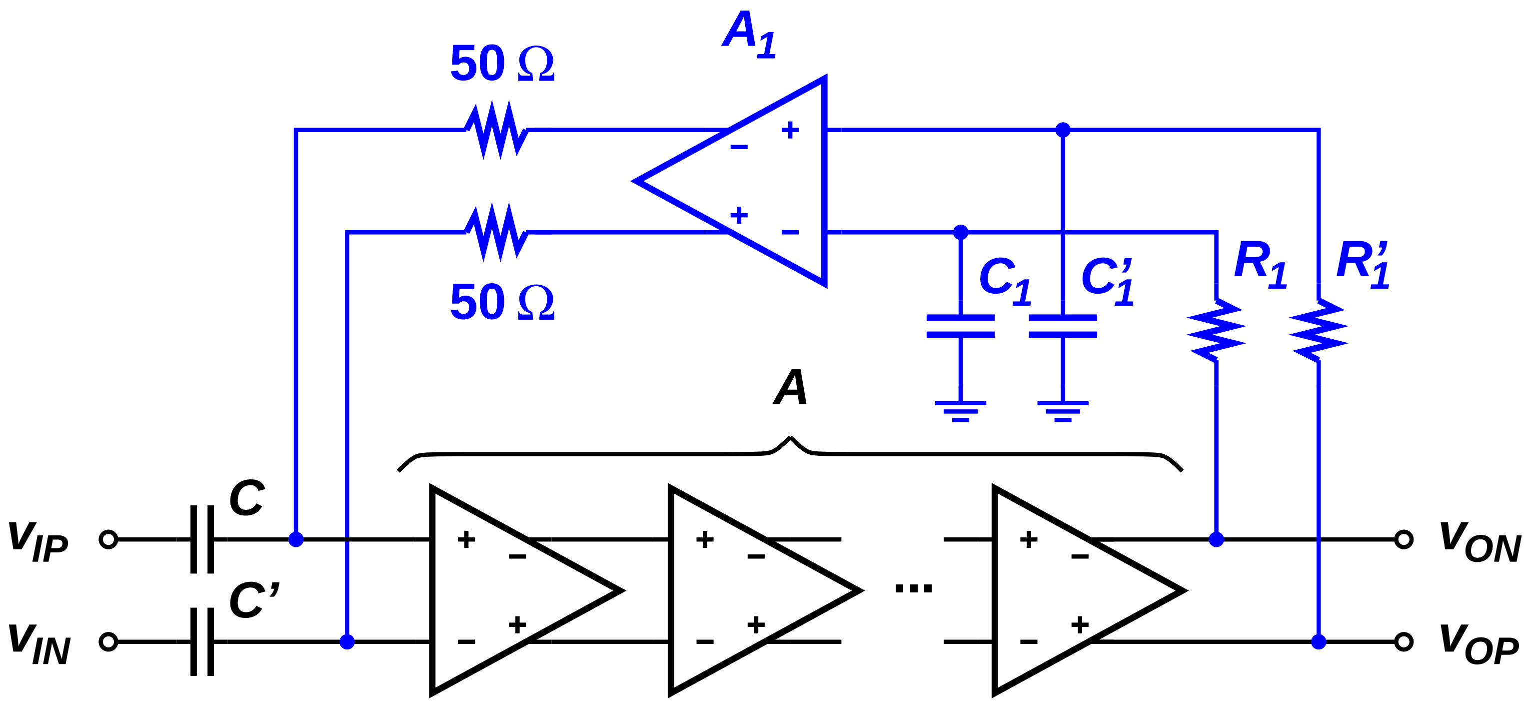


Lumped amplifier



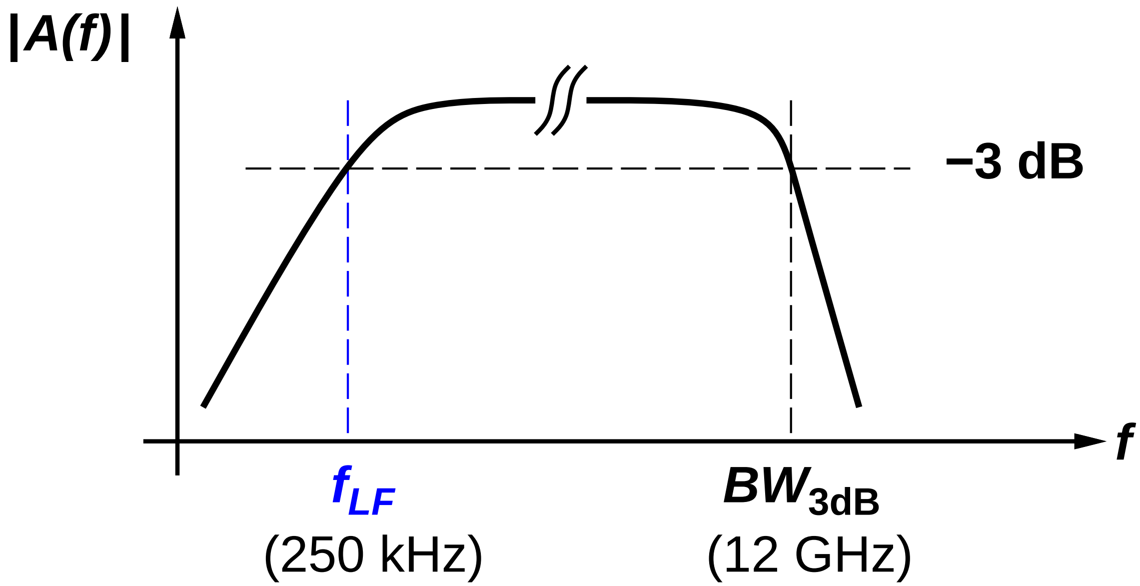
Distributed amplifier

Offset Compensation (1)



- **Reduces offset of main amplifier:** $V_{OS} \rightarrow \dfrac{V_{OS}}{A A_1 + 1}$
- **For BJT amplifiers, usually $A_1 = 1$ (buffer only)**
- **For MOS amplifiers, additional loop gain is needed to compensate the larger offset**

Offset Compensation (2)



- **Offset compensation also suppresses low frequencies!**

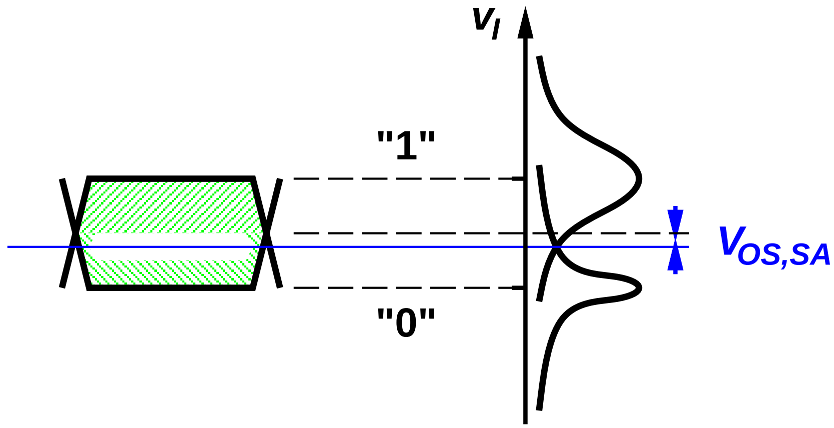
➛ **Low−frequency cutoff:**

$$f_{LF} = \frac{1}{2\pi} \frac{A A_1 / 2 + 1}{R_1 C_1}$$

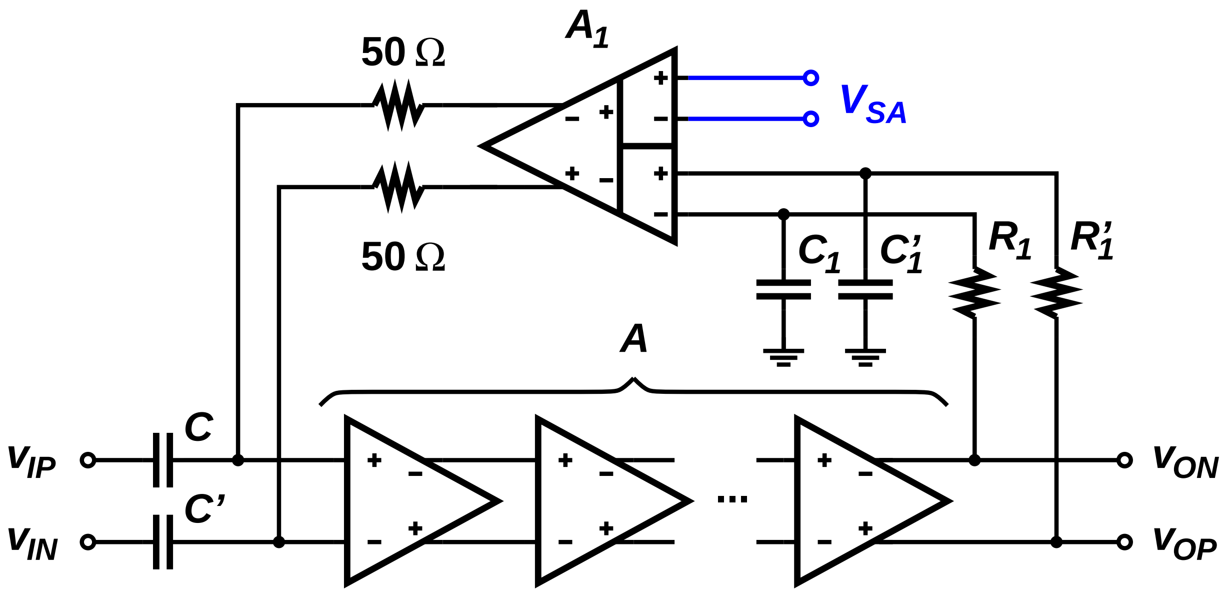
➛ **Very small loop bandwidth required (e.g., 1 kHz)**

Slice−Level Adjustment

- **Receiver with APD or optical preamplifier produces more noise on ones than zeros:**

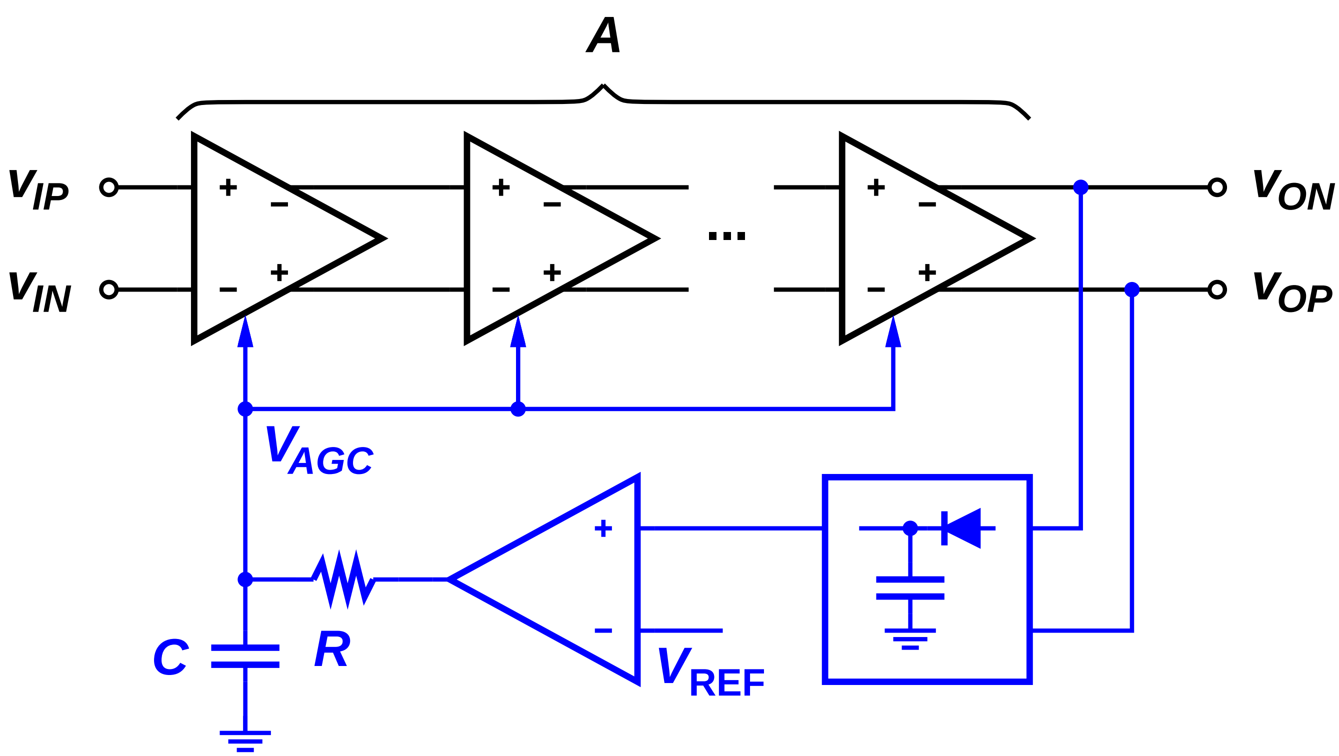


→ **Introduce controlled amount of offset in MA to optimize slice level**



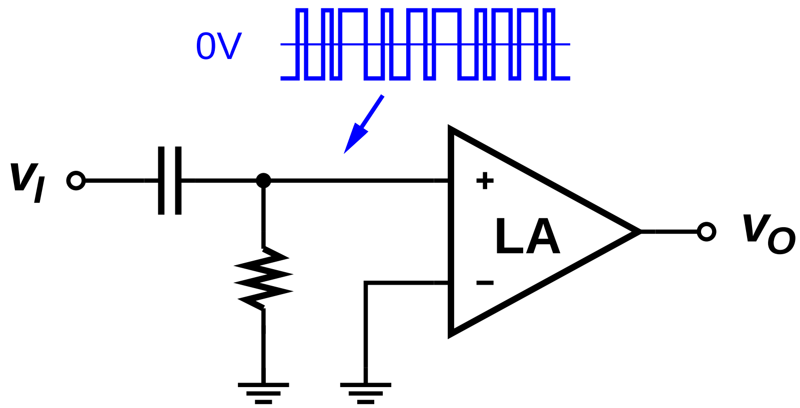
Automatic Gain Control (AGC)

- **The AGC amplifier consist of:**
  - **Variable gain amplifier (VGA)**
  - **Automatic gain control (AGC) loop:**
    - ➛ **Amplitude detector**
    - ➛ **Op amp**
    - ➛ **Low−pass filter**

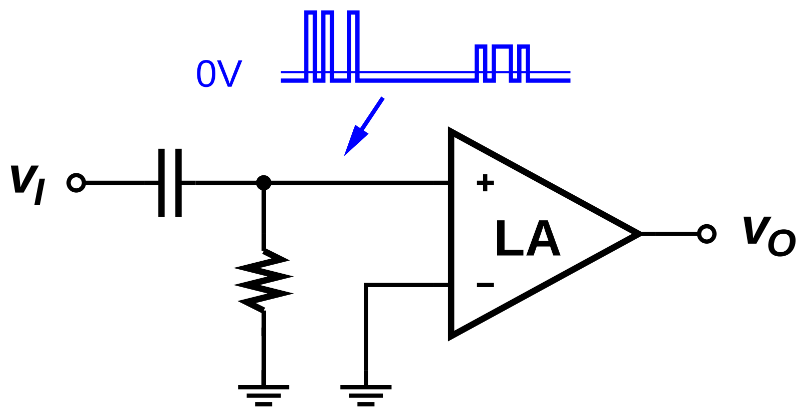


Burst−Mode Amplifier (1)

- **Continuous mode:**
  - **DC balanced**
    - ➜ **Average = 0.5**
  - **e.g., SONET**



- **Burst mode:**
  - **Not DC balanced**
    - ➜ **Average ≪ 0.5, time dependent**
  - **e.g., BPON, EPON**



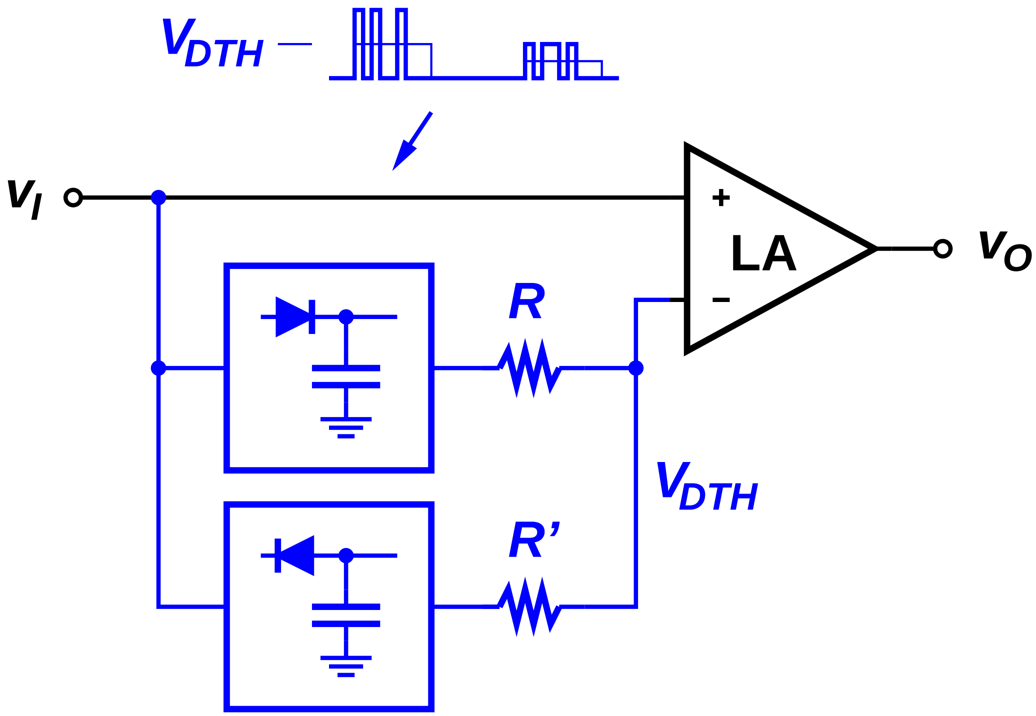
Bad slicing!

➜ **Bit errors**

➜ **Pulse−width distortions**

Burst−Mode Amplifier (2)

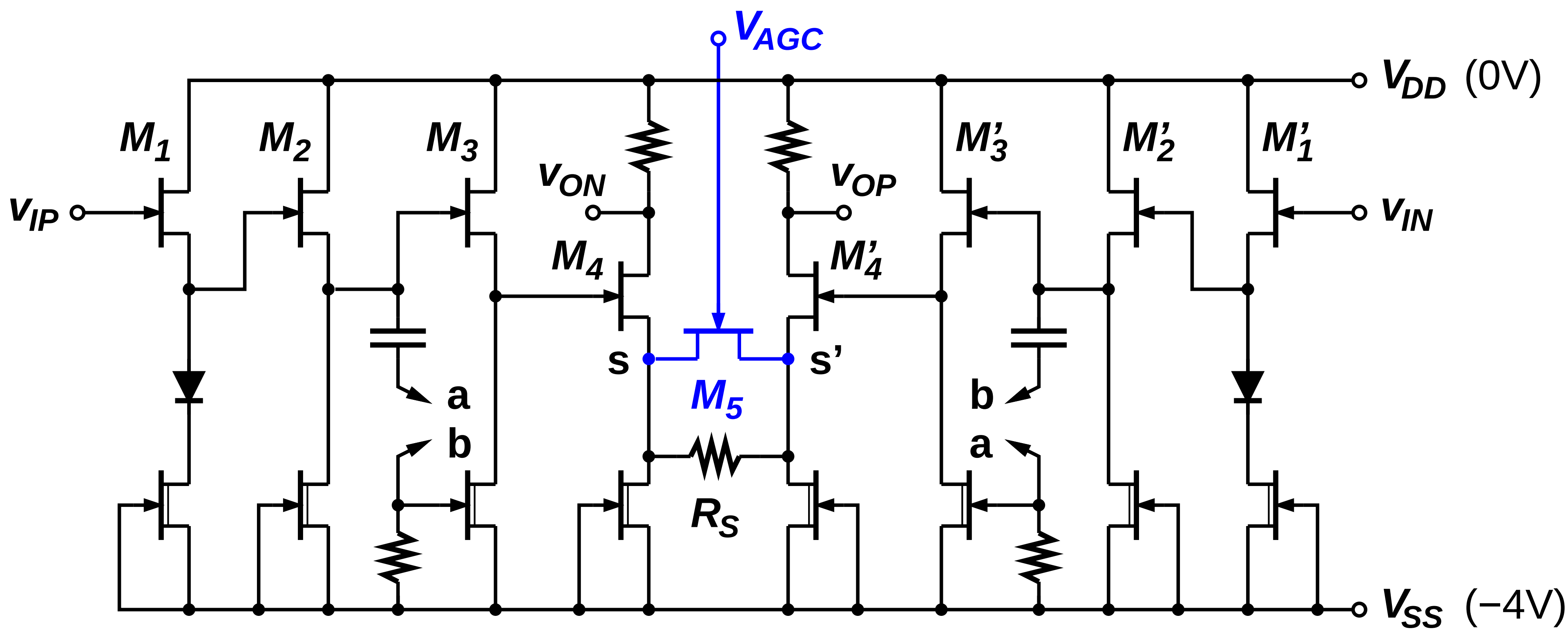
- **Burst−mode limiting amplifier:**



→ **Determine slice level V_{DTH} for each burst; reset peak detectors after burst**

MESFET, HFET Implementation

- **VGA or LA stage:**

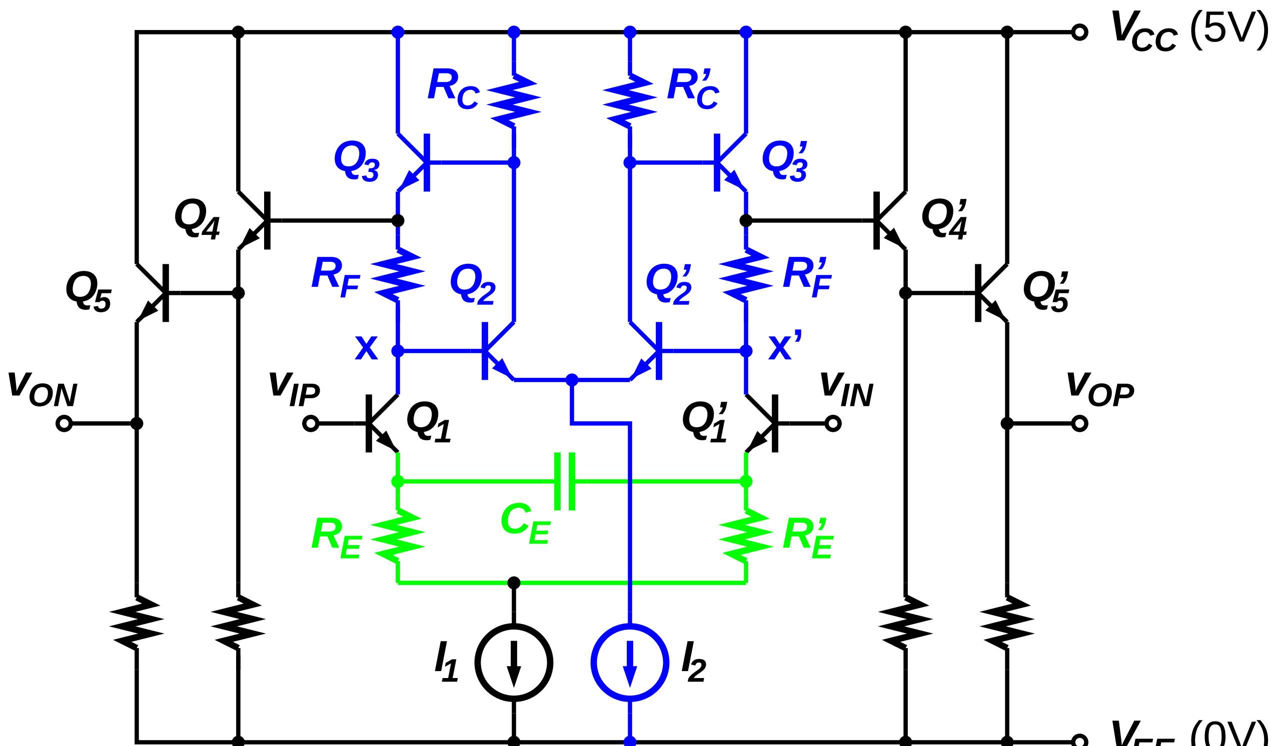


- **Variable source degeneration → gain control (AGC)**
- **For limiting amplifier, connect sources s and s'**
- **Buffers with R−C network to speed up transitions**

[Z. Lao et al. 1997]

BJT, HBT Implementation (1)

- "Cherry−Hooper" LA stage:

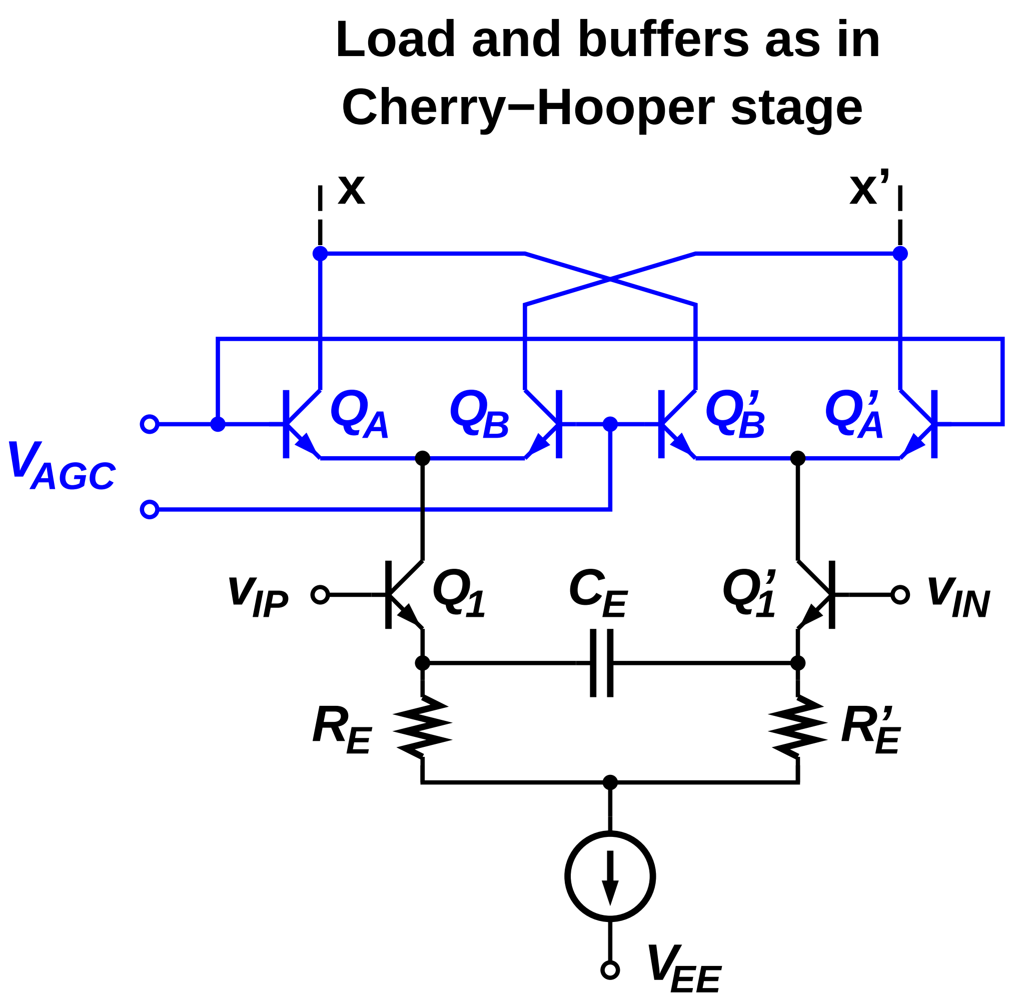


- Gain = R_F / R_E
- Series feedback: R_E
  - ➜ Reduce input cap.
  - ➜ Speed up input pole
- Shunt feedback: R_F
  - ➜ Suppress cap. at x, x'
  - ➜ Suppress Miller effect
- Emitter followers
  - ➜ Buffer outputs
  - ➜ Increase V_{CE1}

[T. Masuda et al. 2000]
[E. Cherry et al. 1963]

BJT, HBT Implementation (2)

- **VGA stage:**

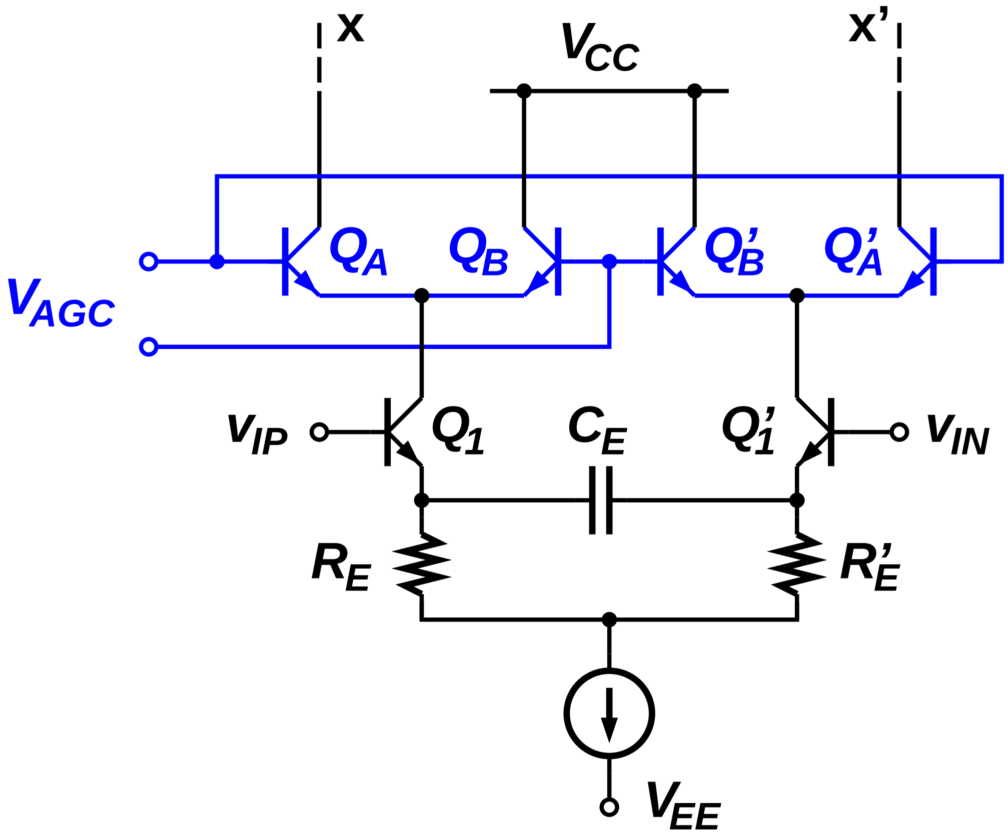


- **Reduce gain by adding inverted signal current**
- **"Gilbert cell"**
- **4−Quadrant multiplier: gain = 0 for V_{AGC} = 0**
  → Avoid signal inversion

[M. Moller et al. 1994]

BJT, HBT Implementation (3)

- **VGA stage:**

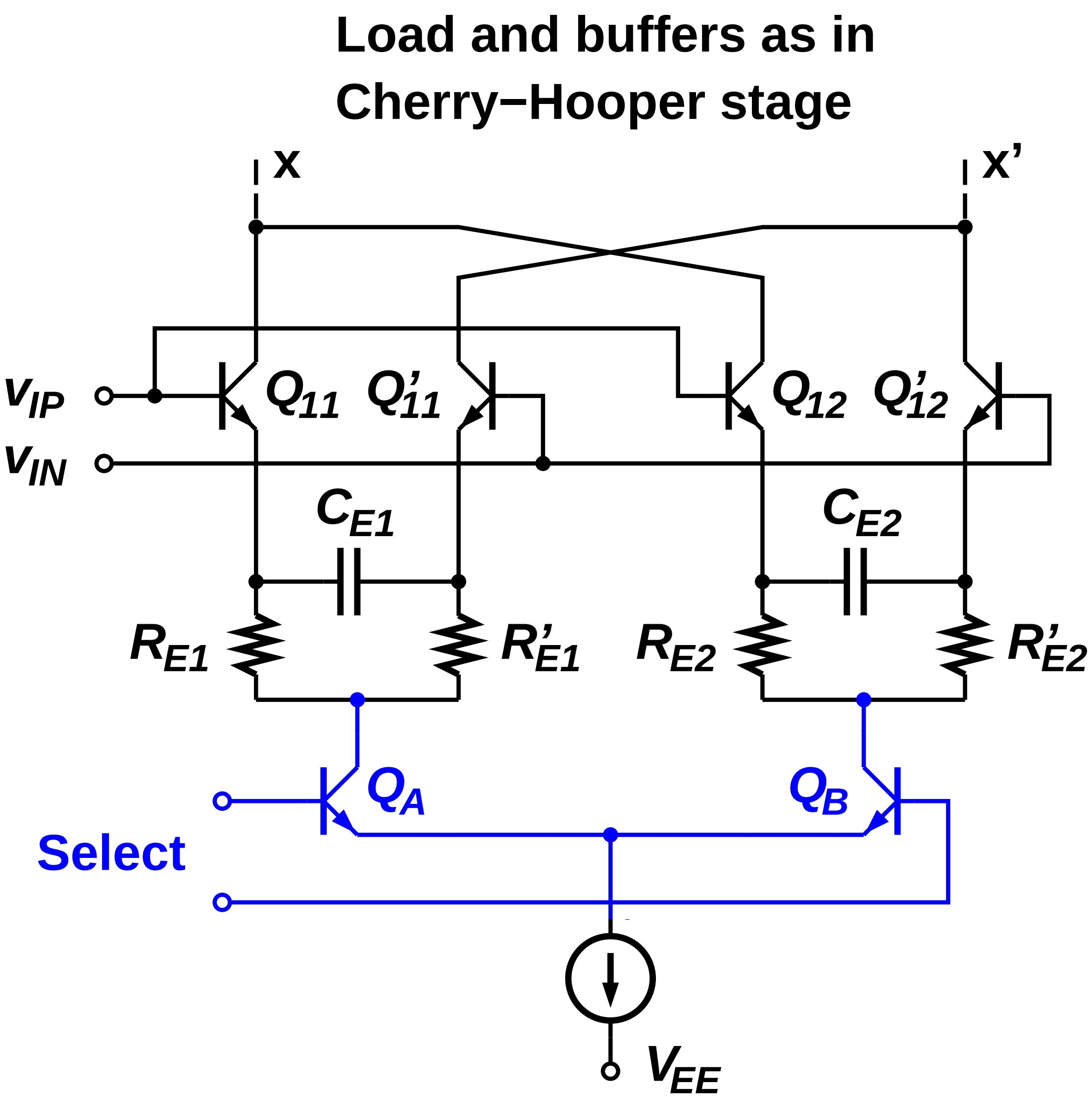


- **Reduce gain by dumping some of the signal current**
- **2−Quadrant multiplier**
- **Requires bias stabilization**

[M. Soda et al. 1994]

BJT, HBT Implementation (4)

- **PGA stage:**

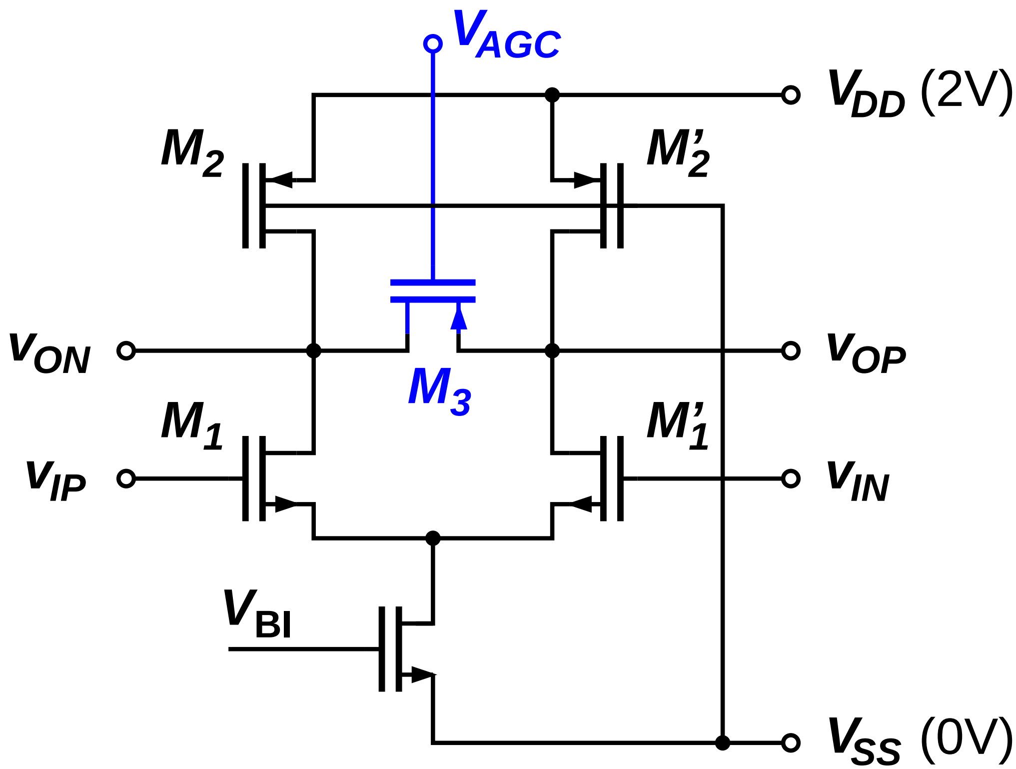


- **Enable one of two differential pairs**
- **Select gain: R_F/R_{E1} or R_F/R_{E2}**

[Y. Greshishchev et al. 2000]

CMOS Implementation (1)

- **Low−voltage VGA stage:**



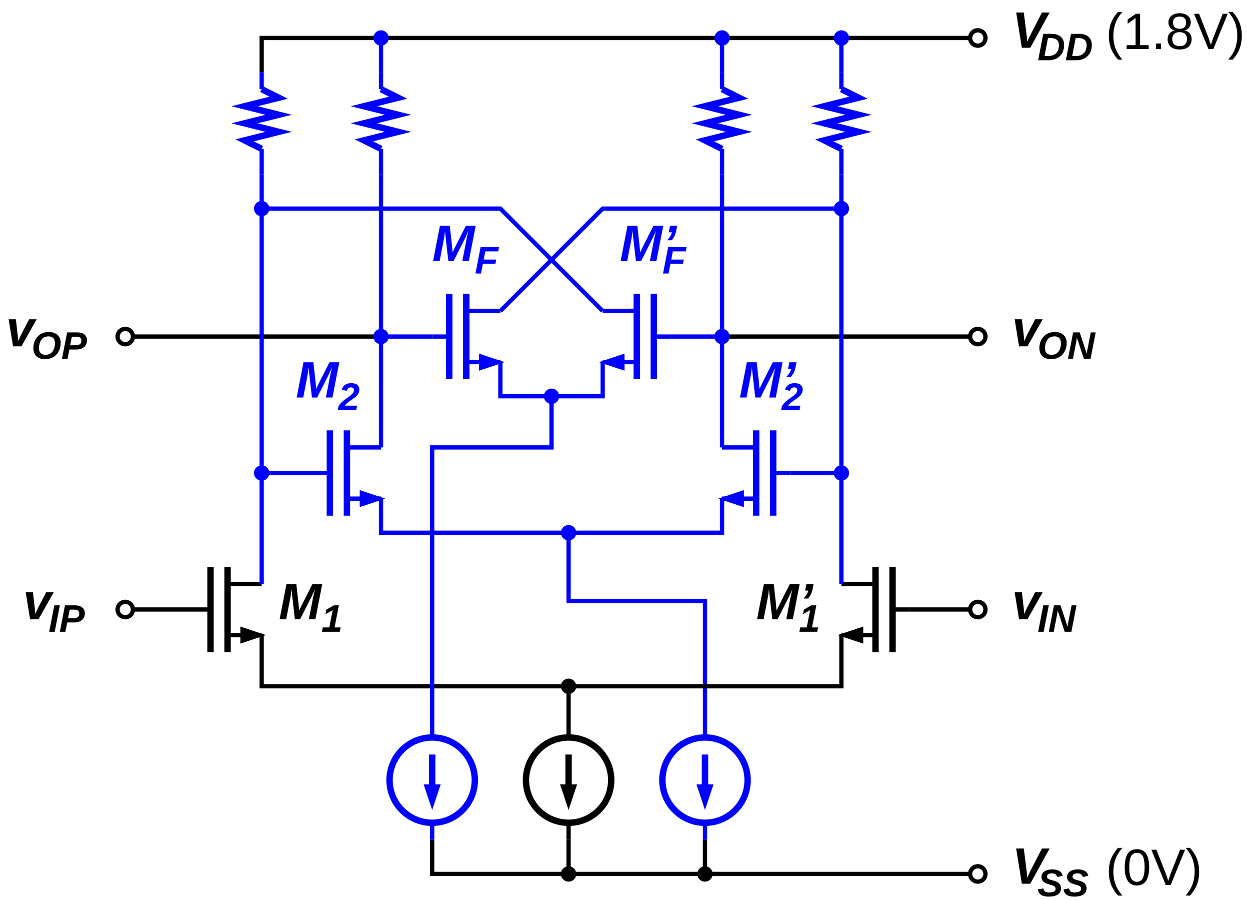
- **Variable (differential) p−MOS load**

  → Gain control (AGC)

[A. Tanabe et al. 1998]

CMOS Implementation (2)

- **LA stage:**

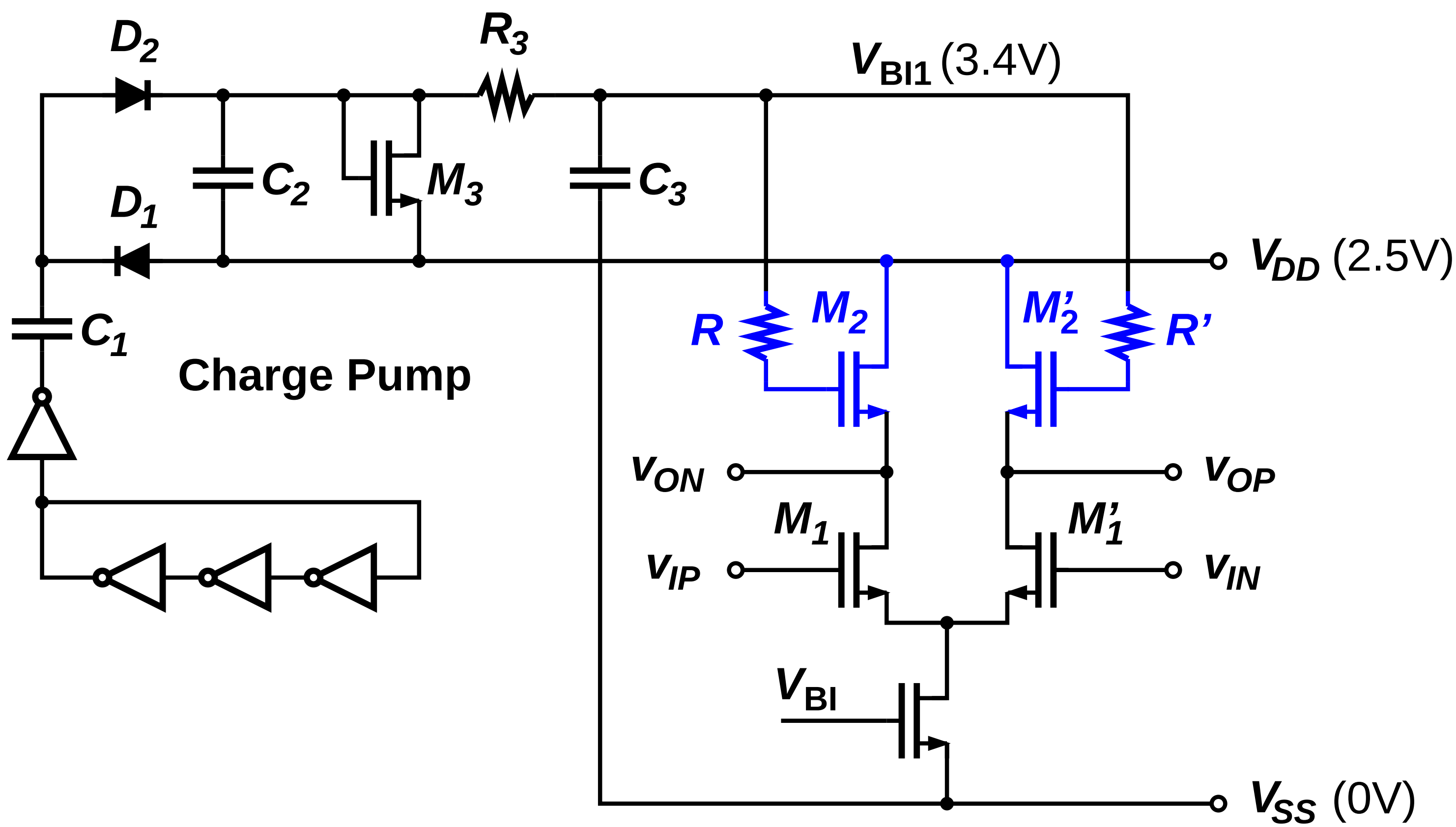


- **Active−feedback TIA load**

[S. Galal et al. 2003]

CMOS Implementation (3)

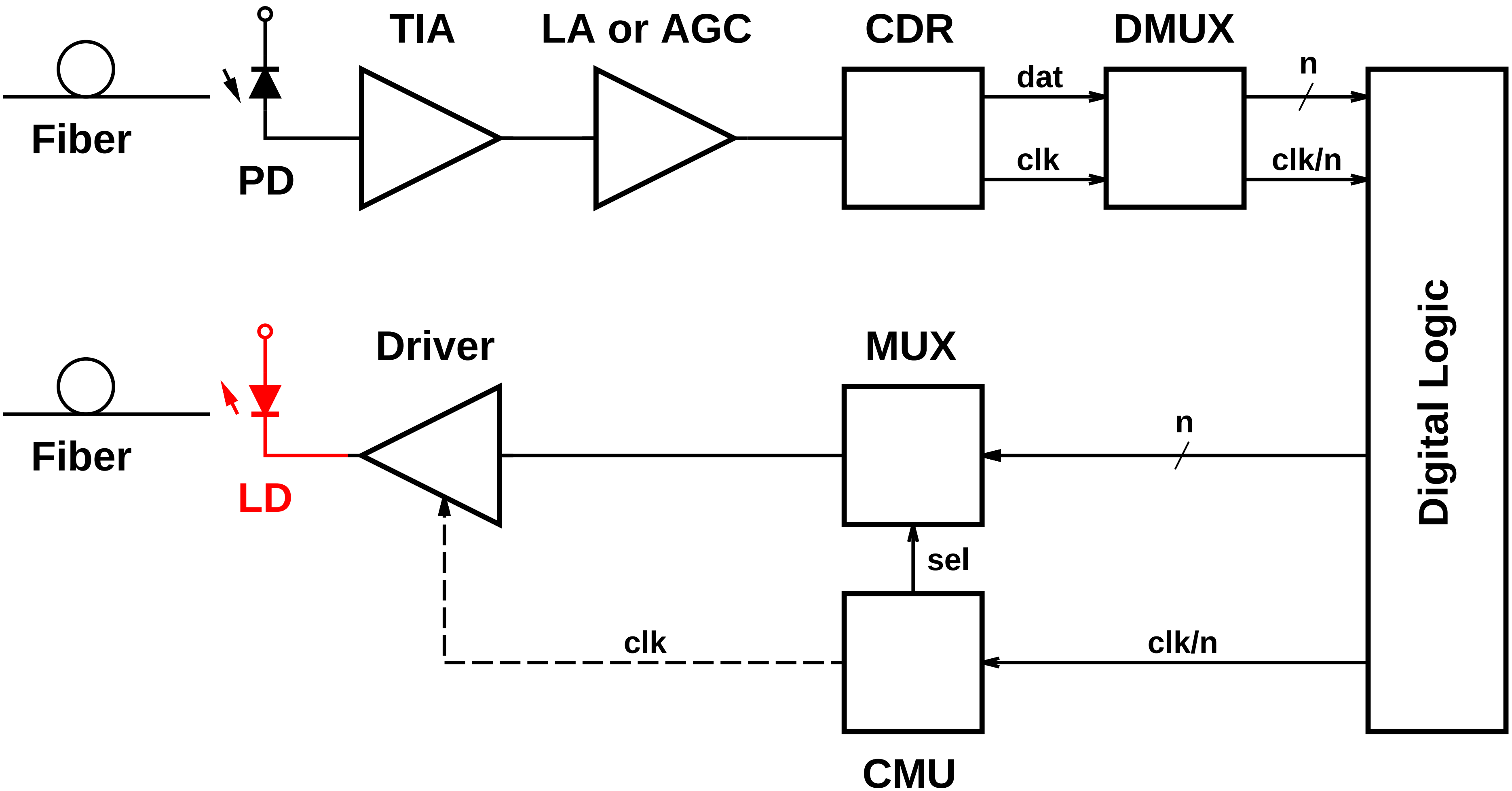
- **LA stage:**



- **Active inductor loads (M_2, R) → extended bandwidth**
- **High gate bias voltage (V_{BI1}) → extended headroom**
- **Stable gain: $(W_1/W_2)^{1/2}$**

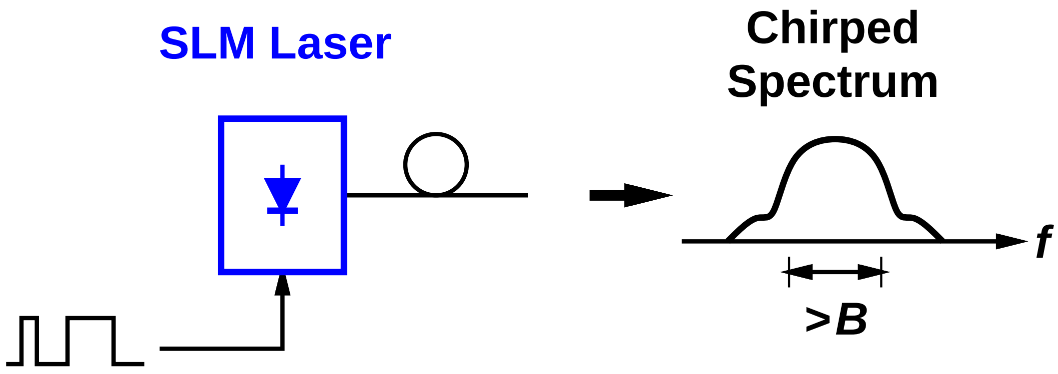
[E. Sackinger et al. 2000]

Lasers & Modulators



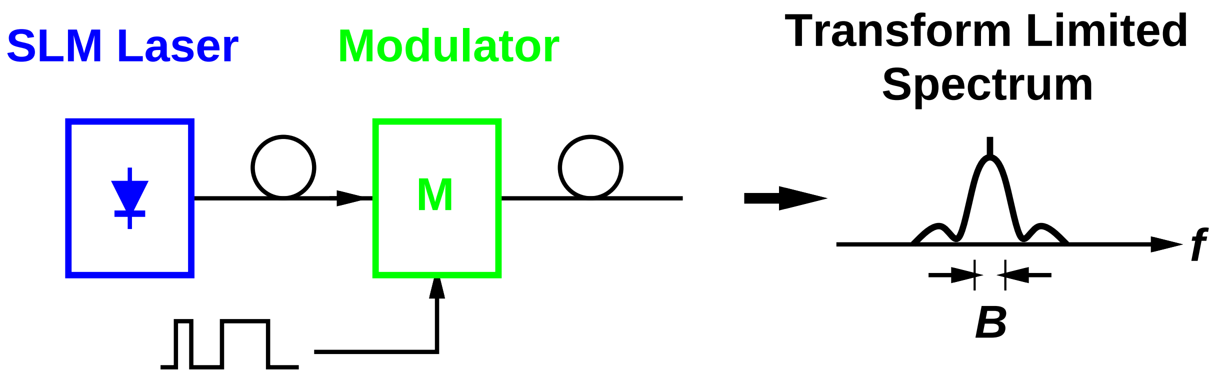
Direct vs. External Modulation

- **Direct modulation:**



→ **Linewidth limited by chirp (or laser modes)**
→ **Strong dispersion at 1.55 um; used mostly at 1.3 um**

- **External modulation:**

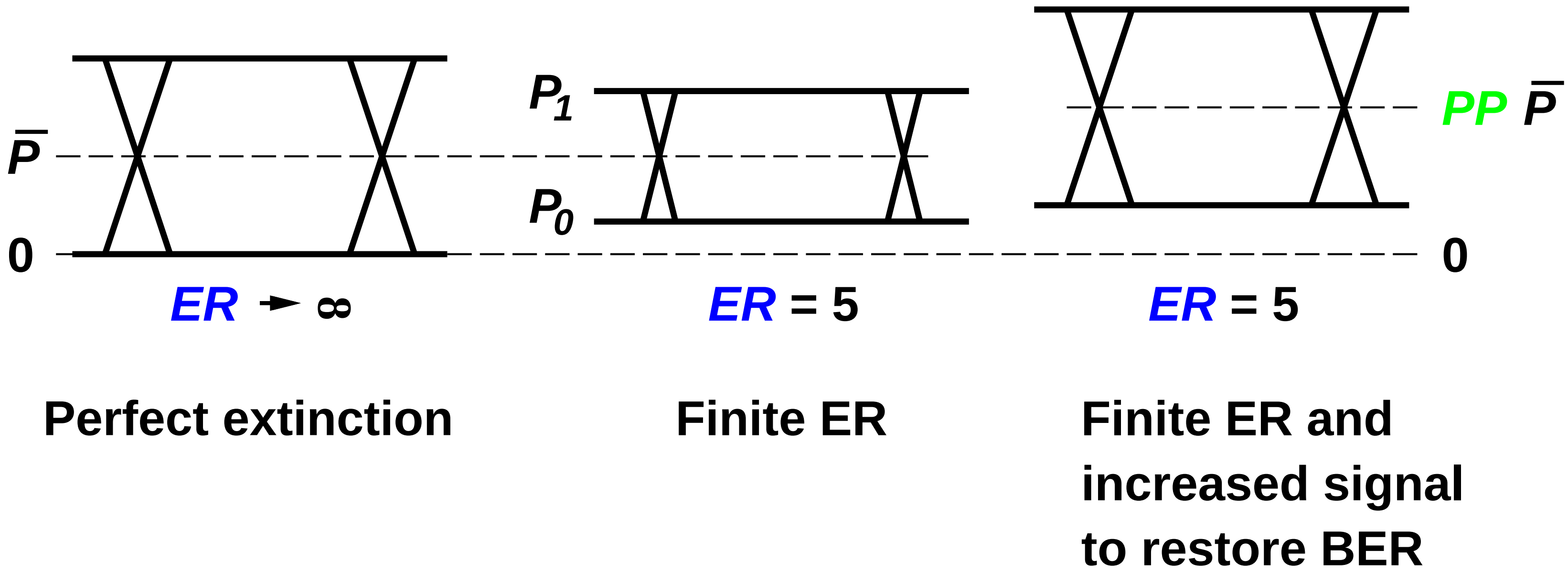


→ **Linewidth limited by baseband signal ($BW \approx B$)**
→ **Used at 1.55 um for long distance communication**

Extinction Ratio

- Extinction ratio definition:

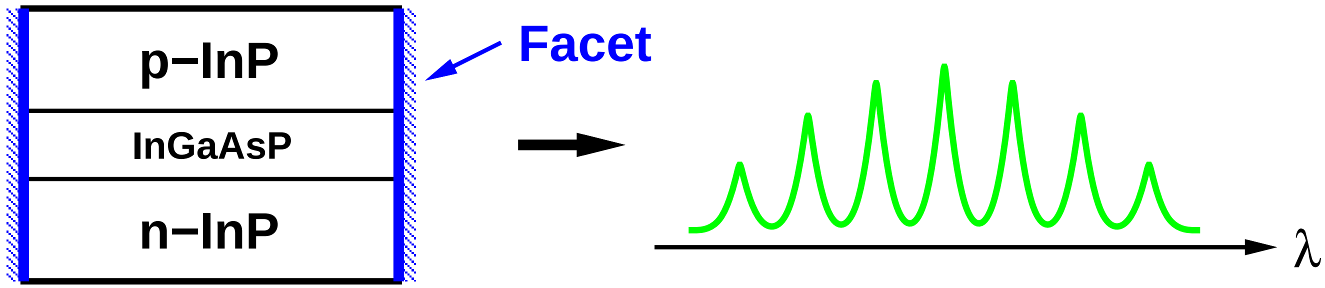
$$ER = \frac{P_1}{P_0}$$



- Finite extinction ratio causes power penalty (*PP*)
- Typical ER values:
  - Direct modulation: 9 ... 14 dB
  - External modulation: 11 ... 17 dB

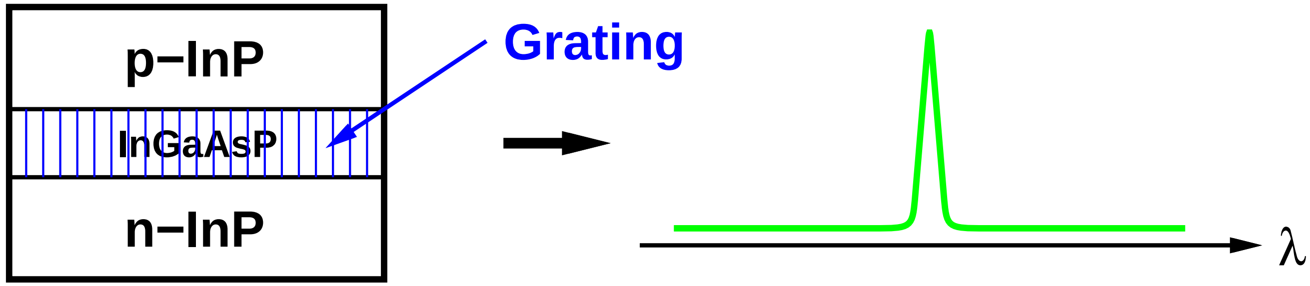
Laser Types

- **Fabry−Perot (FP) laser:**



➛ **Multiple−longitudinal mode (MLM); wide linewidth**

- **Distributed−feedback (DFB) laser:**



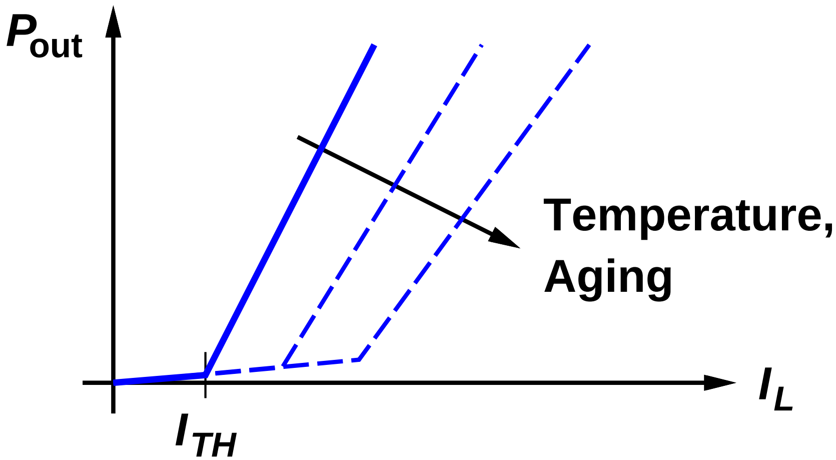
➛ **Single−longitudinal mode (SLM); narrorw linewidth**

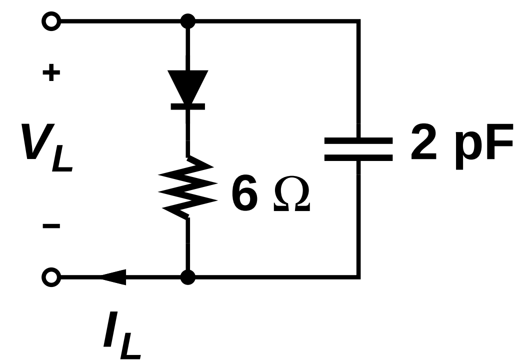
- **Vertical−cavity surface−emitting laser (VCSEL):**

➛ **Single−longitudinal mode; fairly narrorw linewidth**

Laser Characteristics

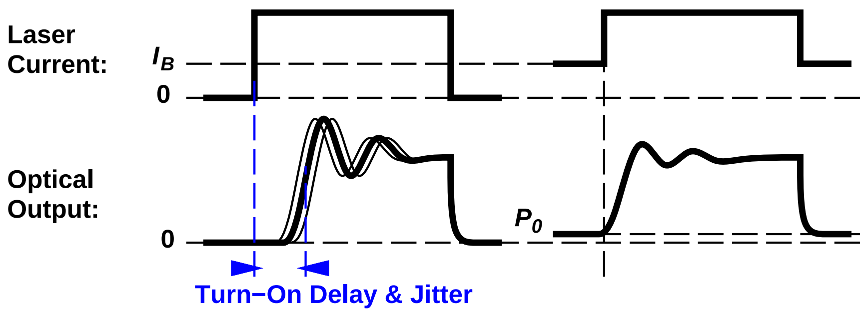
- **Optical output power vs. laser current:**





➞ **Automatic power control (APC) is required**

- **Turn−on delay, jitter, and extinction ratio:**

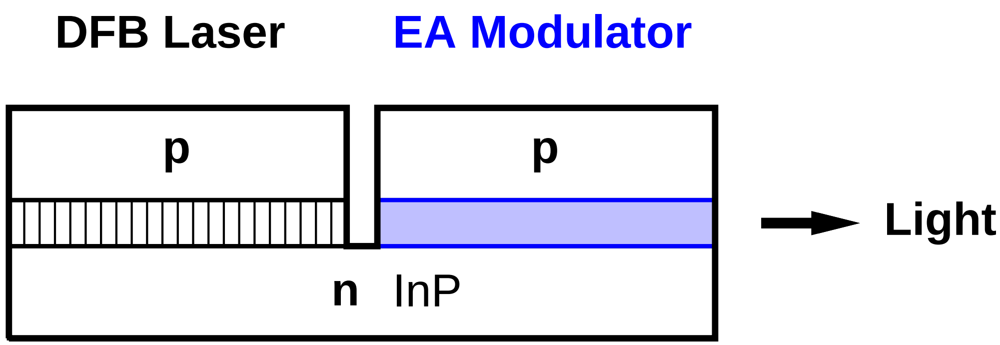


➞ **Use bias current $I_B = I_{TH}$ to reduce turn−on delay and jitter**

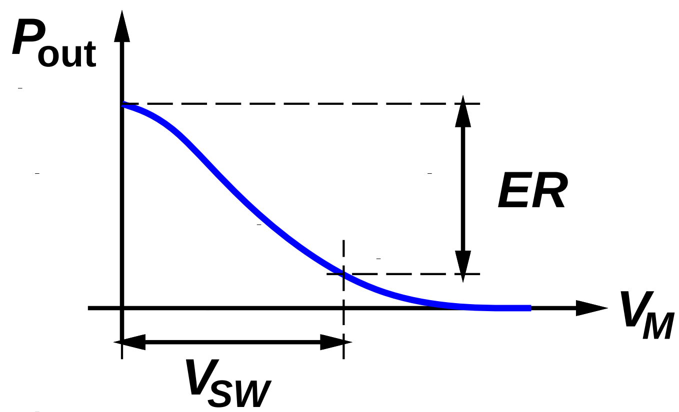
➞ **But bias current also reduces the extinction ratio!**

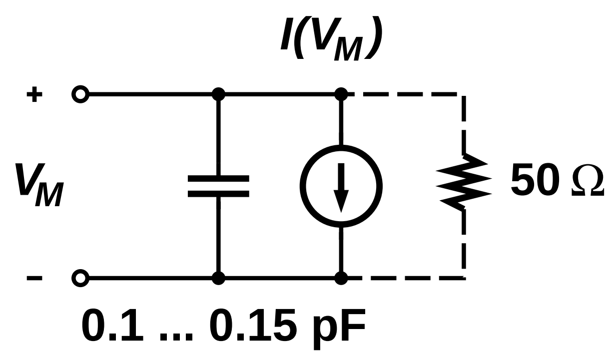
Electroabsorption Modulator (EAM)

- **Can be integrated with laser on same substrate (EML):**



- **Switching curve and electrical equivalent circuit:**





V_{SW} = 1.5 ... 4 V

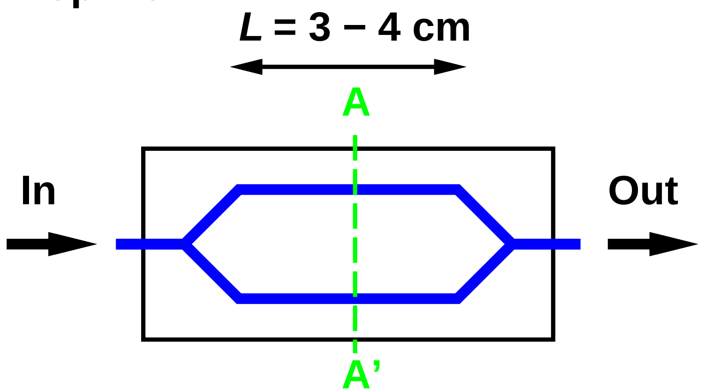
ER = 11 ... 13 dB

- **Reverse biased diode**
  - → **Capacitive load**
  - → **Nonlinear photocurrent**
- **Often parallel matching resistor**

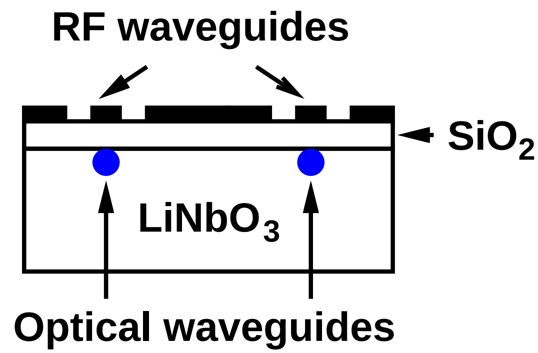
Mach−Zehnder Modulator (MZM)

- **Typically based on lithium niobate (lithium−niobate modulator):**

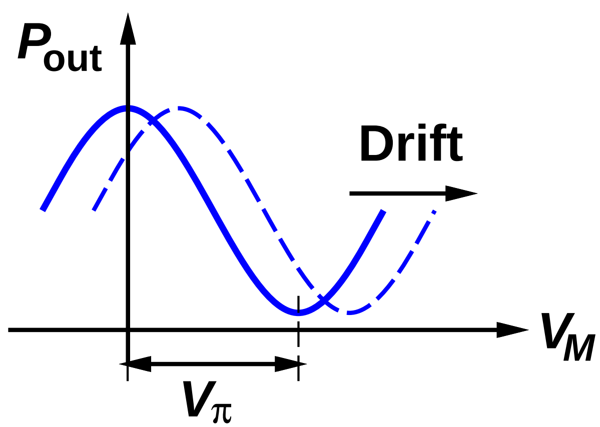
Top view:

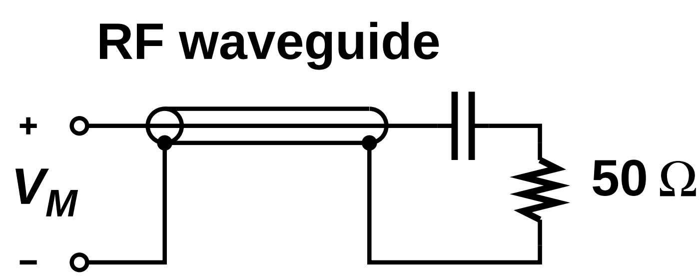


Cut A−A':



- **Switching curve and electrical equivalent circuit:**



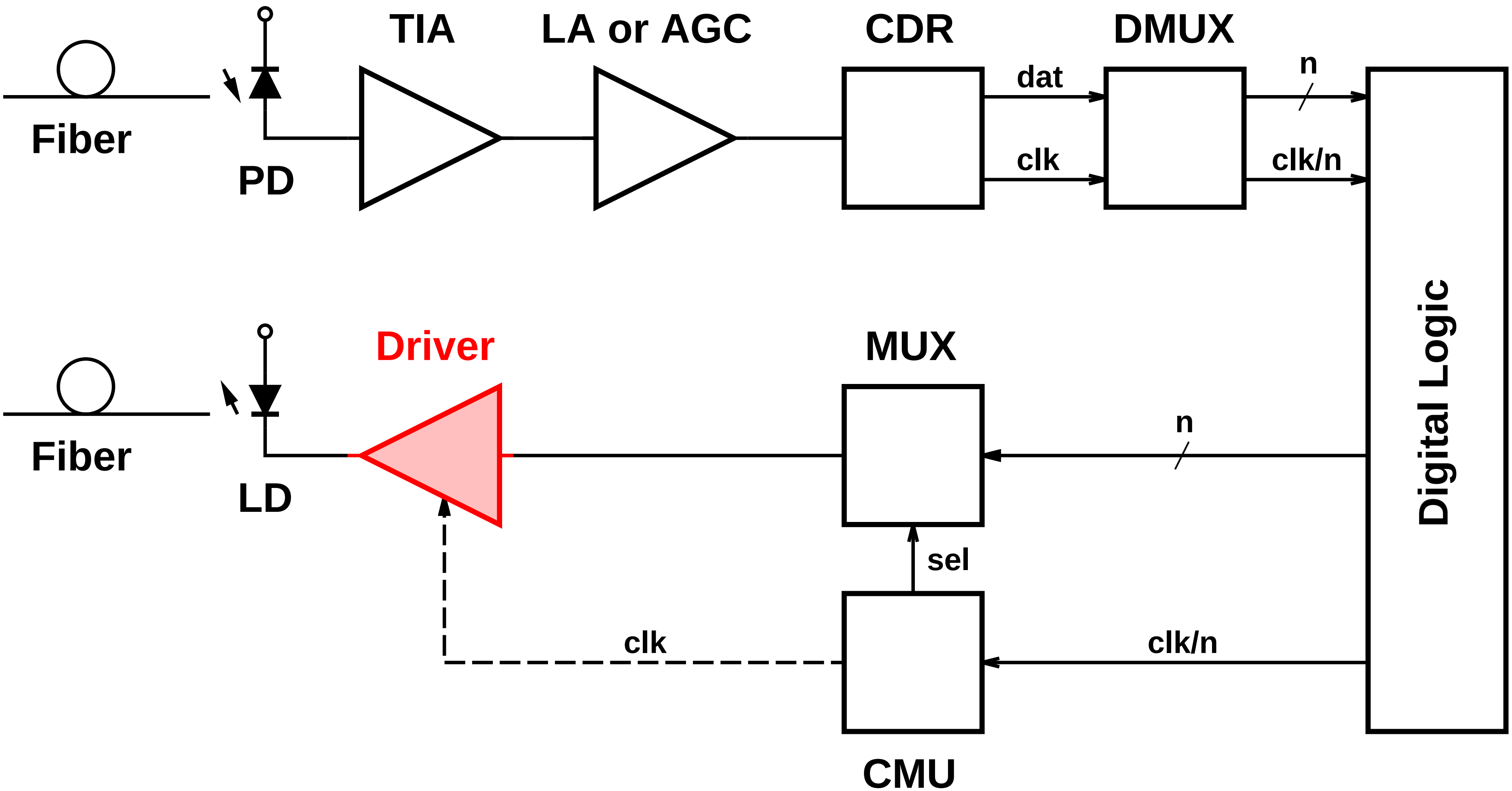


V_π = 4 ... 6 V

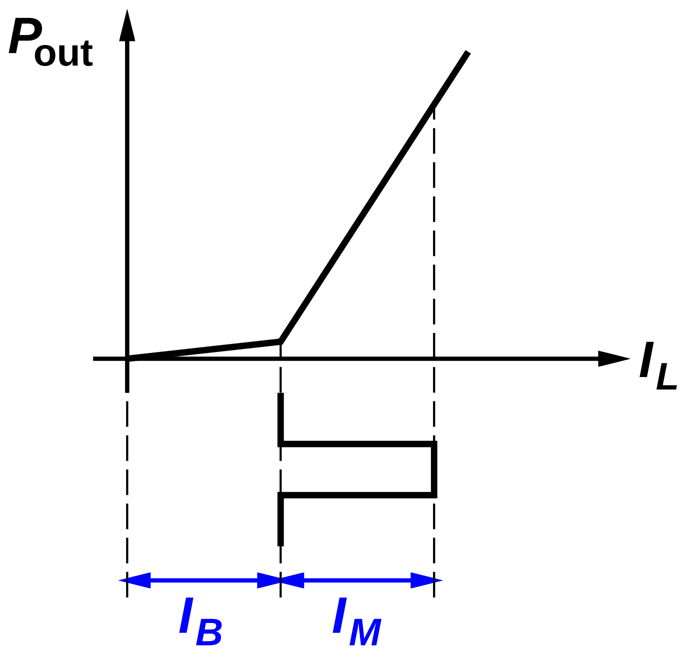
ER = 15 ... 17 dB

- **Terminated transmission line**
- **Single− and dual−drive versions**

Laser and Modulator Drivers



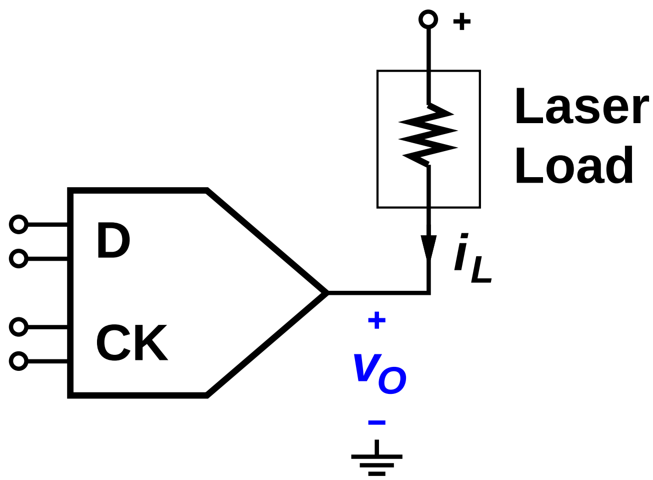
Modulation and Bias Current Range (Laser Drivers)



- Choose modulation and bias current range large enough to reach desired laser power under worst−case conditions (high temperature, end of life, etc.)

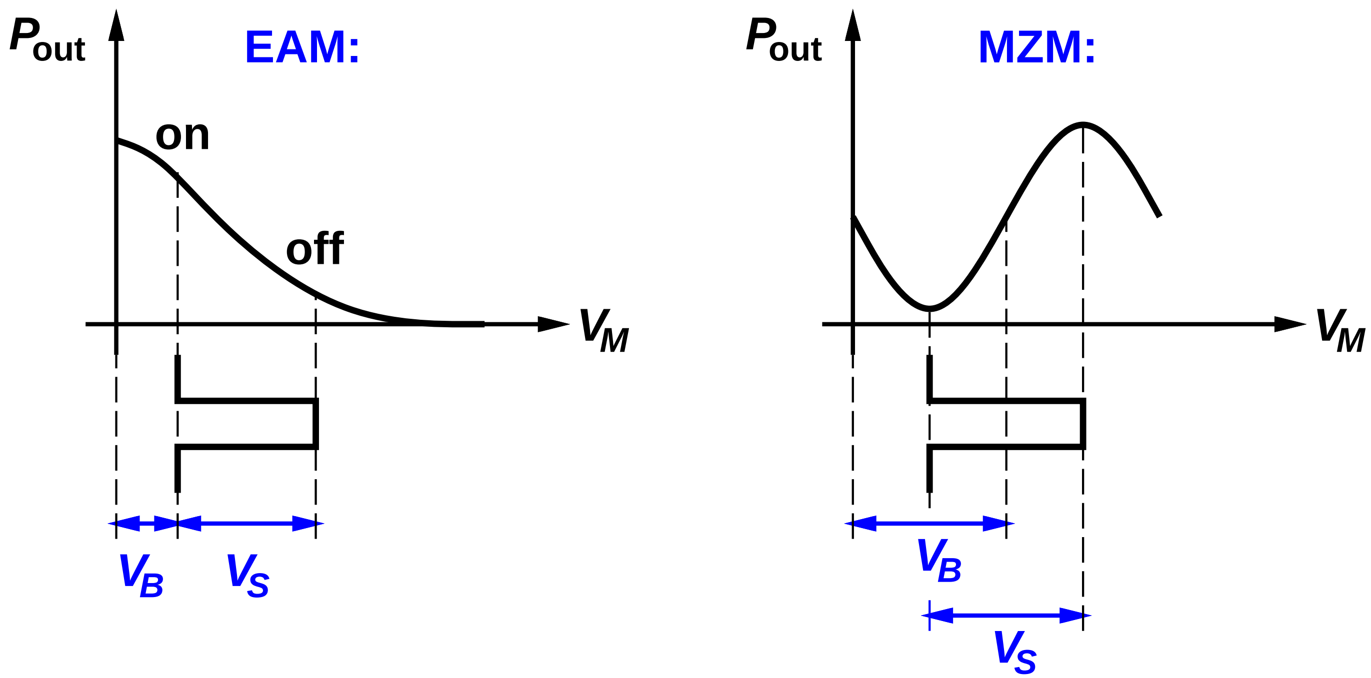
- Typical values (for drivers of uncooled lasers):
  - Modulation current range: 10 ... 100 mA
  - Bias current range: 0 ... 100 mA

Output Voltage Range (Laser Drivers)



- **Permissible output voltage range = compliance voltage**
- **Make minimum voltage small to minimize supply voltage requirements (especially for DC−coupled loads)**
- **Make maximum voltage large to permit pull−up inductor(s) and AC coupling (output swings above the supply voltage)**
- **Typical values:**
  - **Minimum voltage: 1.4 ... 2.0 V**
  - **Maximum voltage: supply voltage**

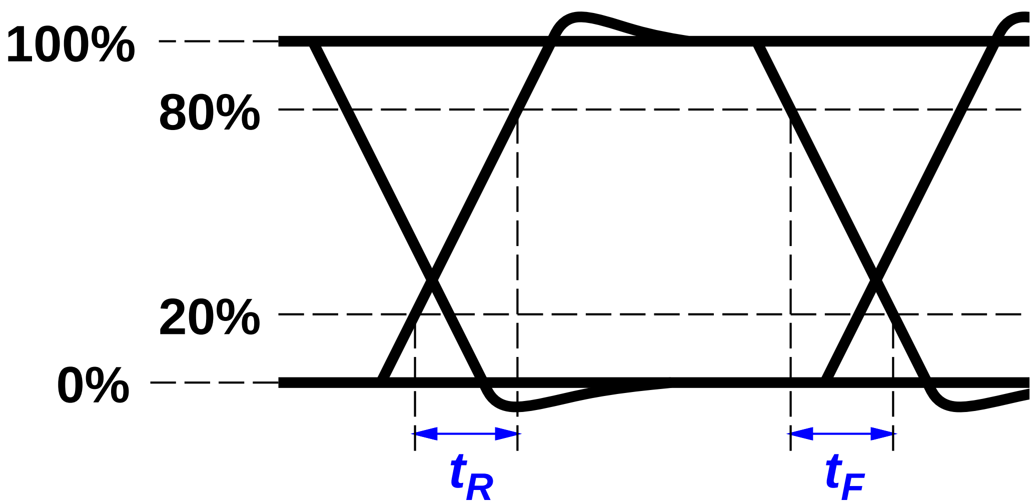
Modulation and Bias Voltage Range (Mod. Drivers)



- Choose modulation and bias voltage range large enough to cover the worst−case conditions
- Typical values for modulation voltage (voltage swing) range:
  - EAM driver: 0.2 ... 3 V
  - MZM driver: 0.5 ... 5 V
- Typical values for bias voltage (DC offset voltage) range:
  - EAM driver: 0 ... 1 V (chirp control)
  - MZM driver: 0 ... 10 V (drift compensation)

Rise and Fall Times

- Time for signal to move from the 20% to the 80% level (sometimes 10% to 90%) and vice versa:



- For laser drivers, fast rise time increases chirp!

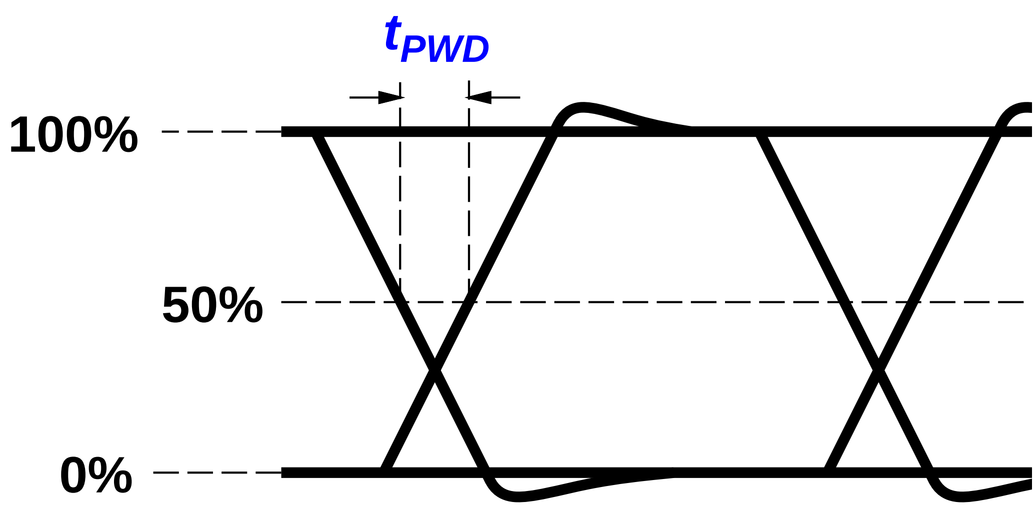
- Typical values:

  2.5 Gb/s: $t_{R,F}$ < 100 ps (0.25 UI)

  10 Gb/s: $t_{R,F}$ < 40 ps (0.40 UI)

Pulse–Width Distortion

- **Observe crossing point in the eye diagram:**

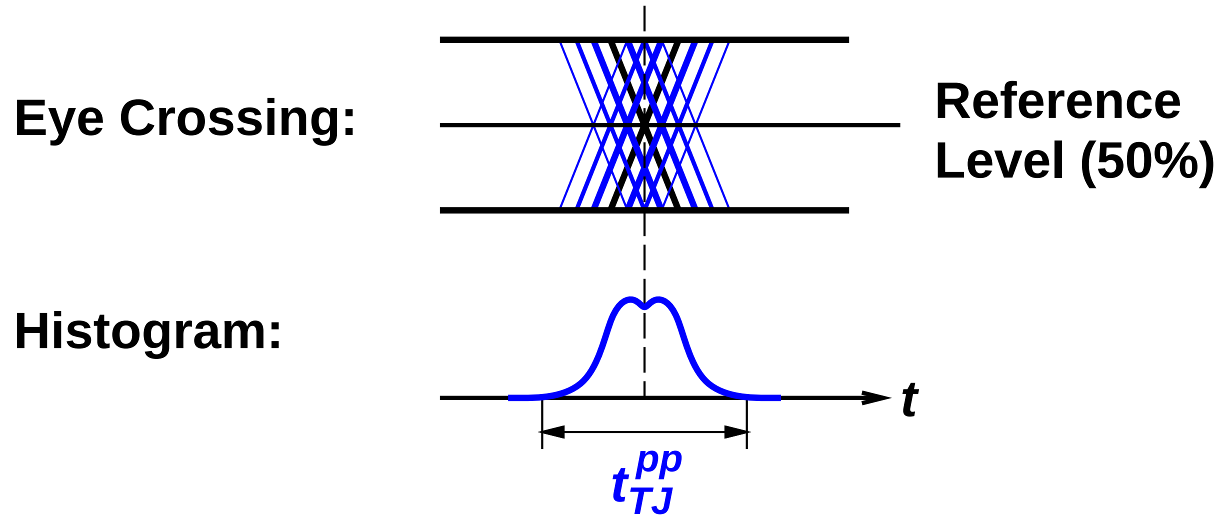


- **Laser/modulator drivers often feature a PWD adjustment**
  → Pulse–width control circuit

- **Typical values < 0.05 UI (electrical, w/o PWD adjust):**
  2.5 Gb/s: t_{PWD} < 20 ps
  10 Gb/s: t_{PWD} < 5 ps

Jitter Generation

- Histogram of 50% crossing points:



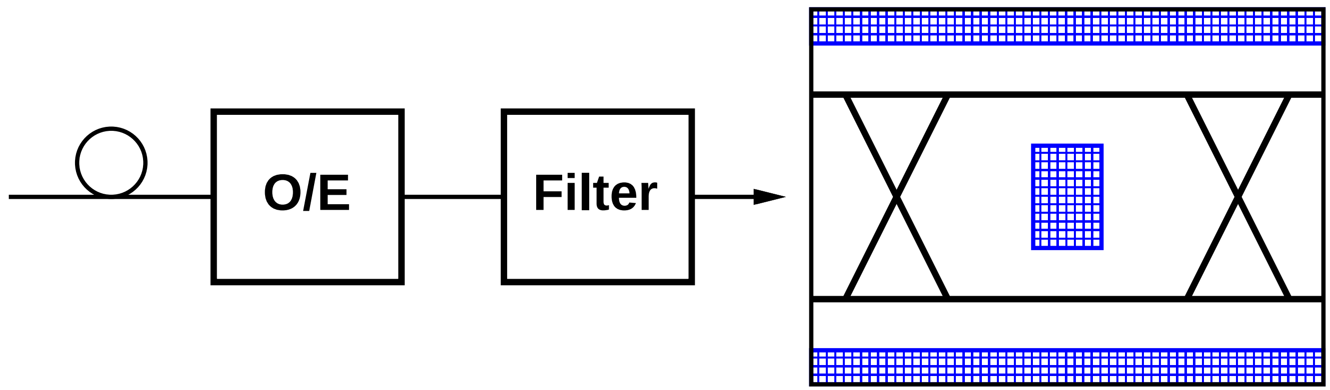
- Jitter types: determinisitic (DJ), random (RJ), total (TJ), ...
- Jitter amount: histogram, peak−to−peak (pp), root−mean−square (rms), ...
- Jitter bandwidth: wideband, narrowband
- Typical values < 0.1 UI peak−peak (SONET requirements):

  2.5 Gb/s: t_{TJ}^{pp} < 40 ps @ BW = 12 kHz to 20 MHz

  10 Gb/s: t_{TJ}^{pp} < 10 ps @ BW = 50 kHz to 80 MHz

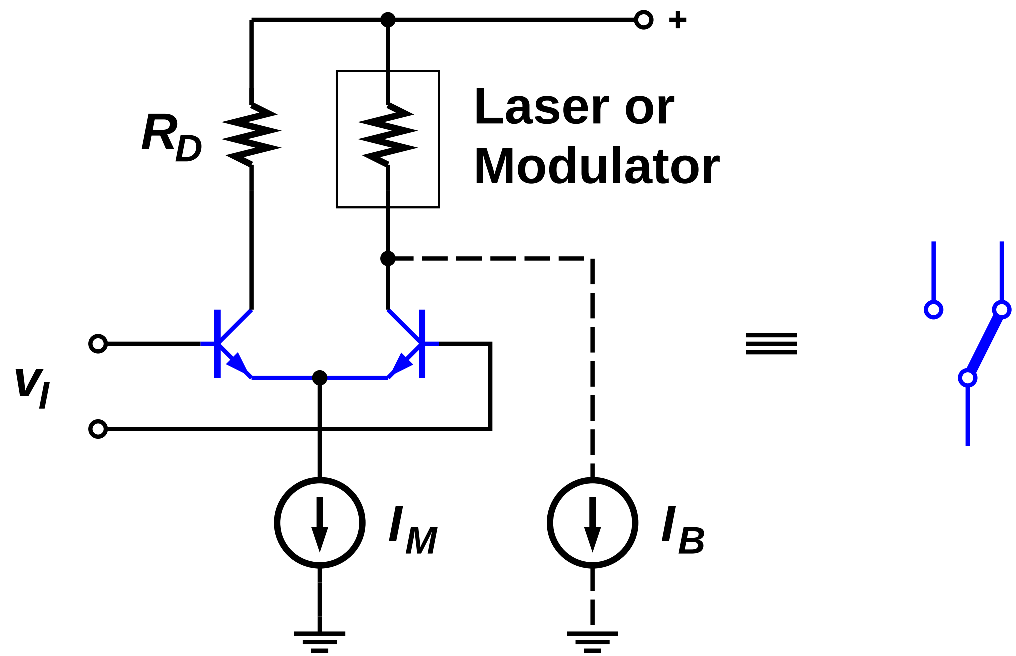
Eye−Diagram Mask Test

- Compare filtered optical eye against mask:



- The filter simulates the receiver response:
  4th−order Bessel−Thompson response with $BW = 0.75B$
  (SONET reference receiver)
- Signal must stay outside of the blue areas
- Mask test checks rise/fall time, PWD, jitter, ISI, ringing, noise, ...

Current−Steering Output Stage

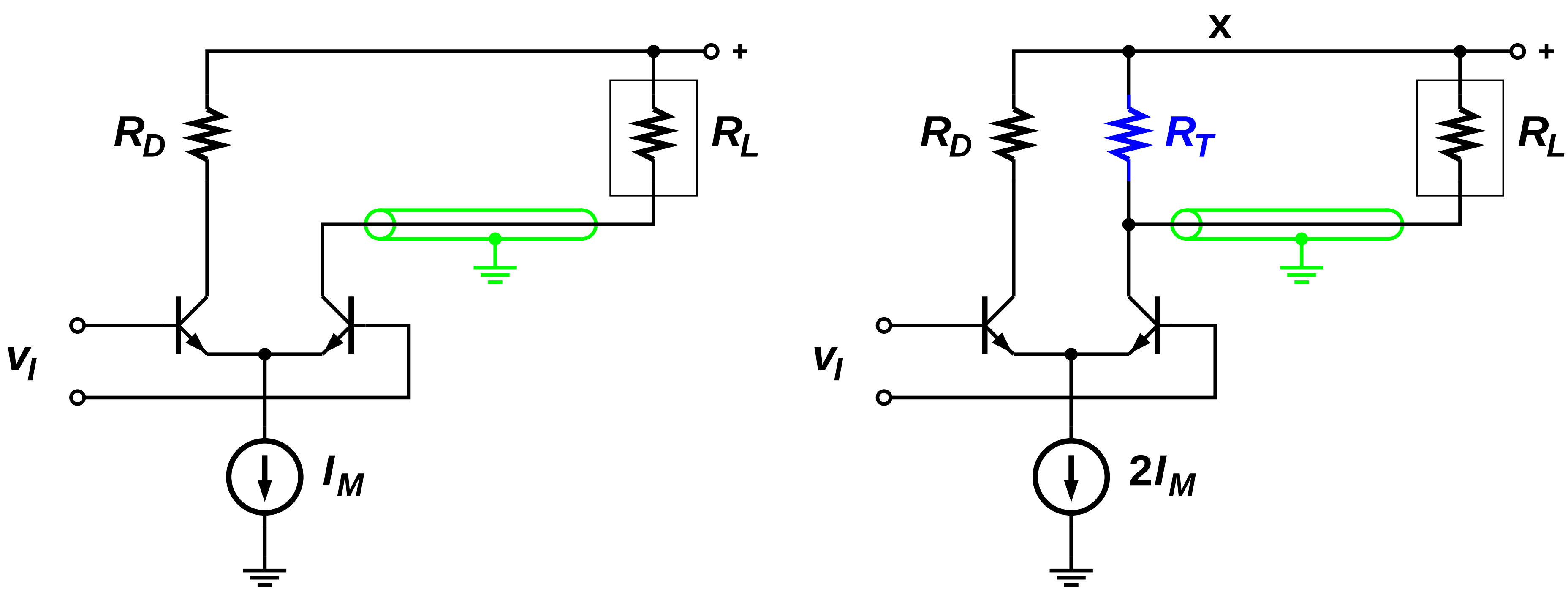


- Differential inputs:
  - ➛ Avoids pulse−width distortions
  - ➛ Insensitive to supply noise
- Constant power supply current:
  - ➛ Minimizes power supply noise
  - ➛ But increased power dissipation

- Control modulation current (or voltage) with tail current source I_M
- Add bias current source, I_B, if bias current (or voltage) is required

Transmission Line & Termination

- For high−speed drivers use transmission line to connect laser/modulator:



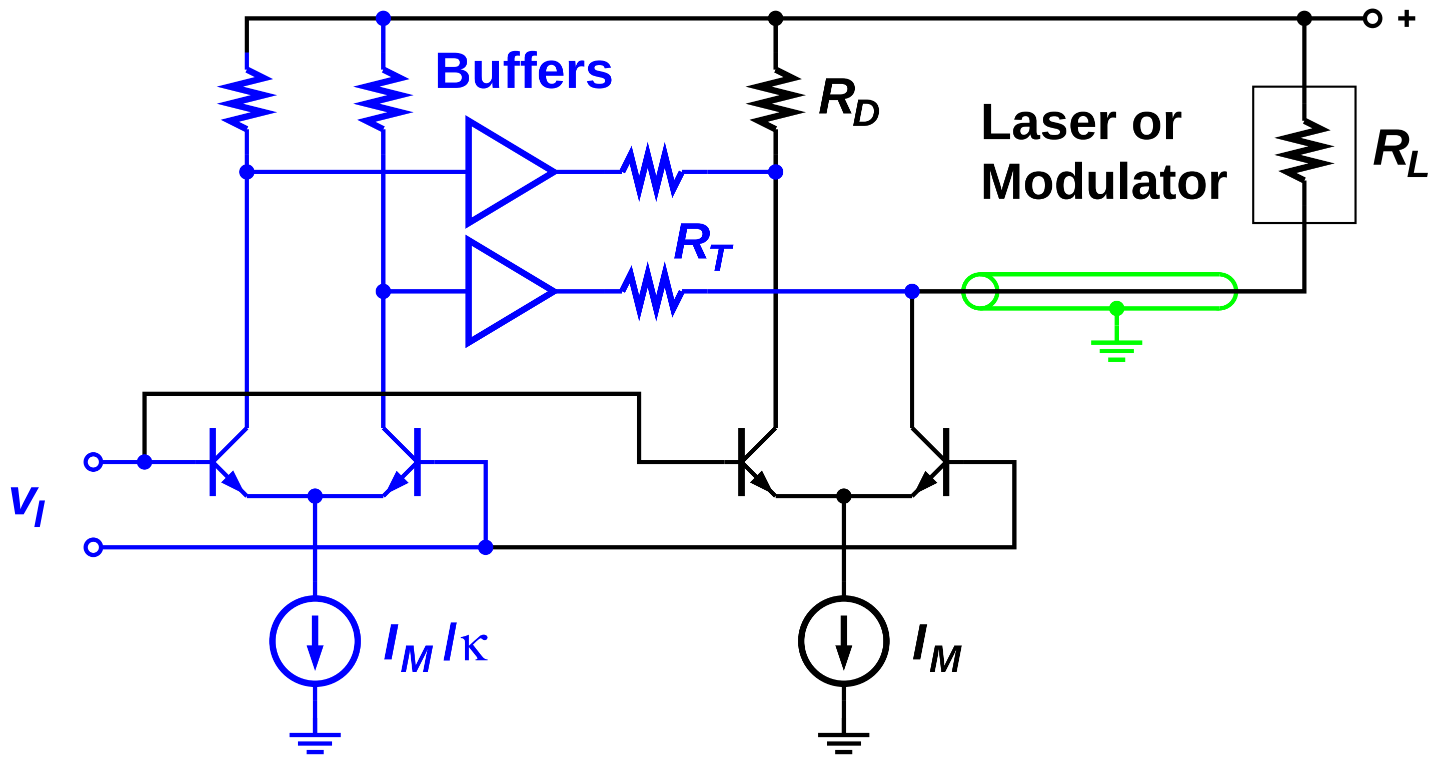
Without back termination

➞ Reflections cannot be absorbed
➞ Double reflections
➞ Jitter and ER degradation
➞ Use only if load matching is good

With back termination

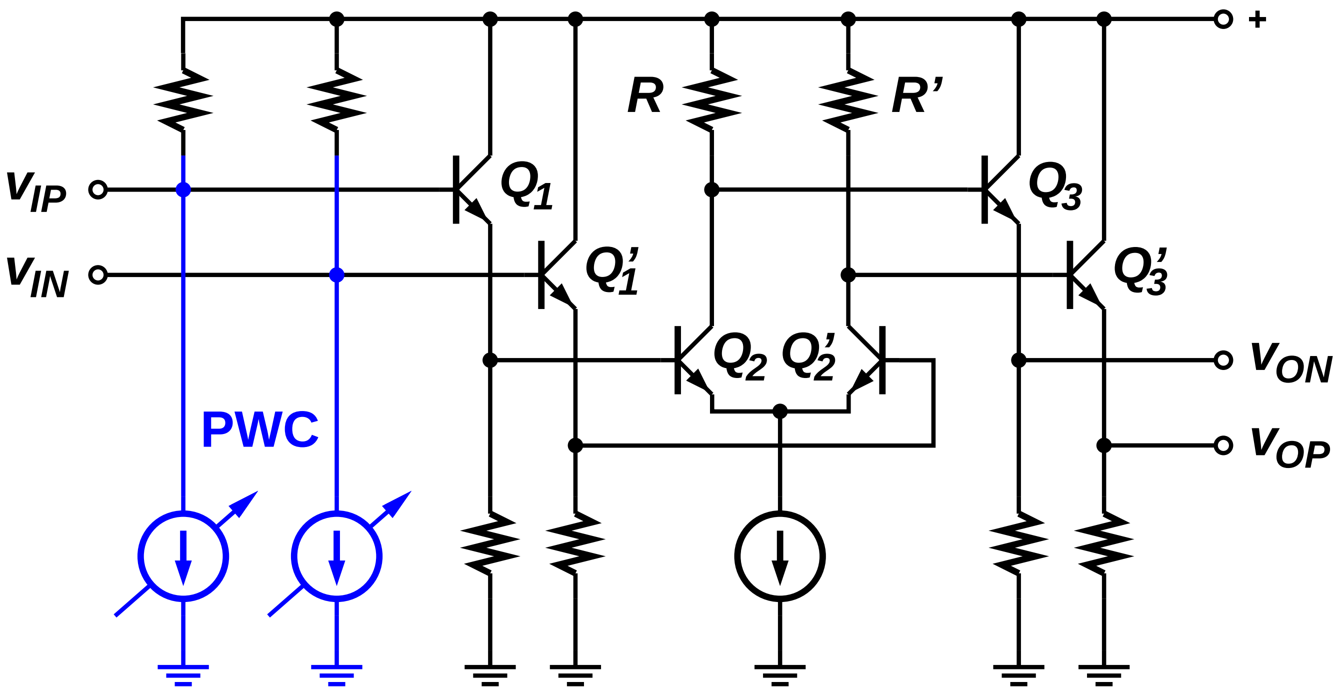
➞ Absorb reflections
➞ Clean signal at load
➞ Power dissipation doubled!
➞ Use if load matching is bad

Active Back Termination



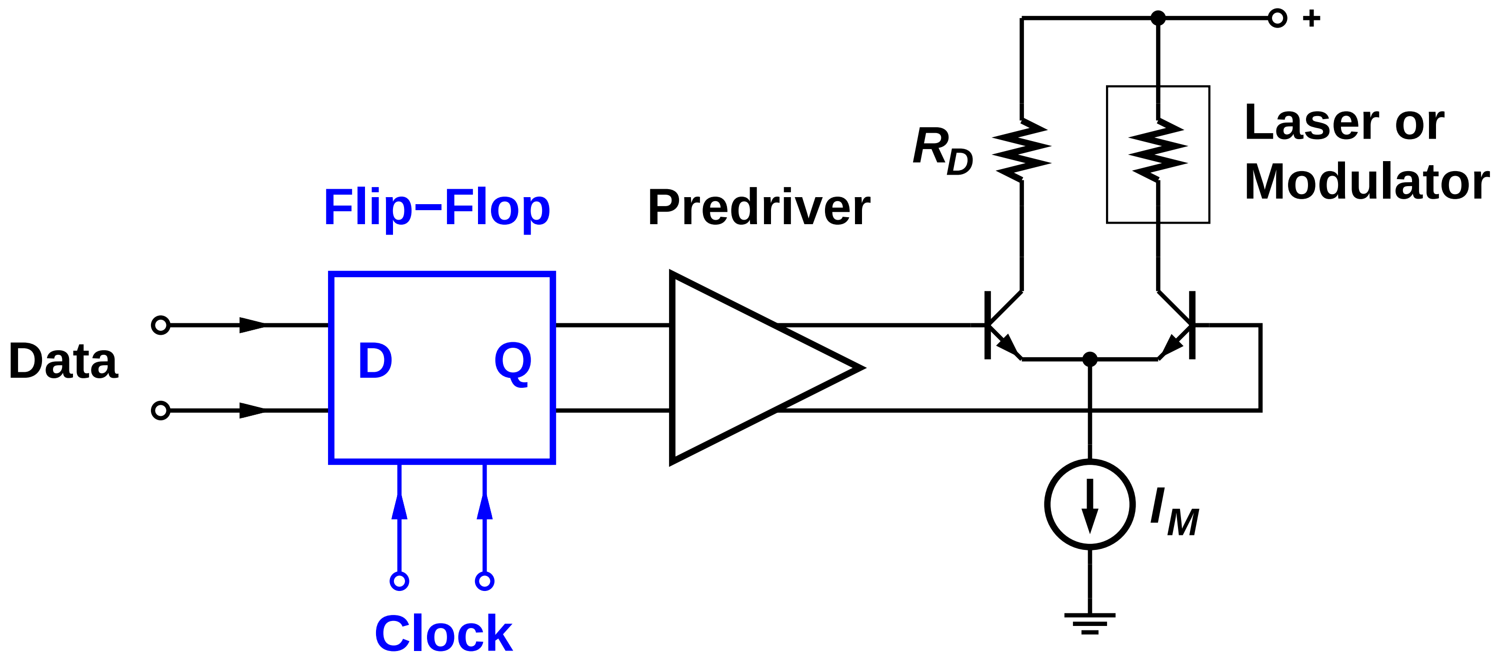
- **Back termination resistor connected to clean signal from replica**
  - → **Normally no voltage across termination resistor (only when refections occur)**
  - → **Low power**

Predriver & Pulse−Width Control



- **Predriver needed to drive large current−steering transistors and to provide sufficient swing at their inputs**
- **Compensate pulse−width distortions due to laser, modulator, ...**
  - ➜ **Introduce offset voltage at input of predriver for pulse−width control (PWC)**

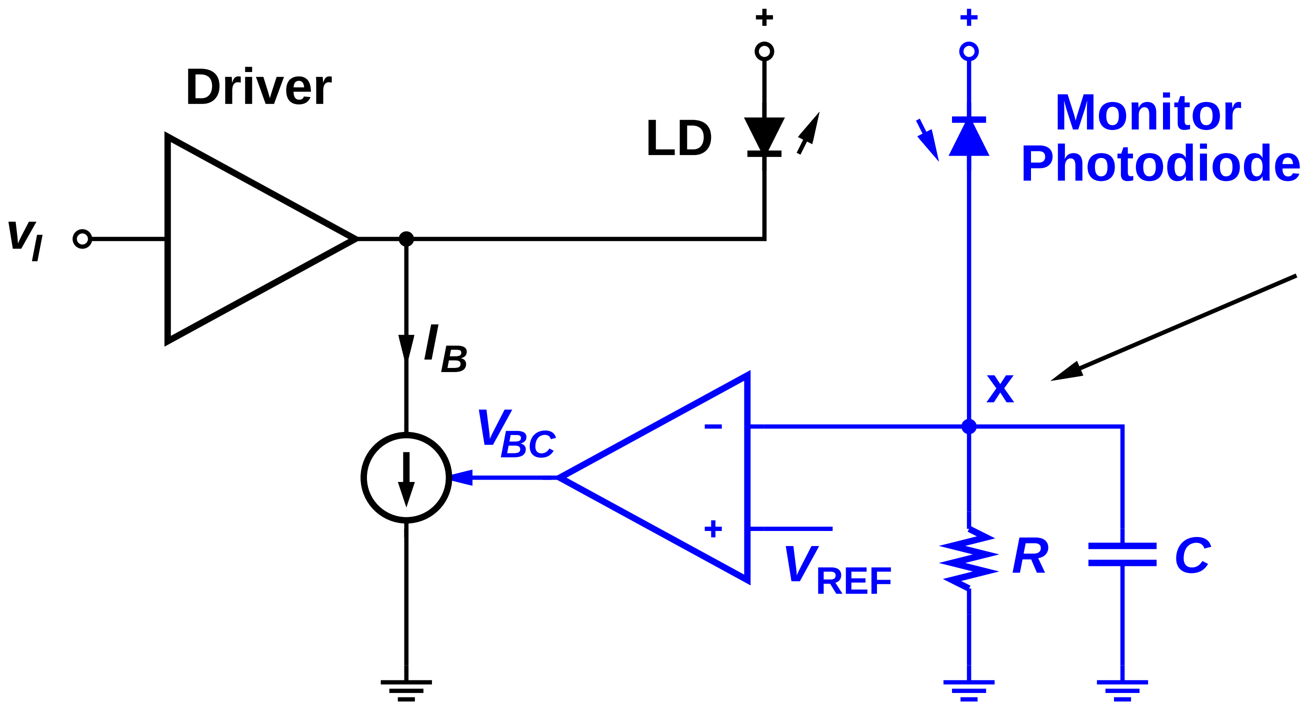
Data Retiming



- Eliminate pulse−width distortion and jitter from input data
- But clock jitter contributes directly to output jitter of transmitter!

  → Low−jitter clock is required

Automatic Power Control (Lasers)

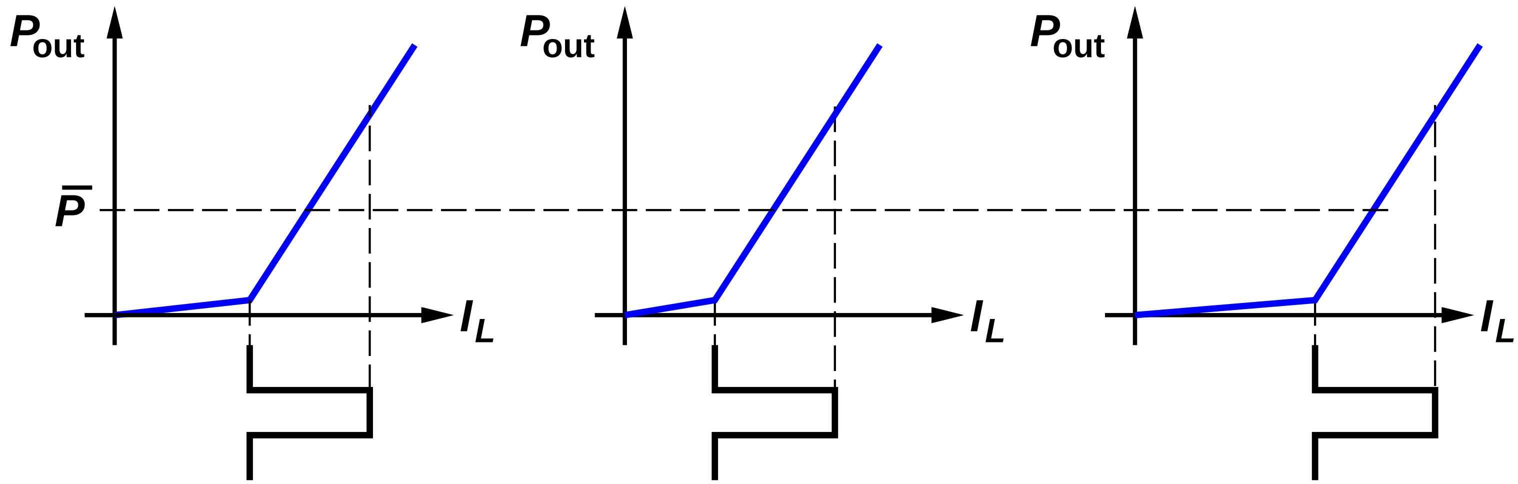


- Monitor photodiode measures the optical output power; automatic power control (APC) controls the laser current
- Average output power is measured
  → Constant mark density required
- Only bias current is adjusted
  → Laser's slope efficiency must be stable

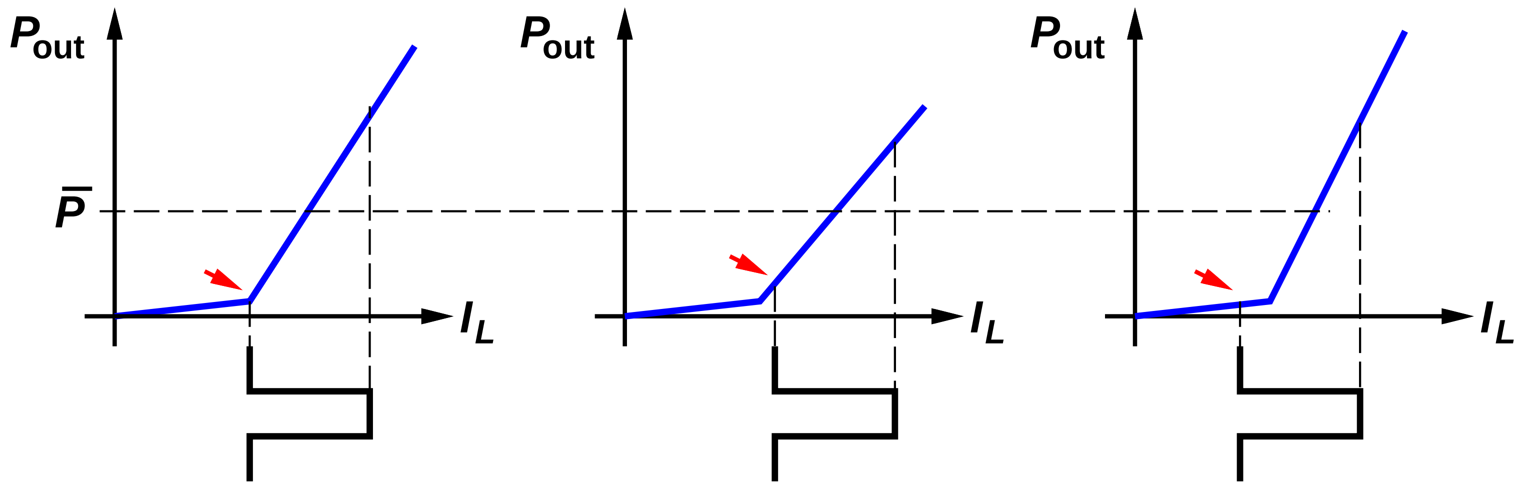
} Continuous−mode single−loop APC

Automatic Power Control (Lasers)

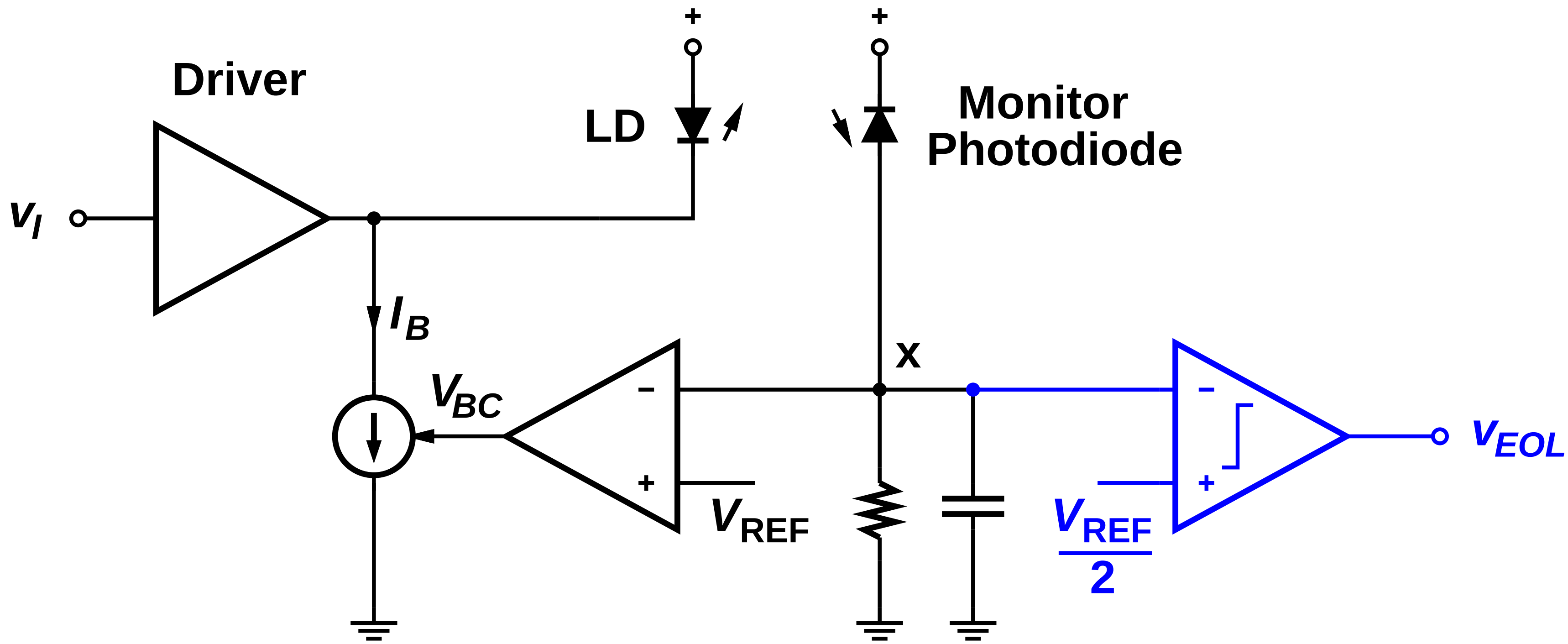
- **Laser threshold−current variations with single−loop APC:**



- **Laser slope−efficiency variations with single−loop APC:**

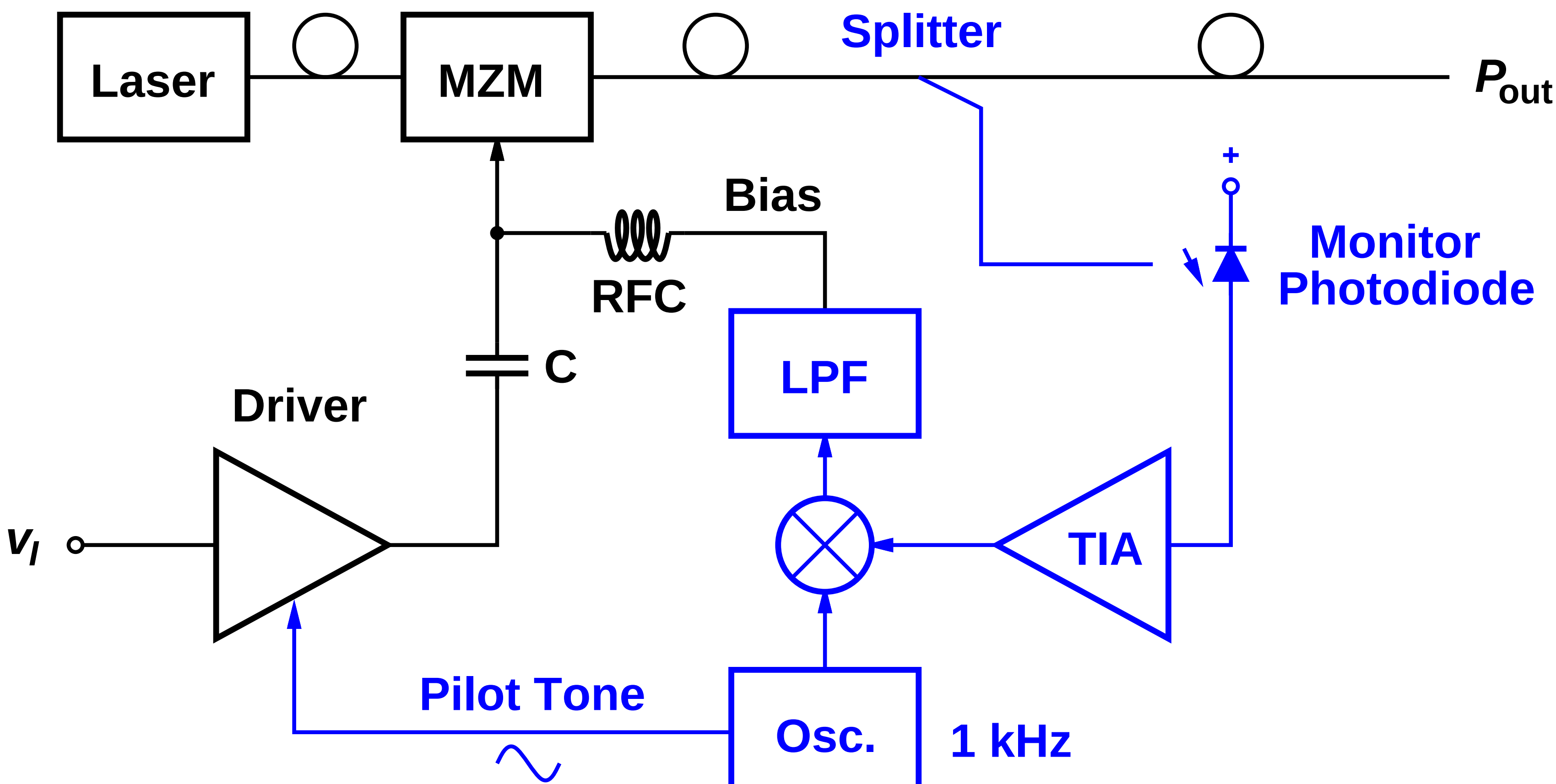


End–of–Life Detection (Lasers)



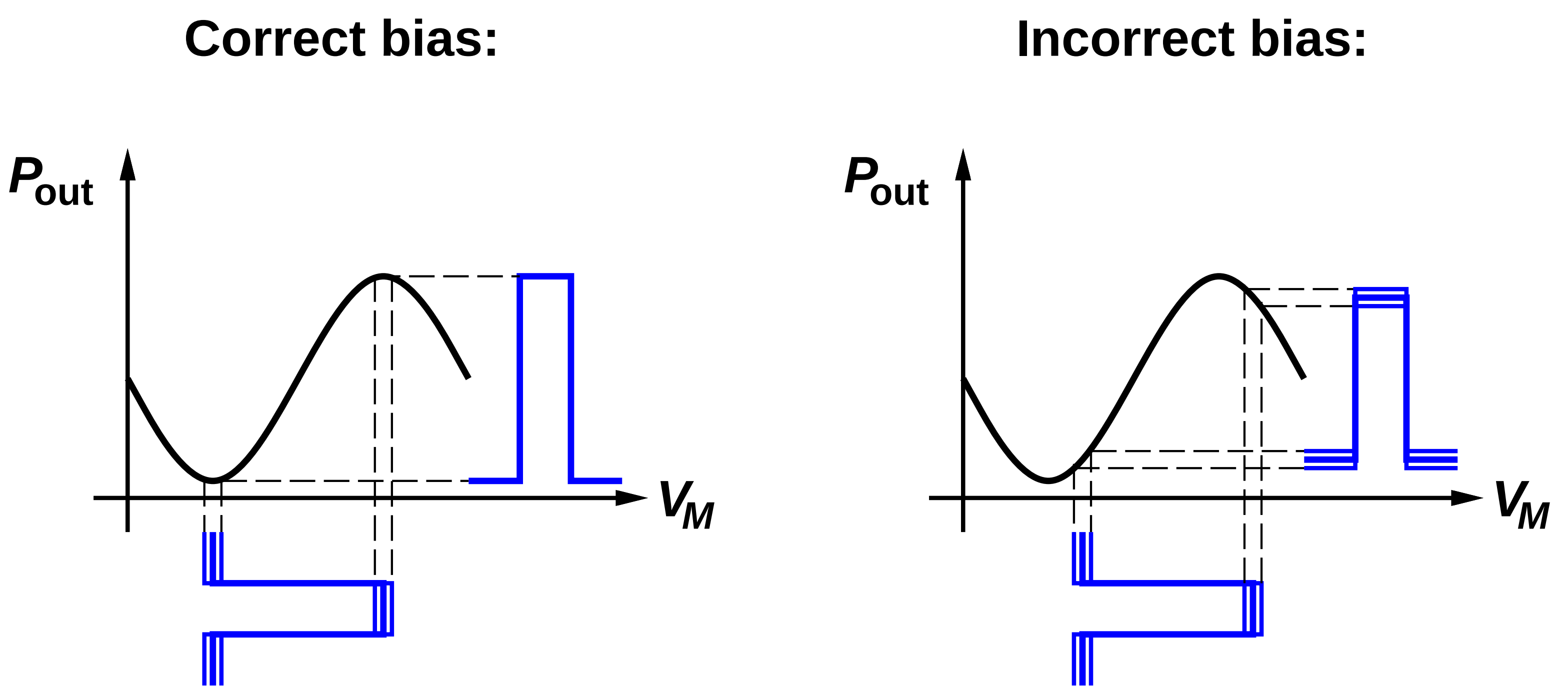
- Laser life: 1 ... 10 years (high temperature)
  10 ... 100 years (cooled to room temperature)
- Automatic end–of–life (EOL) detection
  - → Detect when APC fails
  - → Simple extension to APC circuit

Automatic Bias Control (MZ Modulators)



- Mach−Zehnder modulators drift with time and temperature
  → Automatic bias control (ABC)

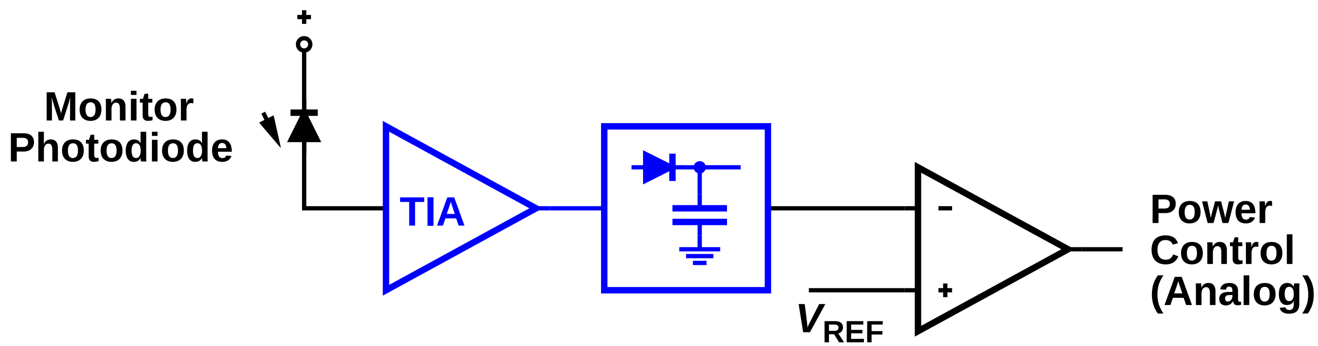
Automatic Bias Control (MZ Modulators)



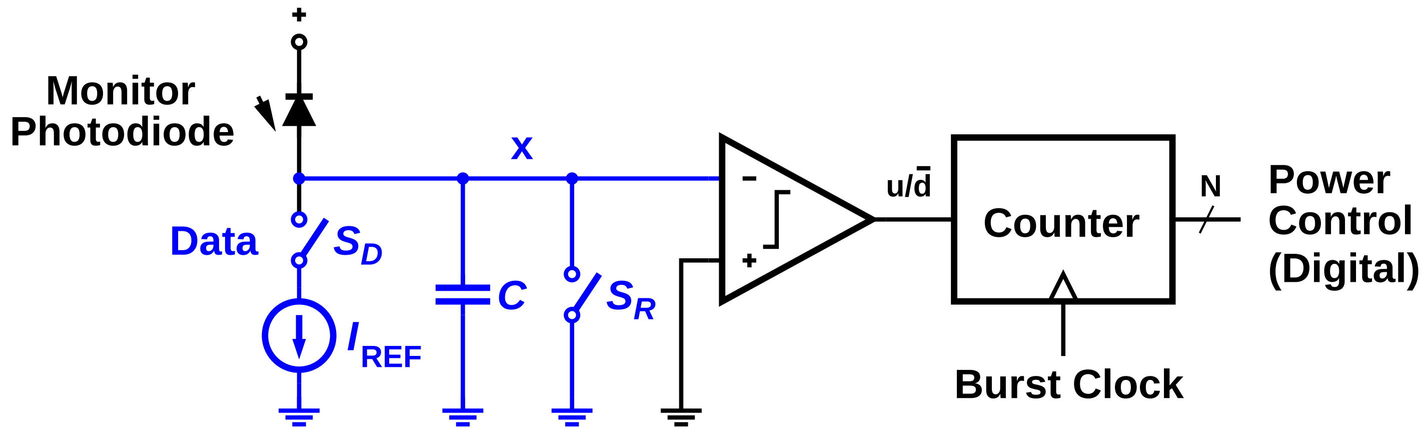
- **Modulate driver output voltage with small pilot tone:**
  - ➛ **Tone is suppressed, if bias correct**
  - ➛ **Tone appears in optical output, if bias incorrect**
  - ➛ **Phase of tone indicates direction of bias correction needed**

Burst−Mode Laser Driver

- High interburst extinction ratio required (>30 dB)
  - ➛ Turn bias current off in between bursts or no bias current at all
- Special APC required (signal not DC balanced)
  - ➛ Burst−mode APC based on peak detection:

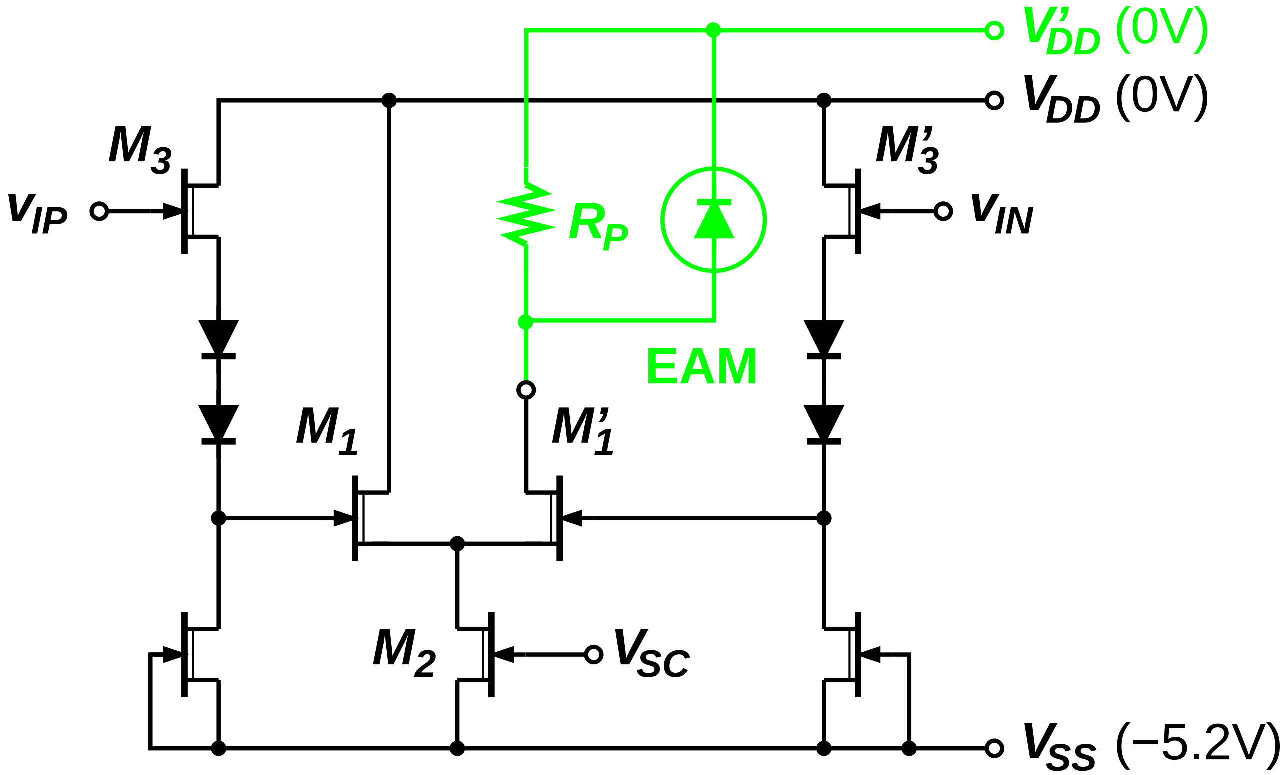


  - ➛ Burst−mode APC based on integrate & dump:



MESFET, HFET Implementation (1)

- EAM−driver output stage:

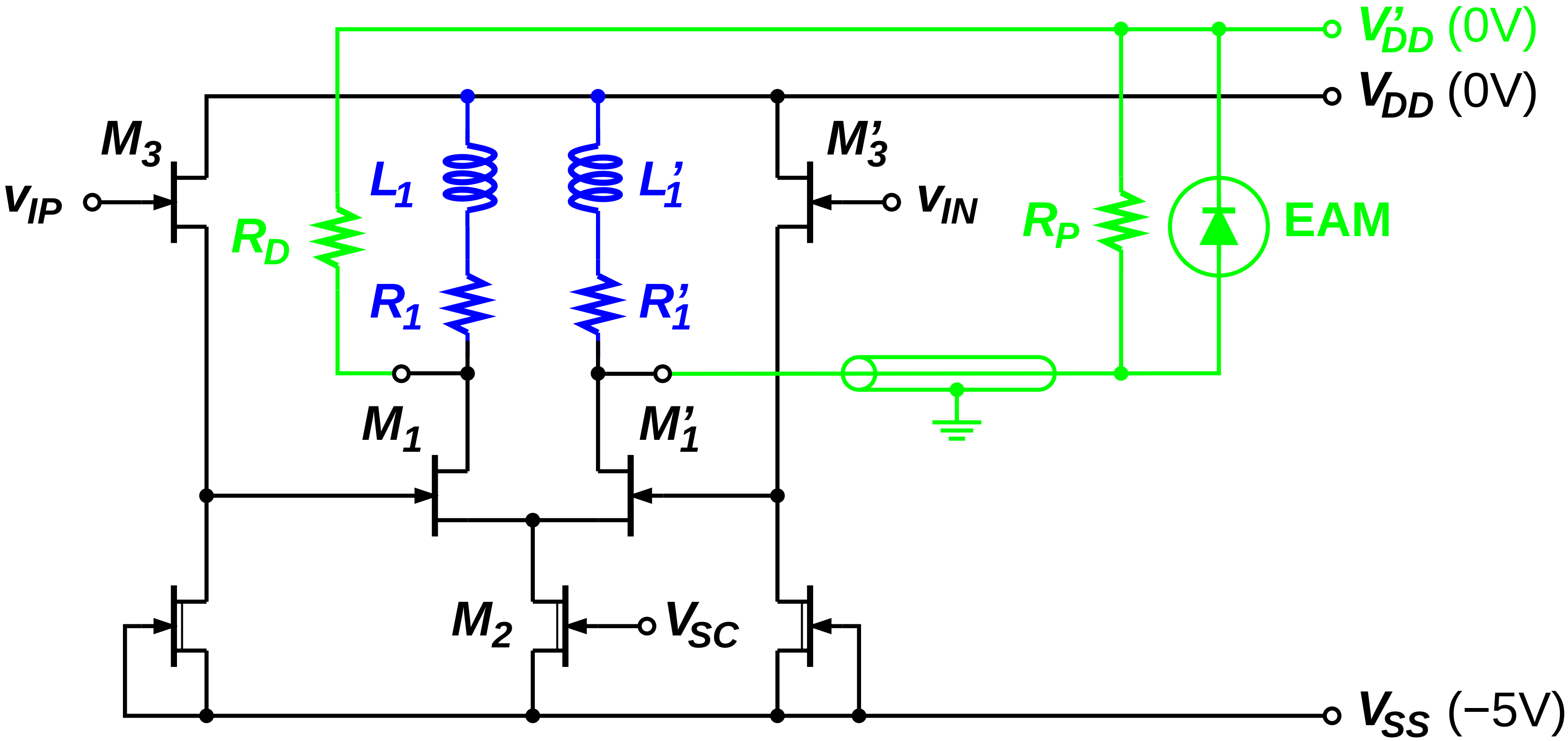


- Open−drain output (no back termination when used with TL)
- V_{SC} controls output−voltage swing

[Y. Suzuki et al. 1992]

MESFET, HFET Implementation (2)

- **EAM−driver (laser−driver) output stage:**



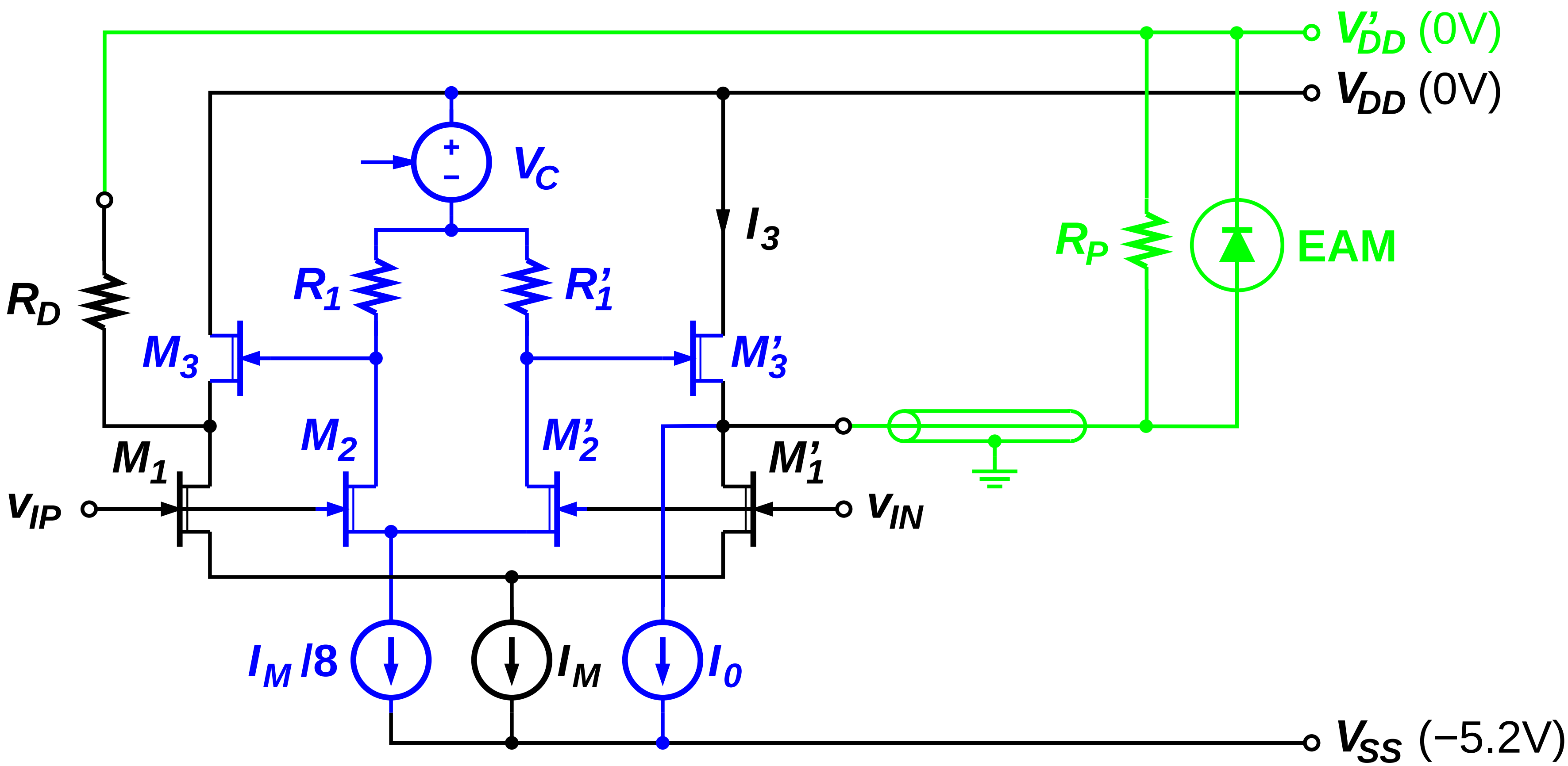
- **Passive back termination for transmission line**

  → **Avoid double reflections, but increased power dissipation**
- **Peaking inductors**

[Z. Lao et al. 1998]

MESFET, HFET Implementation (3)

- **EAM−driver (laser−driver) output stage:**



- **Active back termination for transmission line**

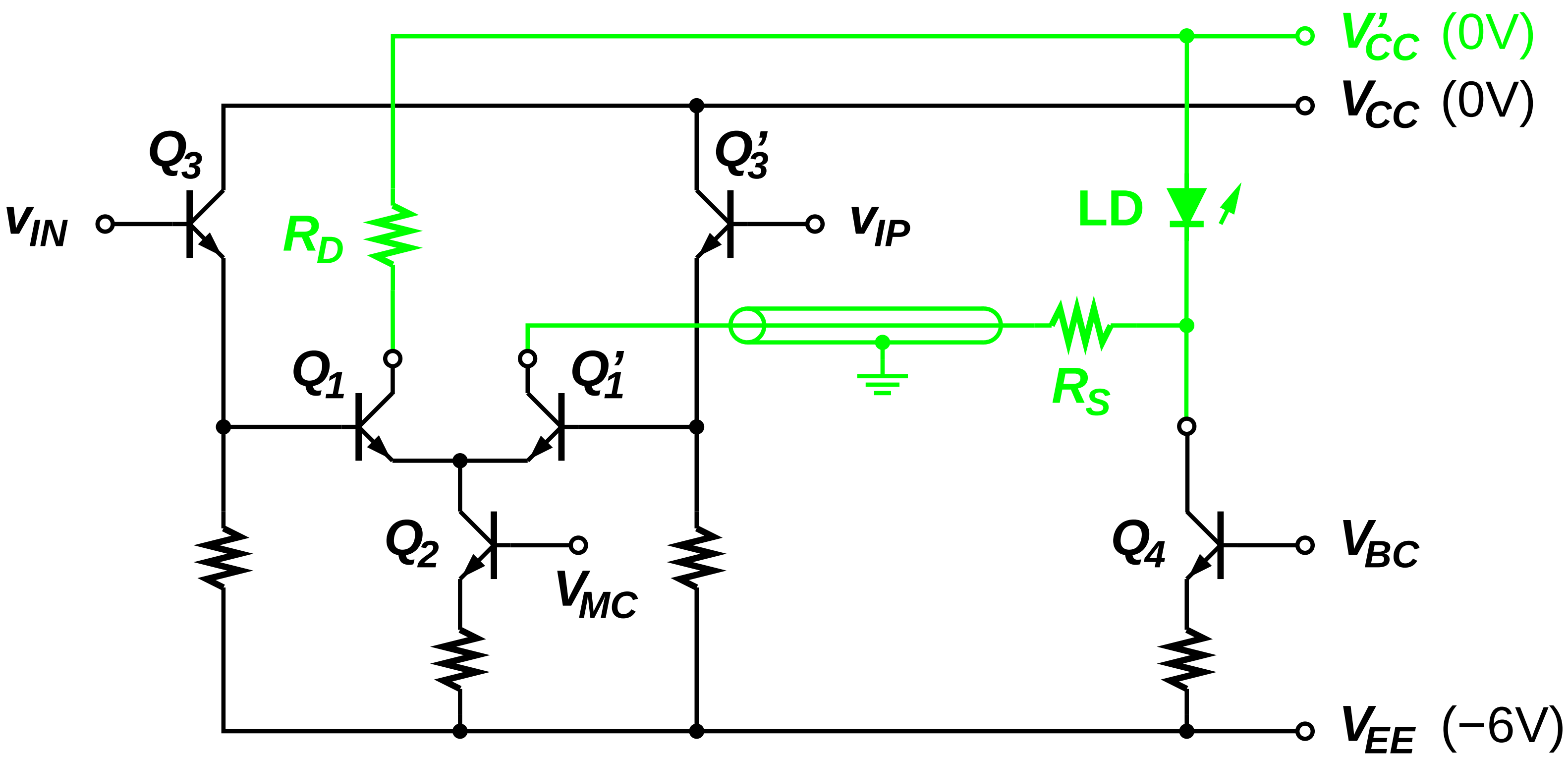
  → Lower power dissipation than passive back termination

- **$1/g_{m3}$ matches transmission line impedance**

[H. Ransijn et al. 2001]

BJT, HBT Implementation (1)

- **Laser−driver output stage:**

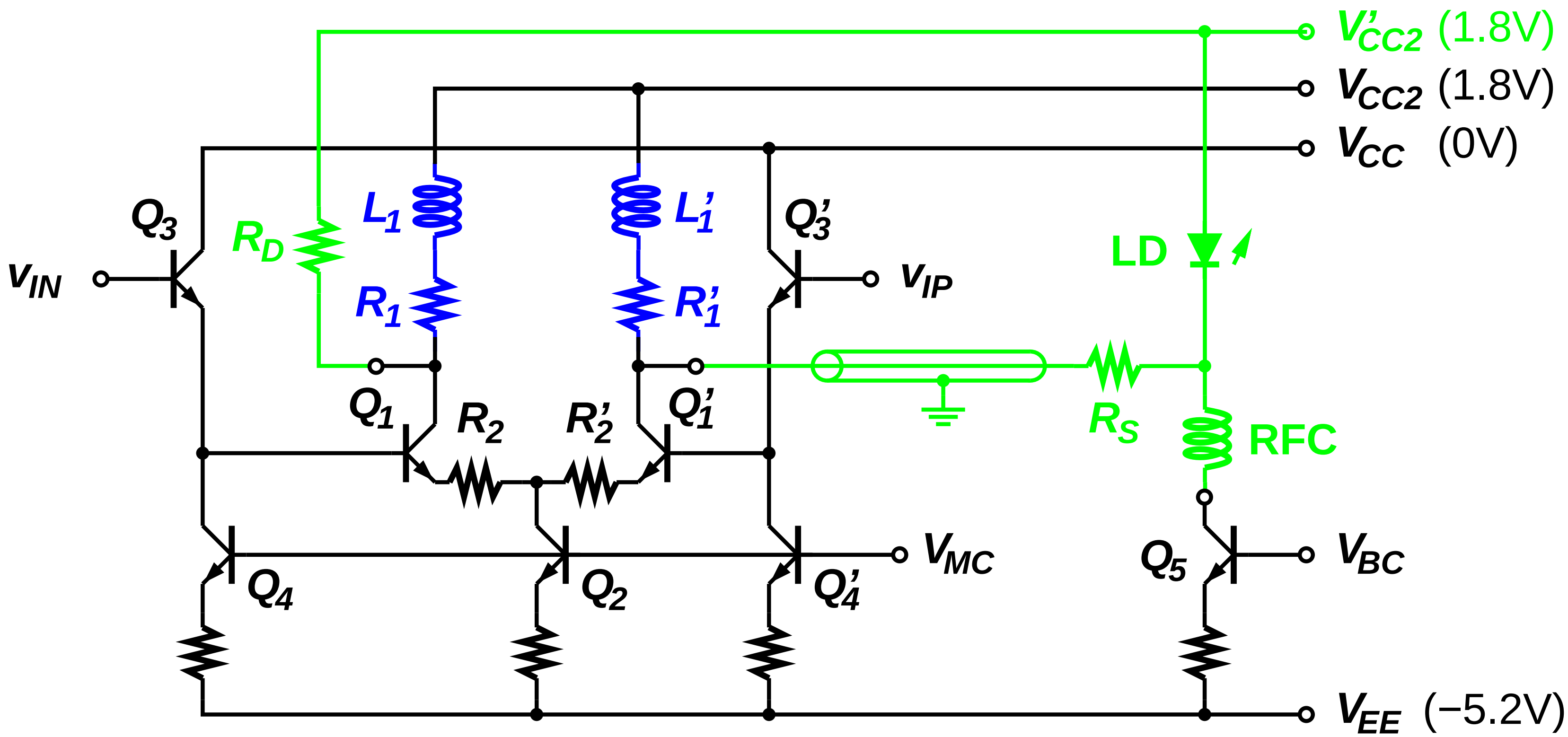


- **Open−collector output (no back termination for TL)**
- **V_{MC} controls modulation current**
- **V_{BC} controls bias current**

[H. Rein 1988]

BJT, HBT Implementation (2)

- **Laser−driver (modulator−driver) output stage:**

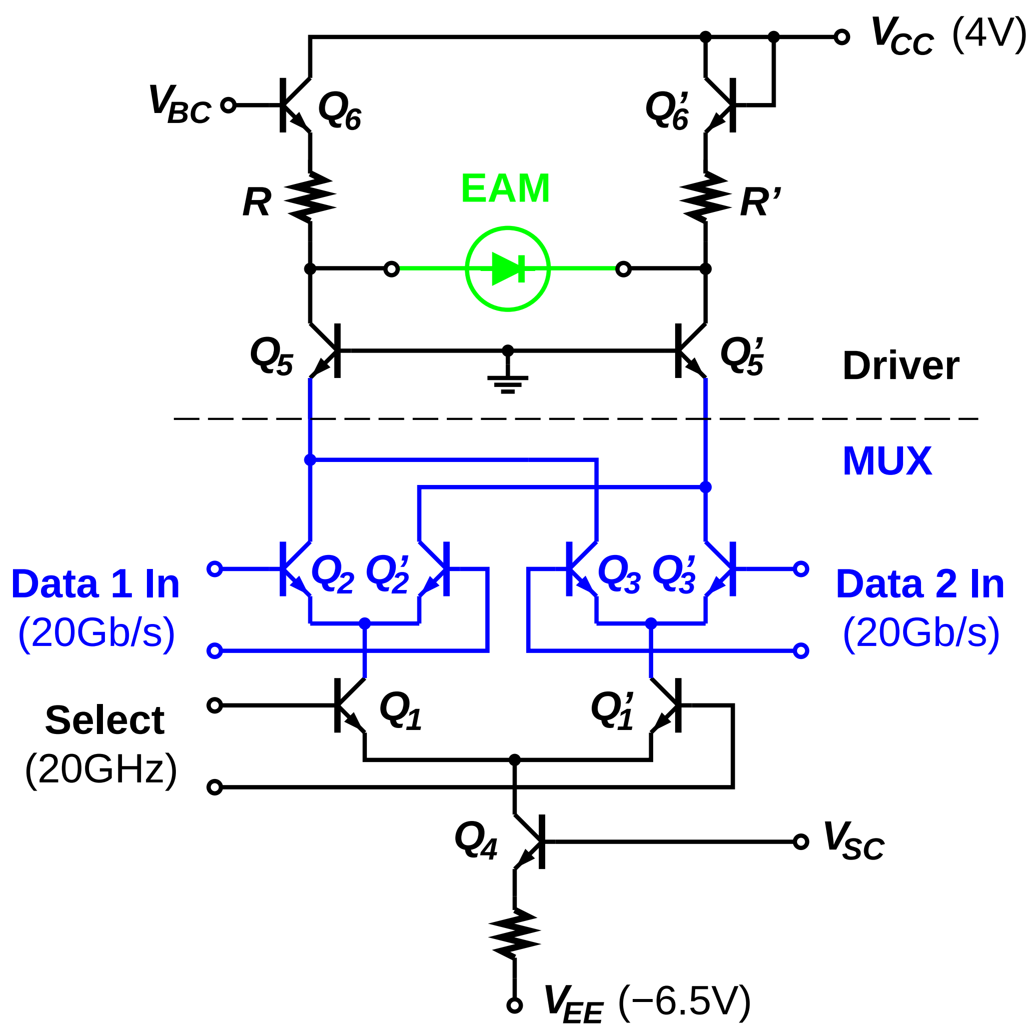


- **Passive back termination for transmission line**
  → **Avoid double reflections, but increased power dissipation**
- **Peaking inductors**
- **Bias current of emitter followers tracks modulation current**

[H. Rein et al. 1994]

BJT, HBT Implementation (3)

- **EAM driver with built−in MUX:**

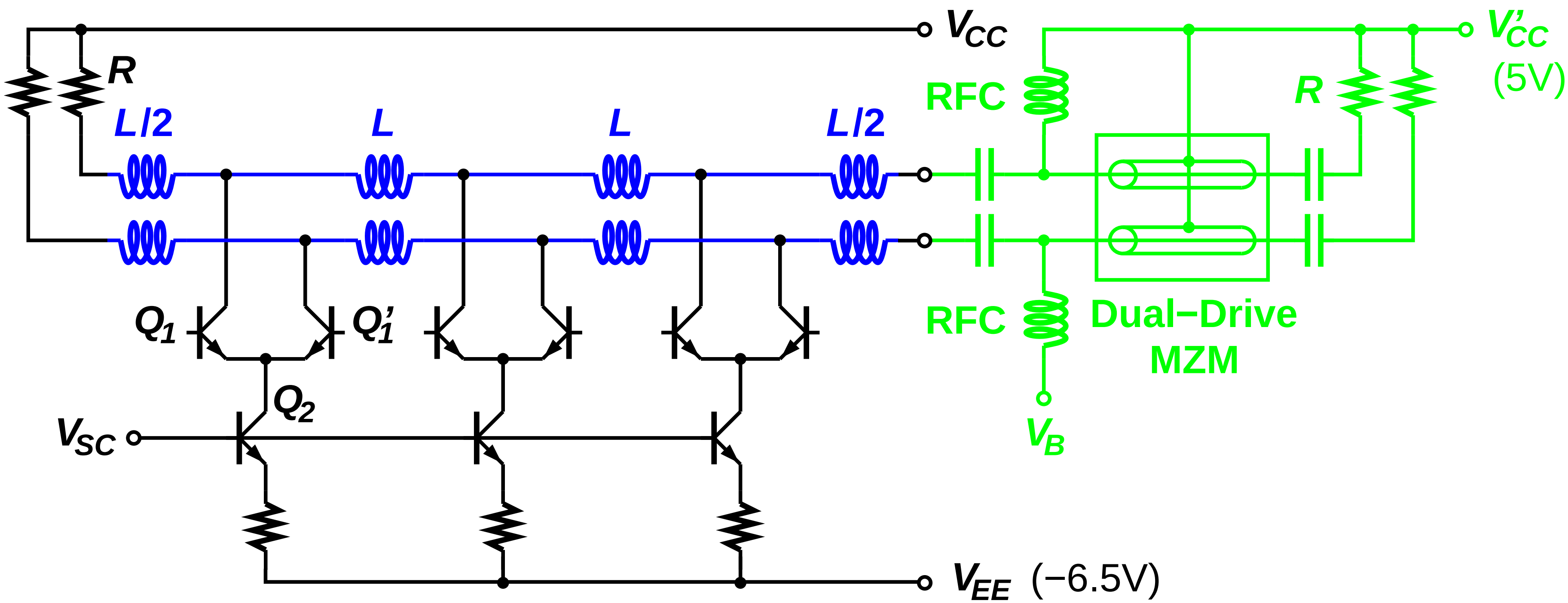


- **Combine MUX and output stage of driver (power MUX)**
- **Differential drive**
  → **Relaxes output swing, but symmetric EAM needed**
- V_{SC} **controls voltage swing**
- V_{BC} **controls bias voltage**

[M. Moller et al. 1998]

BJT, HBT Implementation (4)

- **MZM−driver output stage:**

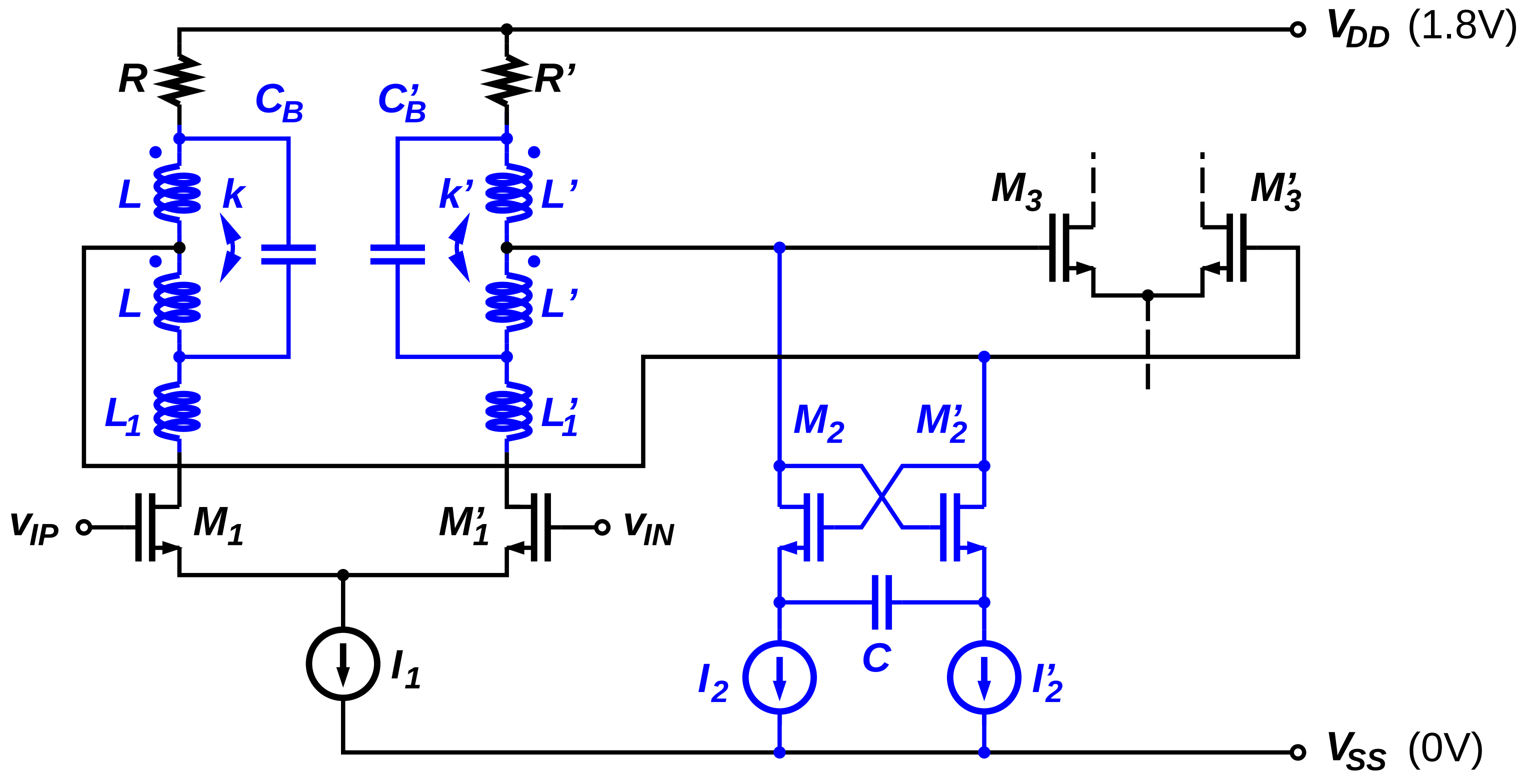


- **Distributed output stage (input TL and EFs not shown)**
- V_{SC} **controls voltage swing; use to inject pilot tone for ABC**
- V_B **MZM bias voltage**

[T. Wong et al. 1996]

CMOS Implementation (1)

- **Predriver for laser/modulator driver:**

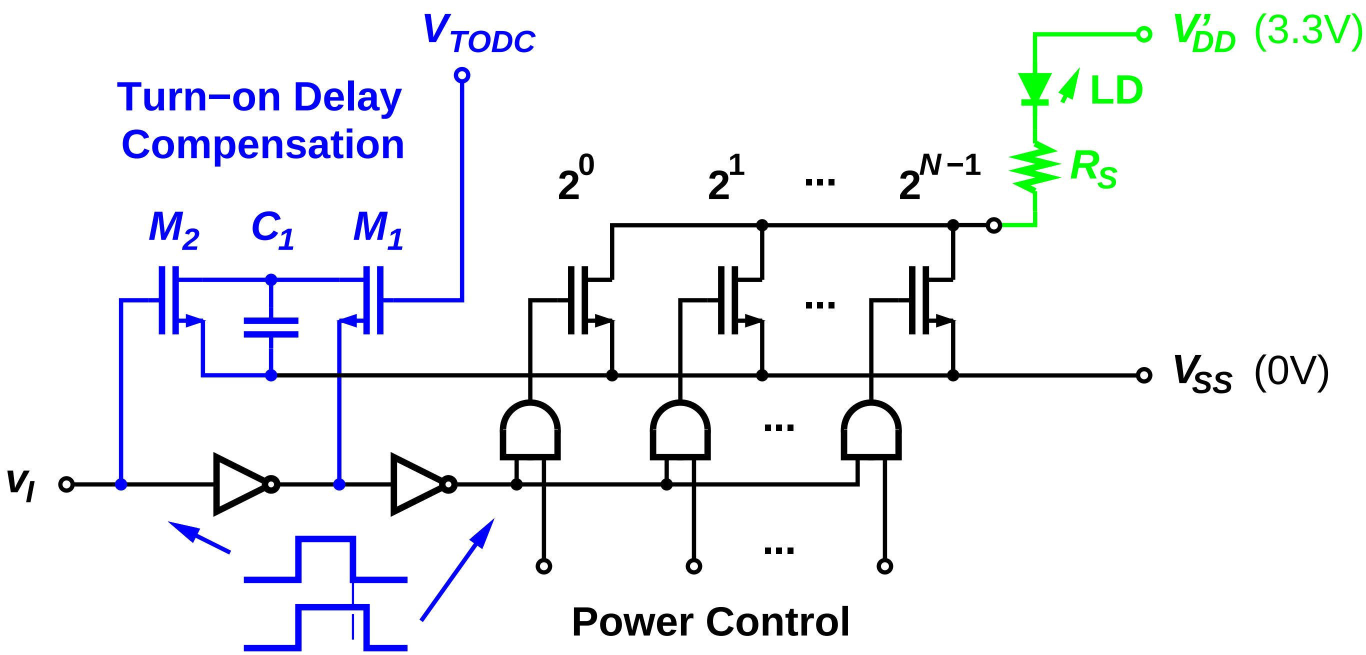


- **T−coil networks to drive output stage**
- **Negative impedance converter (NIC) to cancel capacitance**

[S. Galal et al. 2003]

CMOS Implementation (2)

- **Low−power burst−mode laser driver (155 Mb/s):**



- **No bias current; use turn−on delay compensation**
  - **→ High extinction ratio, low power consumption**
- **Current switching instead of current steering**
  - **→ Low power consumption**
- **Digital power control**

[E. Sackinger et al. 2000]

Research Directions

- **Higher speed: 40 Gb/s and beyond**
  - **Use heterostructure devices (HBTs and HFETs) based on compound semiconductors (SiGe, GaAs, InP)**
- **Higher integration: OEIC**
  - **Integrate driver & laser on same InP substrate (monolithic)**
  - **Integrate driver & laser using flip−chip technology**
- **Lower power:**
  - **Use low supply voltage**
  - **Avoid TL and matching resistors by copackaging driver & laser**
- **Lower cost:**
  - **Use mainstream technology (CMOS, BiCMOS)**
  - **Driver as part of a CMOS "system on a chip"**