MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

SINGAPORE-MIT ALLIANCE
Program on Advance Materials for Micro and Nano Systems

MIT6.772/SMA5111 COMPOUND SEMICONDUCTOR DEVICES

Problem Set No. 3

Issued: March 20, 2003 **Due:** April 3, 2003

NOTE: If needed, use parameter values from the list of materials properties at the end of Problem Set 2.

Problem 1 -

(a) Design a GaAs MESFET made on n-type GaAs, $N_d = 10^{17}$ cm^{-3}, to have a pinch-off voltage of 0 V, i.e., find what the channel thickness, a, must be. Assume the barrier height, ϕ_B, is 0.8 V.

(b) If the channel length, L, is 0.5 μm and its width, W, is 100 μm, what is the maximum low-field conductance the channel have assuming the maximum forward bias that can be applied to the gate before there is excessive gate conduction, $V_{GS,max}$, is 0.5 V? Use a value for the electron mobility, μ_e, of 4000 cm^2/V-s.

(c) If the saturation velocity, s_{sat}, of the electrons is 10^7 cm/s, what is the maximum drain current through this device with $V_{GS} = 0.5$V, and at what drain voltage does it occur? Assume a uniform channel field, v_{DS}/L, to do the calculation. Also, comment on how good an assumption this is.

Problem 2 -

Draw the schematic of a direct-coupled FET logic (DCFL) inverter. Plot the v_{IN}-v_{OUT} transfer characteristic of this inverter with a power supply of 2 V, and under two conditions: (a) With the output terminal open circuited. (b) With the output connected to the input of an identical stage.

Assume that the drain current of the MESFET's can be modelled as a square-law device, i.e., with an expression identical to that used to model MOSFETs, with V_T replaced by V_P and with the following parameter values: Enhancement-mode device: $V_P = 0.1$ V and $K = 0.1$ mA/V^2. Depletion-mode device: $V_P = -0.5$ V and $K = 0.1$ mA/V^2. Assume that the gate diode of the MESFET can be modelled as a break-point diode with a turn-on voltage of 0.8 V.

Problem 3 -

Consider a heterojunction bipolar transistor made with an $Al_{0.4}Ga_{0.6}As$ emitter 0.5 μm thick doped n-type with $N_D = 5 \times 10^{16}$ cm^{-3}, a GaAs base 0.05 μm wide doped p-type with $N_A = 1 \times 10^{19}$ cm^{-3}, and a GaAs collector 2 μm thick doped n-type with $N_D = 5 \times 10^{16}$ cm^{-3}. The emitter-base junction is graded to remove the conduction band spike, but you can ignore this graded region and assume the emitter is all $Al_{0.4}Ga_{0.6}As$

when the composition matters. Refer to table at the end of Problem Set 2 for the properties of the AlGaAs and GaAs.

(a) Calculate the emitter defect of this device, where the emitter defect is defined as the ratio of the hole current across the emitter-base junction to the total emitter-base junction current, i.e., the hole plus electron currents.

(b) What is the sheet resistance of the base region in ohms per square? Ignore the depletion region widths.

(c) What is the collector-base junction capacitance per unit area with a reverse bias of 2 Volts?

(d) Calculate the base transit time of this transistor.

Please use the following mobilities:
Al0.4Ga0.6As
μe=600 cm2/V·s
μh=100 cm2/V·s
GaAs:
μe=4000 cm2/V·s
μh=400 cm2/V·s