Lecture 38 - Bipolar Junction Transistor
(cont.)

May 9, 2007

Contents:

1. Non-ideal effects in BJT in FAR

Reading material:

del Alamo, Ch. 11, §11.5 (§§11.5.1, 11.5.3, 11.5.4, 11.5.5 but only qualitatively)

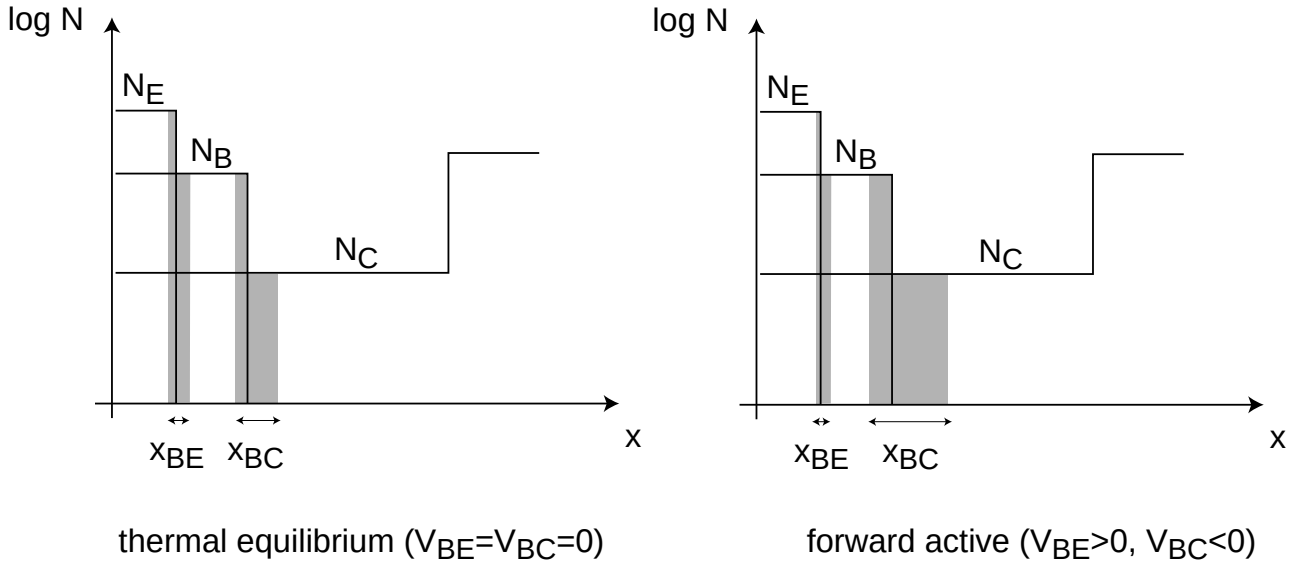
Key questions

- Why are the output characteristics of a BJT in FAR not perfectly flat?
- What is the maximum voltage that the collector of a BJT can sustain in FAR? What are the key design issues for the breakdown voltage?
- Why does the performance of a BJT degrade at high collector current?
- How does one model the base resistance in a BJT?

1. Non-ideal effects in BJT

□ Base-width modulation

V_{BE} and V_{BC} affect x_{BE} and x_{BC}, respectively $\Rightarrow W_B = f(V_{BE}, V_{BC})$.



thermal equilibrium (V_{BE}=V_{BC}=0) forward active (V_{BE}>0, V_{BC}<0)

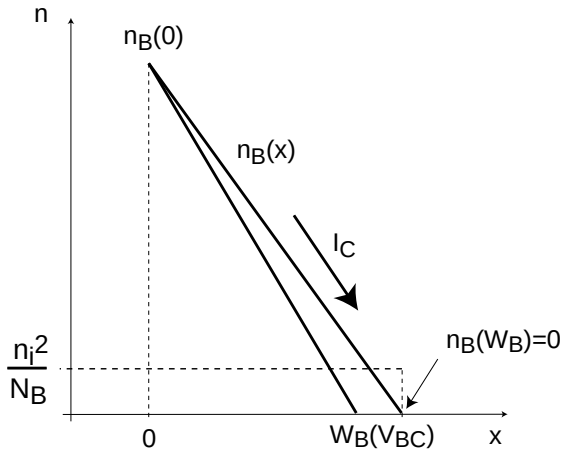
- *Early effect*: impact of V_{BC} on W_B

$$|V_{BC}| \uparrow \Rightarrow x_{BC} \uparrow \Rightarrow W_B \downarrow \Rightarrow I_C \uparrow,\ I_B\ unchanged$$

- *Reverse Early effect*: impact of V_{BE} on W_B

$V_{BE} \uparrow \Rightarrow x_{BE} \downarrow \Rightarrow W_B \uparrow \Rightarrow$ smaller I_C than ideal $\Rightarrow \beta_F \downarrow,\ I_B\ unchanged$

□ *Early effect*: impact of V_{BC} on $W_B \Rightarrow I_C = f(V_{BC})$



V_{BC} more negative $\Rightarrow$ $W_B(V_{BC}) \downarrow \Rightarrow I_C(V_{BC}) \uparrow$

To capture first-order impact, linearize $W_B(V_{BC})$:

$$W_B(V_{BC}) \simeq W_B(V_{BC}=0)(1+\frac{V_{BC}}{V_A})$$

V_A is *Early voltage*:

$$V_A = \frac{qN_BW_{Bo}}{C_{jco}}$$

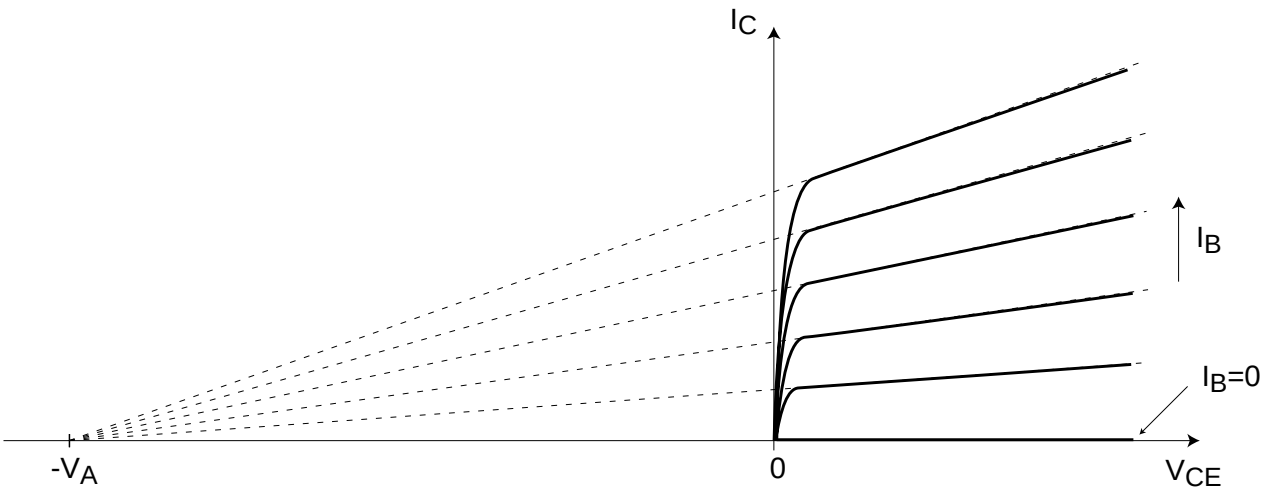
Impact on I_C:

$$I_C(V_{BC}) \simeq \frac{I_C(V_{BC}=0)}{1+\frac{V_{BC}}{V_A}} \simeq I_C(V_{BC}=0)(1-\frac{V_{BC}}{V_A})$$

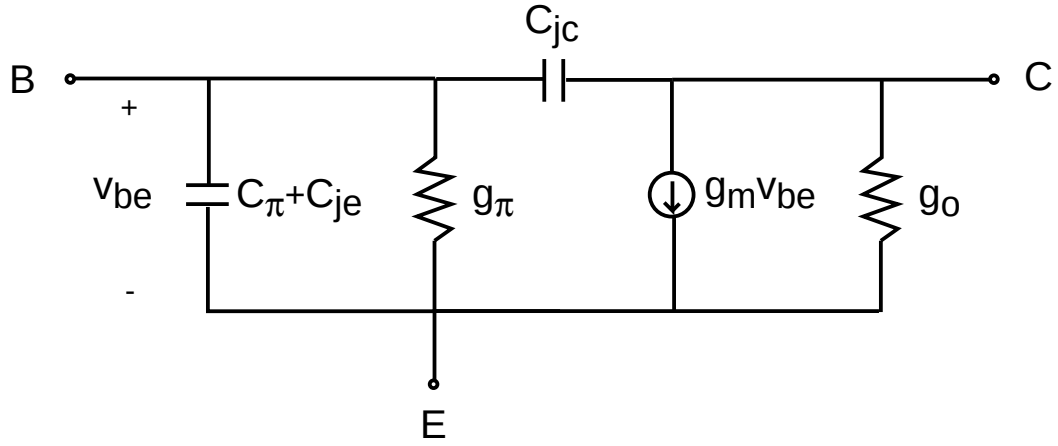
Also, since I_B unchanged:

$$\beta_F(V_{BC}) = \frac{\beta_F(V_{BC}=0)}{1+\frac{V_{BC}}{V_A}} \simeq \beta_F(V_{BC}=0)(1-\frac{V_{BC}}{V_A})$$

Manifestation of Early effect in output characteristics:



Main consequence of Early effect: finite slope in output characteristics in FAR: output conductance.



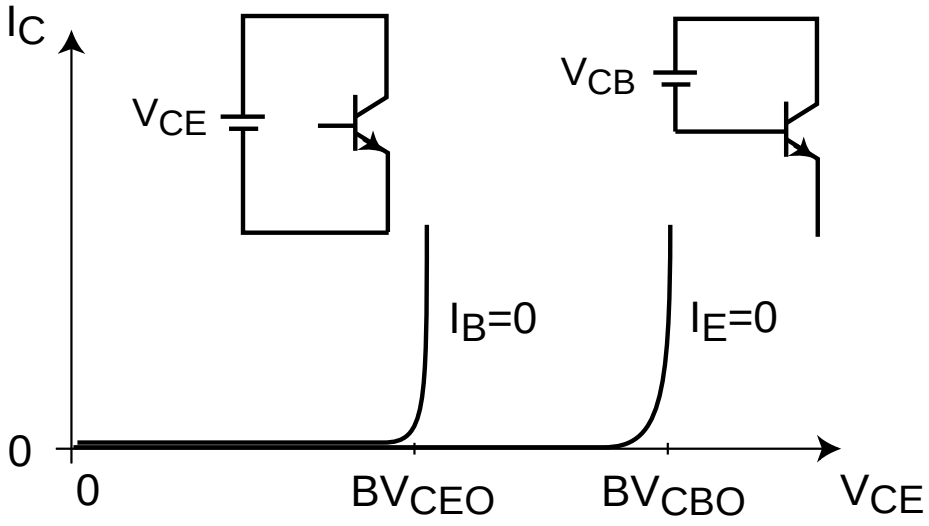
with g_o given by:

$$g_o = \frac{I_C}{V_A}$$

□ Avalanche breakdown

Sudden rise in I_C for large reverse V_{CB}.

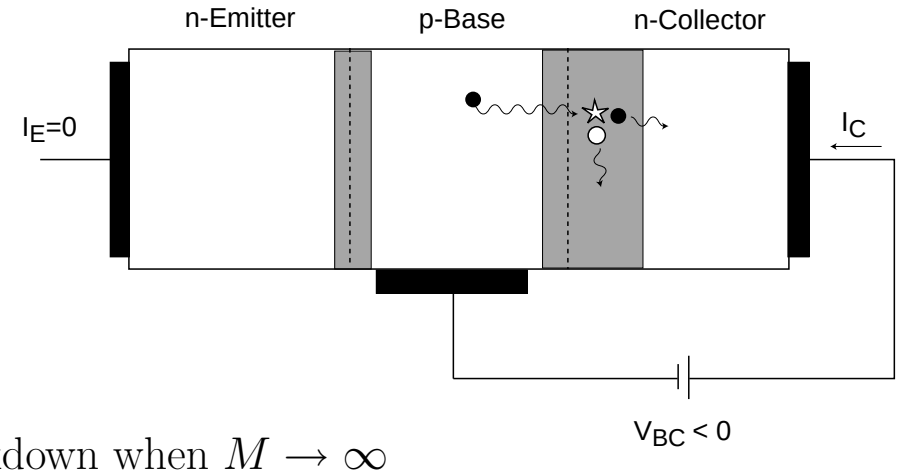
Key issue: breakdown voltage depends on terminal configuration:



Experimental observation:

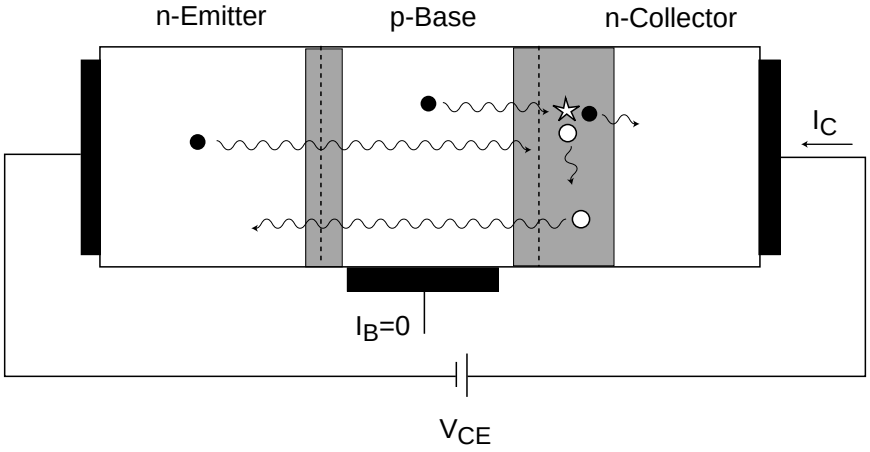
$$BV_{CEO} < BV_{CBO}$$

• Common-base configuration: breakdown as in isolated p-n junction



$\Rightarrow$ breakdown when $M \rightarrow \infty$

• Common-emitter configuration: BE and BC junctions interact in a *positive feedback loop*



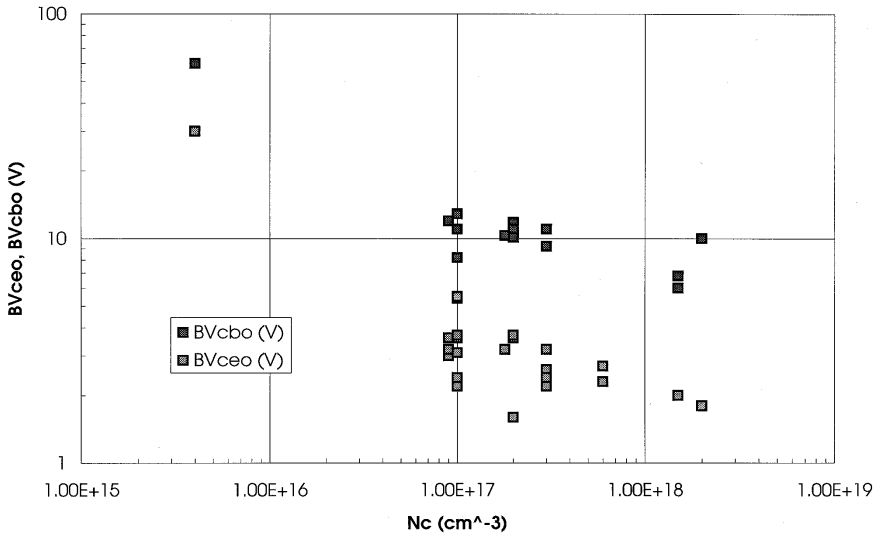
With $I_B = 0$ (or fixed), holes generated in B-C junction must be injected into E $\Rightarrow$ B-E goes into forward bias $\Rightarrow$ $I_C \uparrow$.

Breakdown occurs at finite M *and* enhanced by high β_F:

$$M_{crit} \simeq 1 + \frac{1}{\beta_F}$$

Key dependencies:

- $N_C \uparrow \Rightarrow BV_{CEO} \downarrow,\ BV_{CBO} \downarrow$



- $\beta_F \uparrow \Rightarrow BV_{CEO} \downarrow$ but BV_{CBO} unchanged $\Rightarrow$ don't want more β_F than necessary!.

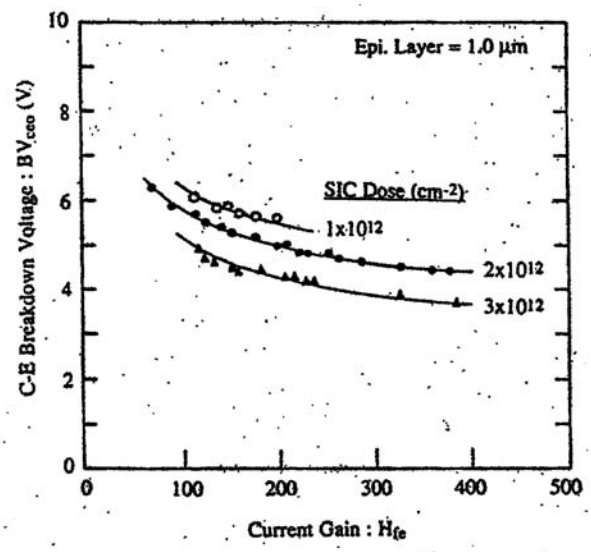


Fig. 12. Collector-to-emitter breakdown voltage dependence on current gain.

Yamaguchi, T., et. al. "Process and Device Characterization for a 30-GHz fT Submicrometer Double Poly-Si Bipolar Technology Using BF2 -implanted Base with Rapid Thermal Process." *IEEE Transactions on Electron Devices* 40, no. 8 (1993): 1484-1495. Copyright 1993 IEEE. Used with permission.

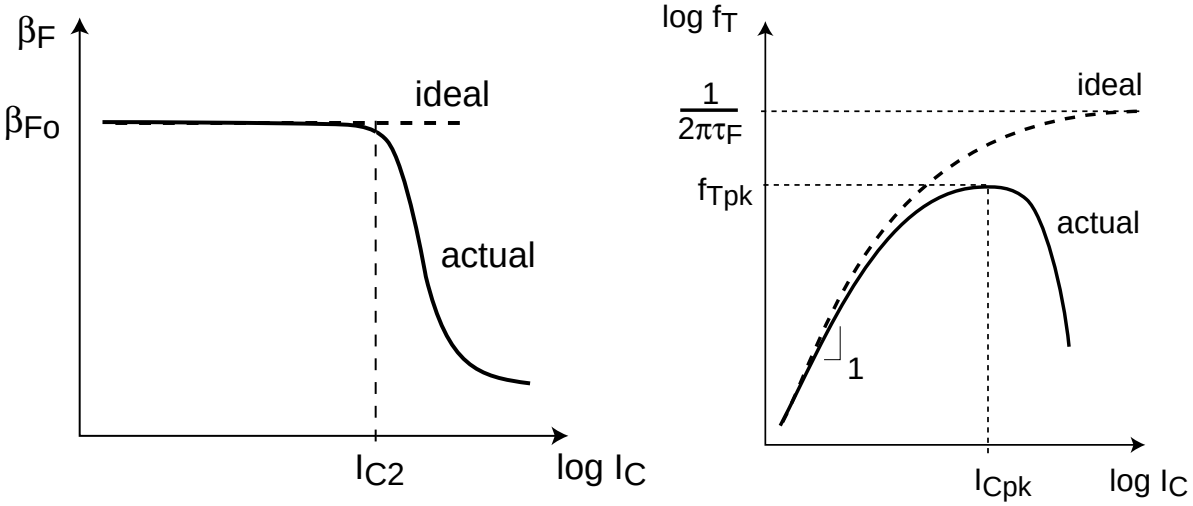
□ High collector current effects

As $I_C \uparrow$, electron velocity in collector $\uparrow$. But, there is a limit: v_{sat}.

Then, as I_C approaches:

$$I_{CK} = qA_E N_C v_{sat}$$

the electrostatics of the collector are profoundly modified $\Rightarrow$ transistor performance degrades:



To first order:

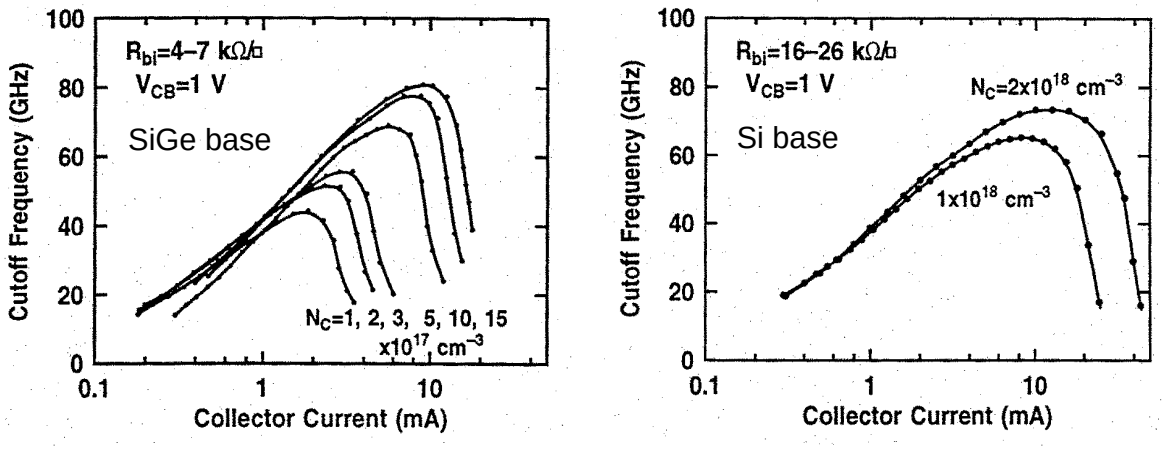
$$I_{C2} \simeq I_{Cpk} \simeq I_{CK}$$

Main origin: formation of *current-induced base* inside collector SCR $\Rightarrow$ effective quasi-neutral base width $\uparrow \Rightarrow \beta_F \downarrow \Rightarrow$ new delay component $\Rightarrow f_{Tpk} \downarrow$

Key design issue: N_C

$$N_C \uparrow \Rightarrow I_{CK} \uparrow \Rightarrow f_{Tpk} \uparrow$$

Experiments [Crabbé IEDM 1993]:



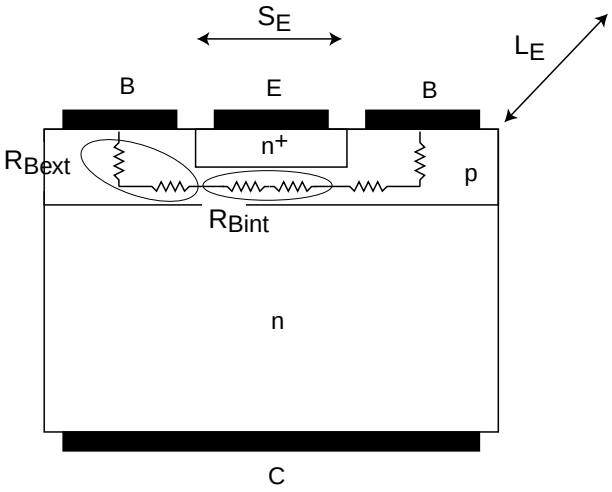
Key trade-off:

Crabbe, E.F., et. al. "Vertical Profile Optimization of Very High Frequency Epitaxial Si and SiGe-base Bipolar Transistors." *Technical Digest of the International Electron Devices Meeting, Washington, DC, December 5-8, 1993.* Piscataway, NJ: Institute of Electrical and Electronics Engineers, 1993, pp. 83-86. ISBN: 9780780314504. Copyright 1993 IEEE. Used with permission.

$$N_C \uparrow \Rightarrow BV \downarrow$$

□ Base resistance

Very important parasitic for digital and analog applications.



Two components to R_B:

- *external*: associated with ohmic contact to base and lateral flow through extrinsic base
- *internal*: associated with intrinsic base

$$R_B = R_{Bext} + R_{Bint}$$

Important issues:

1. R_{Bint} is distributed: how does it scale?
2. Non-linear behavior of R_{Bint} for high I_B

1. *Low-current resistance* (in absence of debiasing)

Define lateral resistance of intrinsic base:

$$R_{blat} = R_{shb}\frac{S_E}{L_E}$$

With:

$$R_{shb} = \frac{1}{q\mu_B N_B W_B}$$

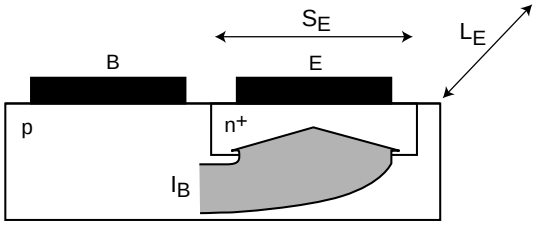
Clearly,

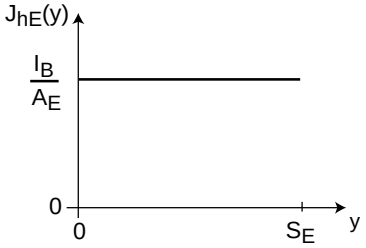
$$R_{Bint} < R_{blat}$$

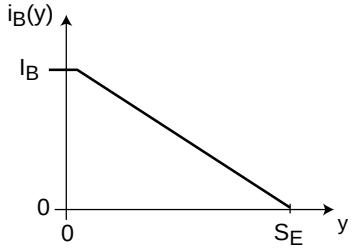
because not all I_B flows across entire intrinsic base.

But, what is proportionality constant?

• BJT with one base contact:







Assume small ohmic drop along base $\Rightarrow i_B(x)$ uniformly distributed:

$$i_B(x) = I_B(1 - \frac{x}{S_E})$$

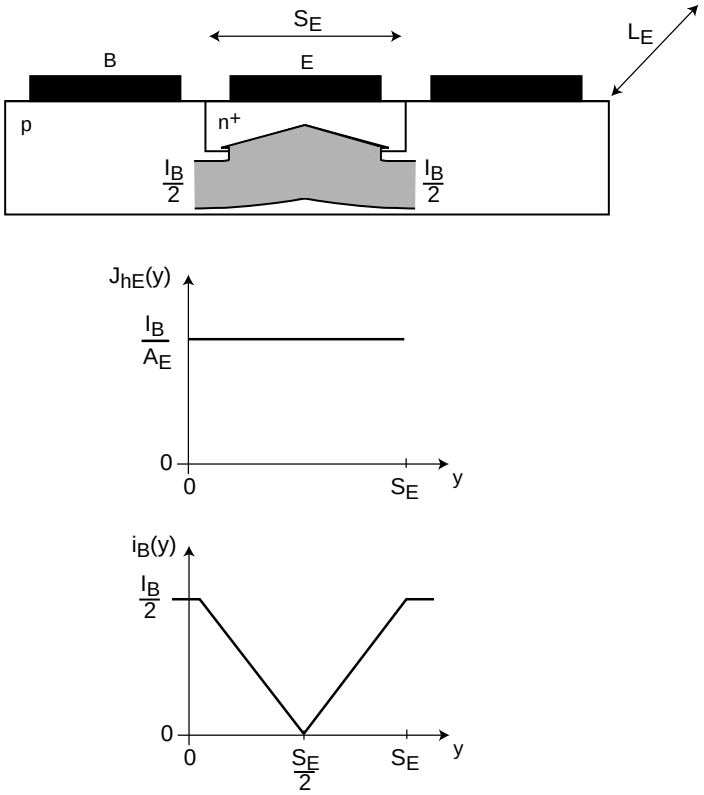
R_{Bint} obtained by examining power dissipation in base:

$$p_B = I_B^2 R_{Bint} = \int_0^{S_E} i_B^2(x) \frac{R_{shb}}{L_E} dx = I_B^2 \frac{1}{3} R_{shb} \frac{S_E}{L_E}$$

Then:

$$R_{Bint} = \frac{1}{3} R_{shb} \frac{S_E}{L_E} = \frac{1}{3} R_{blat}$$

• BJT with two base contacts:



Now:

$$i_B(x) = \frac{I_B}{2}(1 - \frac{2x}{S_E}) \quad \text{for } 0 \leq x \leq \frac{S_E}{2}$$

$$i_B(x) = \frac{I_B}{2}(\frac{2x}{S_E} - 1) \quad \text{for } \frac{S_E}{2} \leq x \leq S_E$$

Intrinsic base resistance:

$$R_{Bint} = \frac{1}{12} R_{blat}$$

This is a quarter of the design with one-base contact.

Total base resistance is:

$$R_B = R_{Bext} + R_{Bint}$$

To get small R_B:

- minimize $R_{Bext} \Rightarrow$ self-aligned process
- minimize $R_{Bint} \Rightarrow$
  - use two base contacts $\Rightarrow$ takes more space
  - increase $W_B \Rightarrow$ degrades frequency response
  - increase $N_B \Rightarrow$ hard, costly, $C_{je} \uparrow,\ BV_{EBO} \downarrow$
  - decrease S_E ($scaling$!) $\Rightarrow$ costly

Useful observation: *trade-off between R_B and I_C*

Remember:

$$I_C = I_S \exp \frac{qV_{BE}}{kT} = \frac{qA_E n_i^2 D_B}{N_B W_B} \exp \frac{qV_{BE}}{kT}$$

Then:

$$\frac{J_C}{R_{shb}} = q^2 n_i^2 D_B \mu_B \exp \frac{qV_{BE}}{kT}$$

rather independent of N_B or doping profile.

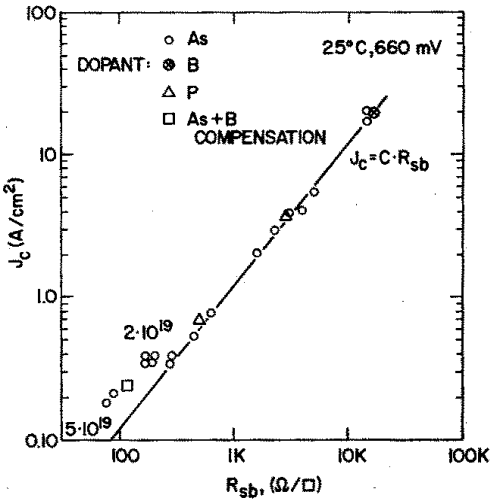
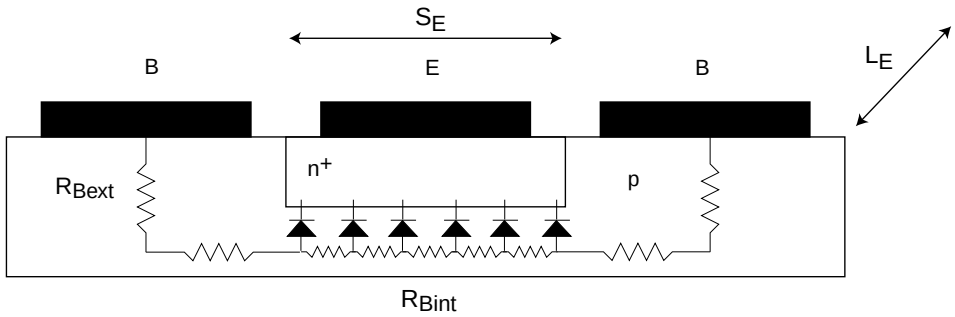


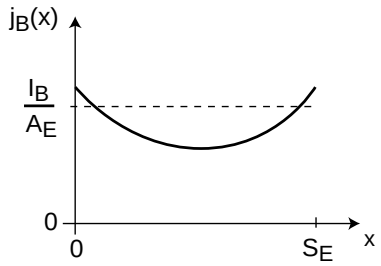
Fig. 3. Collector current density versus base sheet resistance measured at $T = 25°C$ and $V_{EB} = 0.660$ V. Included in this plot are the results from p-n-p transistors with As-doped base, P-doped base, from the n-p-n transistor with B-doped base, and p-n-p transistor with heavily compensated base region.

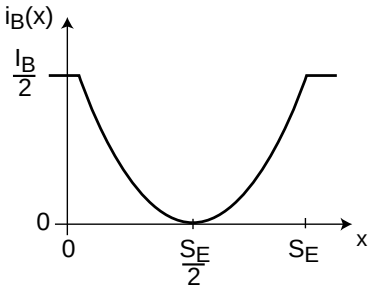
Tang, D. D. "Heavy Doping Effects in p-n-p Bipolar Transistors." *IEEE Transactions on Electron Devices* 27, no. 3 (1980): 563-570. Copyright 1980 IEEE. Used with permission.

2) *Non-linear behavior of R_B*

More accurate equivalent circuit model of distributed R_B:





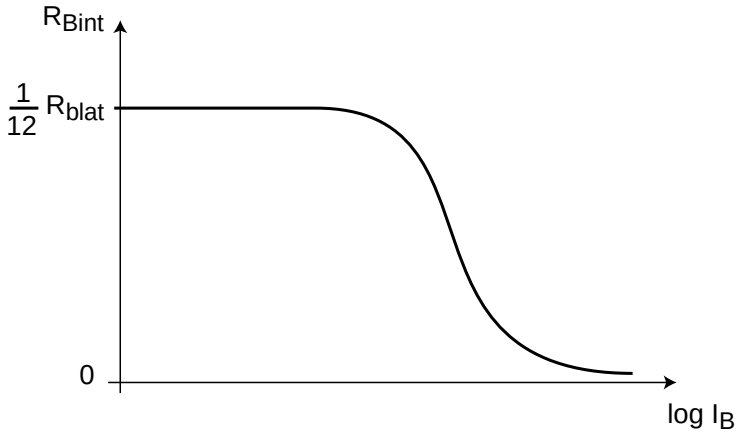


Non-linear B-E diode current $\Rightarrow$ non-uniform current distribution across base:

- base resistance "debiases" center of base
- current "crowds" at edges of base

Analytical model possible (but not pretty).

General behavior of R_{Bint}:



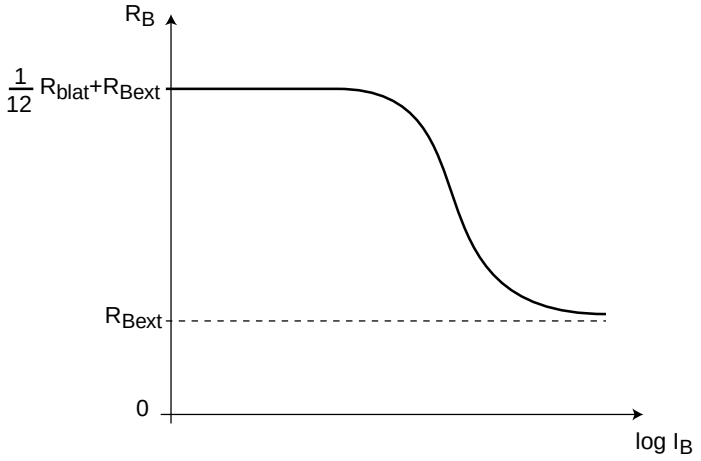
For negligible debiasing to occur:

$$I_B R_{blat} < 0.2\frac{kT}{q}$$

R_{Bin} drops by 50% at:

$$I_B R_{blat} \simeq 6\frac{kT}{q}$$

Overall behavior of R_B:



Consequences of base debiasing:

- R_B depends on $I_B \Rightarrow R_B$ depends on V_{BE} and I_C

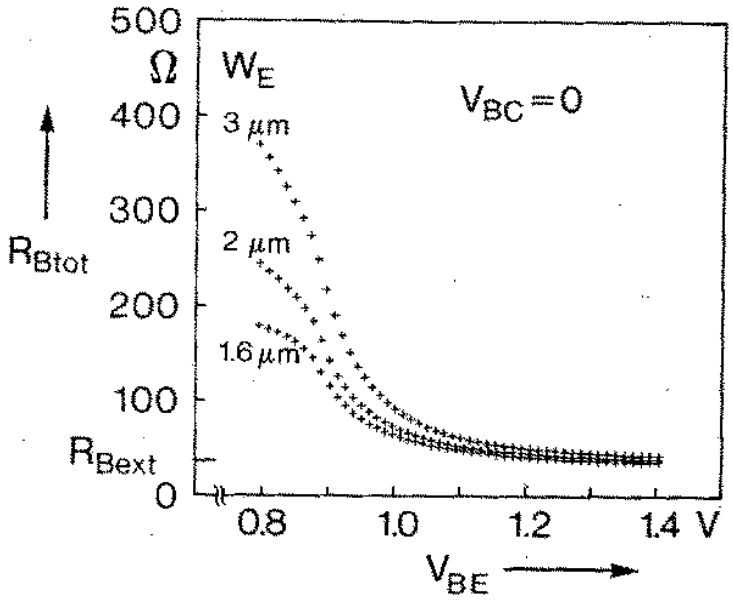


Fig. 2. Measured total base resistance R_{Btot} versus the base–emitter voltage V_{BE} for test structures with different emitter-window widths W_E, but the same emitter-window length ($L_E = 20$ μm).

Weng, J., J. Holz, and T. F. Meister. "New Method to Determine the Base Resistance of Bipolar Transistors." *IEEE Electron Device Letters* 13, no. 3 (1992): 158-160. Copyright 1992 IEEE. Used with permission.

- For high current,

$$R_{Bint} \rightarrow 0 \;\Rightarrow\; R_B \simeq R_{Bext} \text{ and independent of } S_E.$$

• Non-linear behavior of R_{Bint}:

$$small\text{-}signal\ resistance \neq large\text{-}signal\ resistance$$

Ohmic drop in R_B:

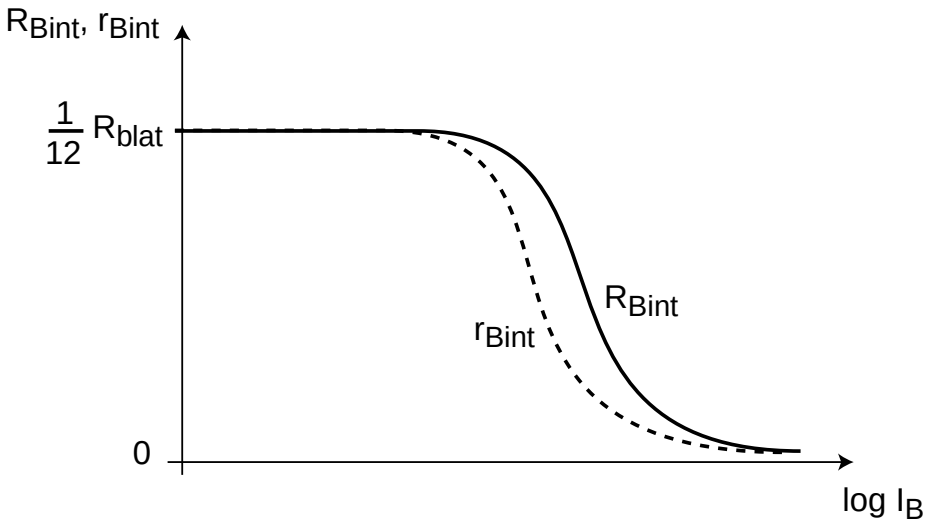
$$V_B = R_B I_B$$

Then, small-signal base resistance:

$$r_B = \frac{dV_B}{dI_B} = R_B + \frac{dR_B}{dI_B} I_B$$

Since $I_B \uparrow \Rightarrow R_B \downarrow$:

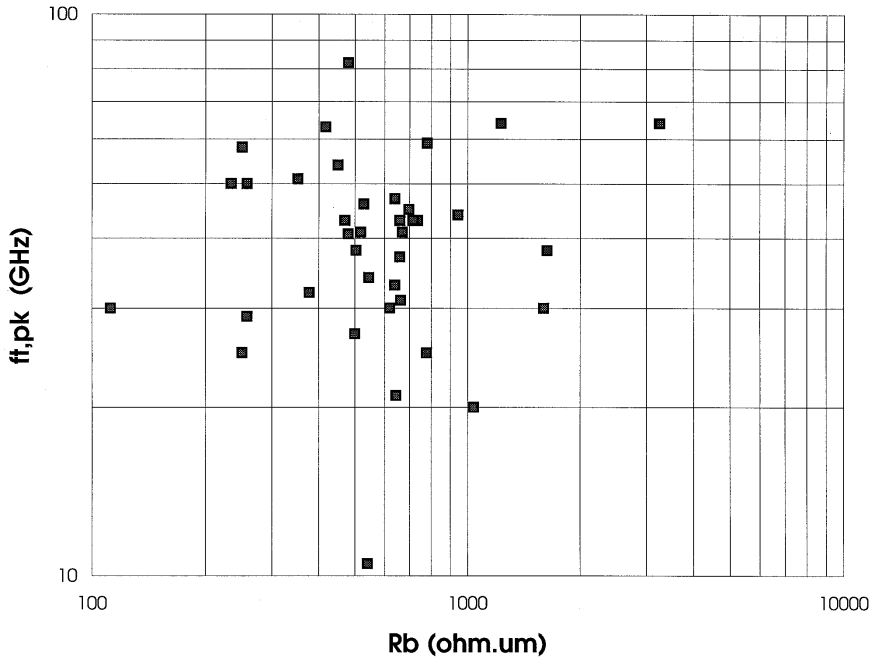
$$r_B \leq R_B$$



Consequences of R_B:

- R_B has no direct impact on f_T, but has indirect impact through constraint in base design.

  Actually, $f_{T,pk}$ does not appear correlated to R_B ($f_{T,pk}$ dominated by N_C):



- r_B crucially important to noise
- $r_B C_{jc}$ important time constant in high-frequency operation of BJT

Key conclusions

- *Early effect*: modulation of W_B by V_{BC} $\Rightarrow$ output conductance in output characteristics.

$$g_o = \frac{I_C}{V_A}$$

- Base-width modulation effects affect I_S and β_F, but not I_B.
- In avalanche breakdown in a BJT:

$$BV_{CEO} < BV_{CBO}$$

  because of transistor current gain.

- $\beta_F \uparrow \Rightarrow BV_{CEO} \downarrow$ w/o affecting BV_{CBO}.
- Key device design issue in avalanche breakdown:

$$N_C \uparrow \Rightarrow BV's \downarrow$$

- At high collector current, velocity saturation of electrons in collector $\Rightarrow$ performance degrades: $\beta_F \downarrow,\ f_T \downarrow$
- Maximum current:

$$I_{Cpk} \simeq qA_E N_C v_{sat}$$

- Two components in R_B:
  - R_{Bext}: associated with ohmic contact and transport through extrinsic base

  - R_{Bint}: associated with intrinsic base

- R_{Bint} is a distributed resistance $\Rightarrow$
  - $R_{Bint} < R_{blat}$
  - R_{Bint} is non linear in I_B.
- Consequence of non-linearity of R_{Bint} at high I_B: small-signal resistance different from large-signal resistance.
- Three technological approaches to reduce R_B:
  - use two base contacts
  - use self-aligned process
  - decrease S_E
- Fundamental trade-off between I_C and R_{shb}.