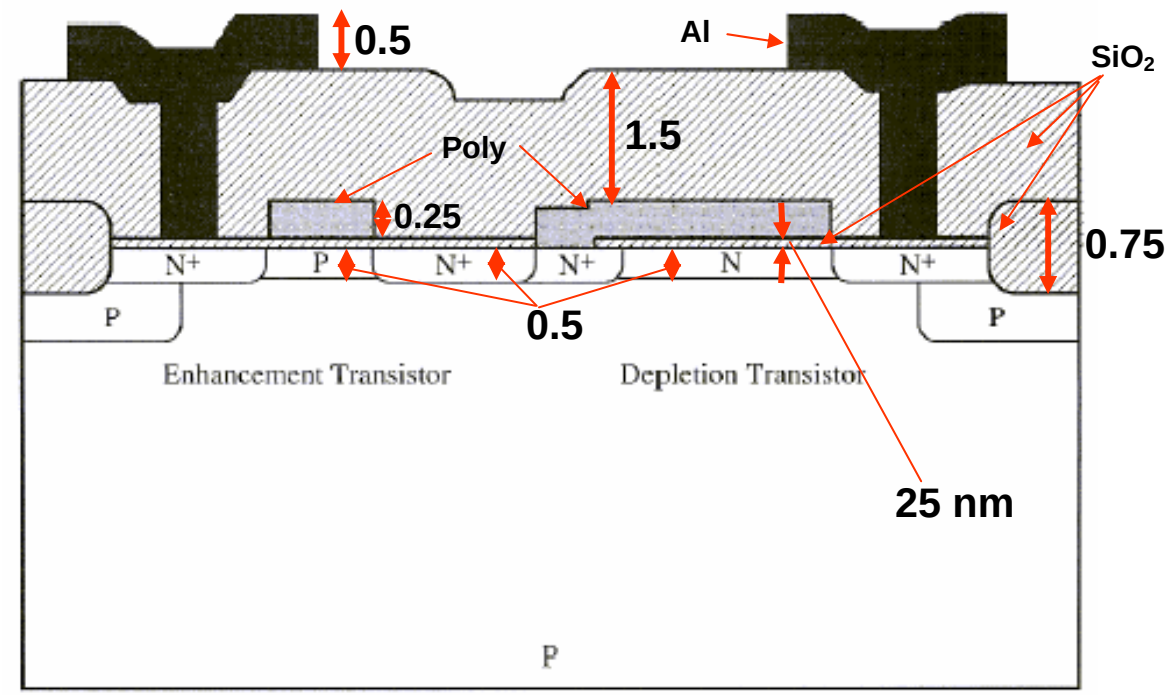
Massachusetts Institute of Technology
3.155J / 6.152J Micro/Nano Processing Technology
Fall Term 2005
Problem Set 8: CMOS

Out: November 16, 2005 **Due: November 23, 2005**

1) Design a process sequence (without detailed times/temperatures) for fabrication of the E/D NMOS device shown below. This process is slightly different from the process described in class in that the gate of the depletion-mode device makes direct contact to the source (as needed in the inverted circuit). You should sketch process cross-sections at each major step (similar to the cross-sections in lecture). Assume the poly is deposited using LPCVD and the thick oxide (1.5 micron) is deposited using a low temperature (400C) PECVD process.

2) Assume that the substrate doping is 10^{15} cm^{-3}. The source and drain junctions should have a doping concentration at the surface of 10^{20} cm^{-3} and 0.5 micron junction depths as indicated. The threshold adjustment implants should have a surface doping of 10^{17} cm^{-3}, and should drop to the substrate doping level at 0.5 microns from the surface. For the process you determined above:
   i) Calculate the oxidation temperature, time and ambient needed to form the LOCOS and gate oxides.
   ii) Calculate the implant doses needed to achieve the desired doping levels for the source/drain and two threshold adjust implants. Ignore the field adjust implant.
   iii) Calculate the anneal times/temperatures needed to 'drive-in' the three implants.
   iv) Show how to implement these anneals into the process flow in Problem 1.



Dimensions in microns unless noted otherwise